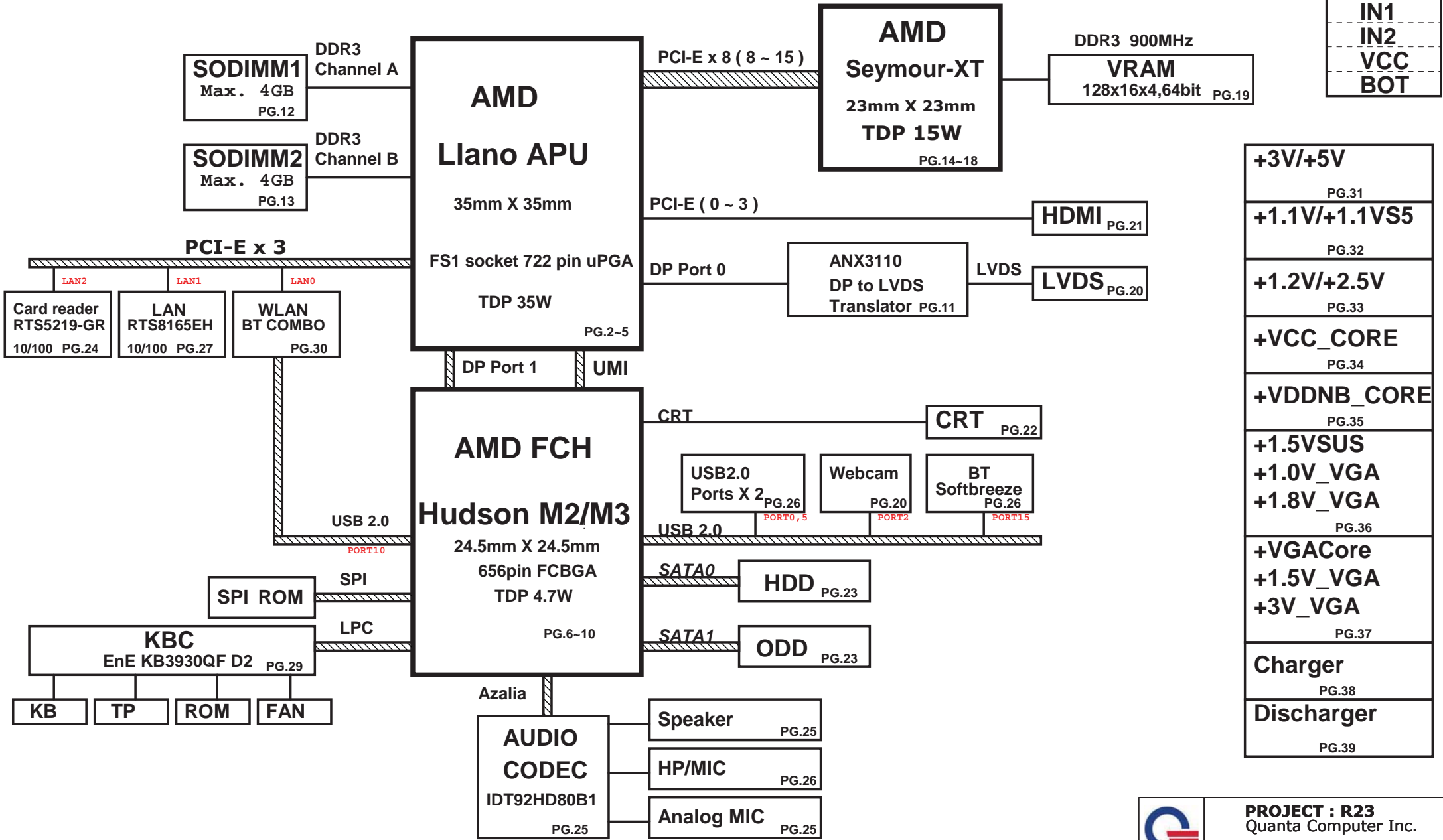



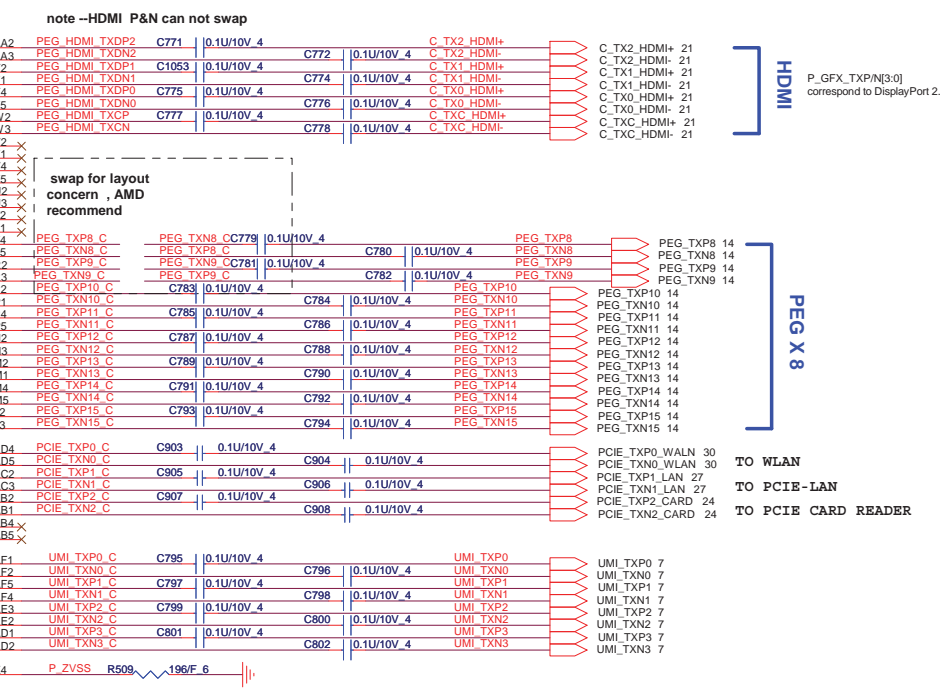
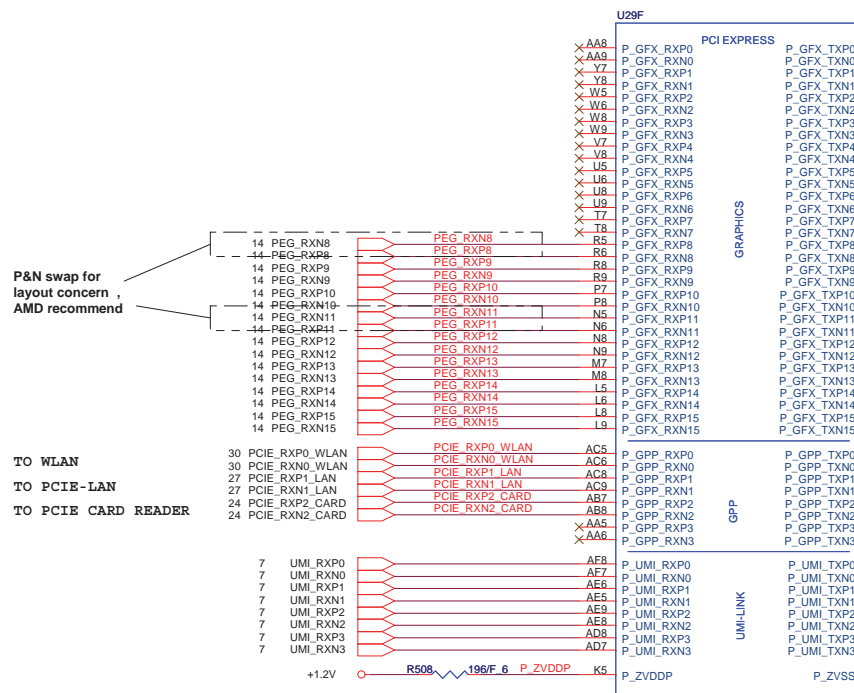
R23 AMD Sabin UMA/Muxless SYSTEM DIAGRAM

Stackup

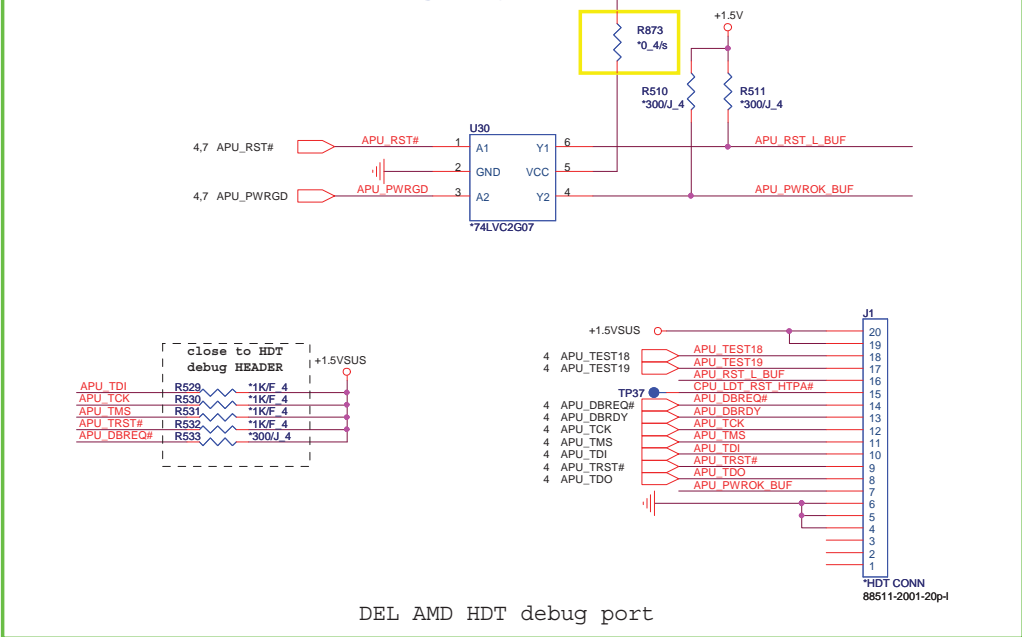
TOP
GND
IN1
IN2
VCC
BOT



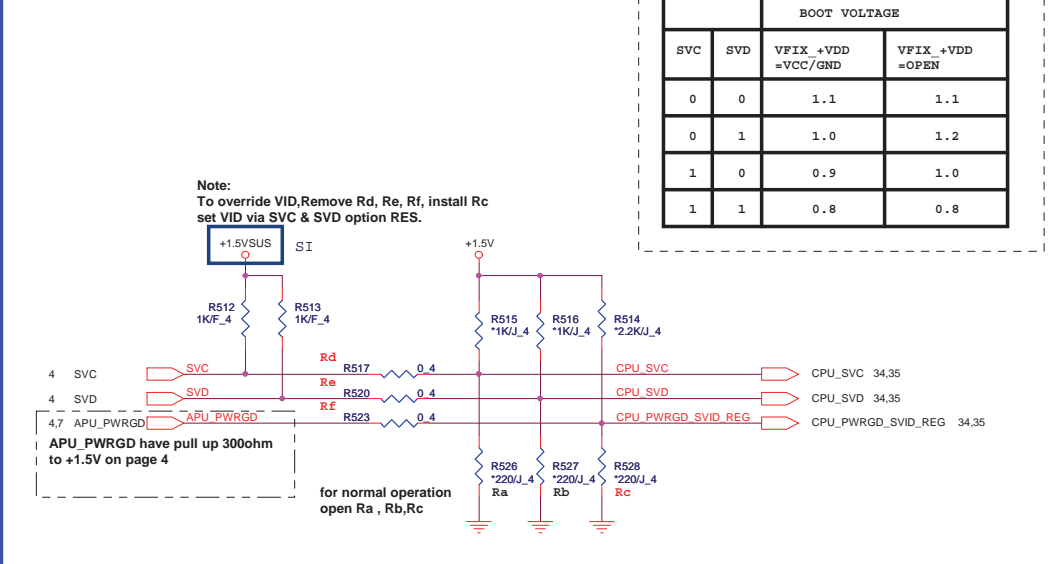
	PROJECT : R23		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number BLOCK DIAGRAM	
Date: Tuesday, May 03, 2011		Sheet 1 of 40	



HDT+ Connector for Debug only



VID Override Circuit

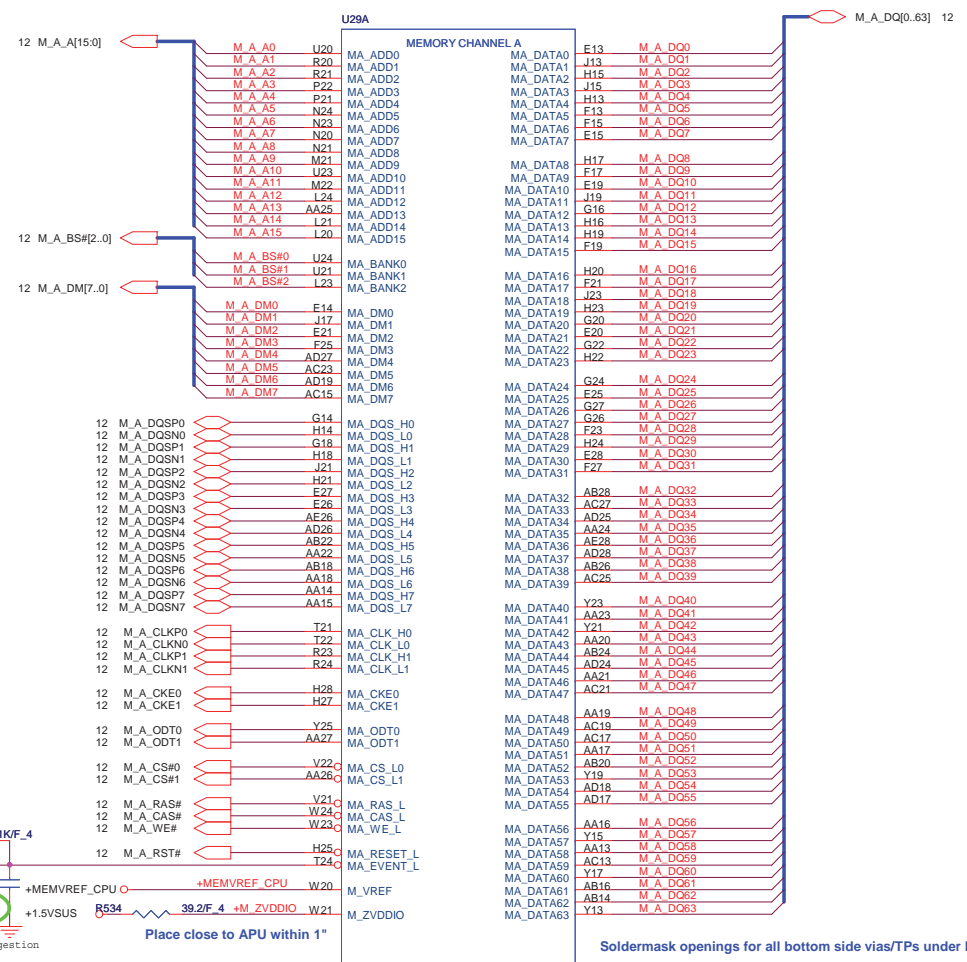


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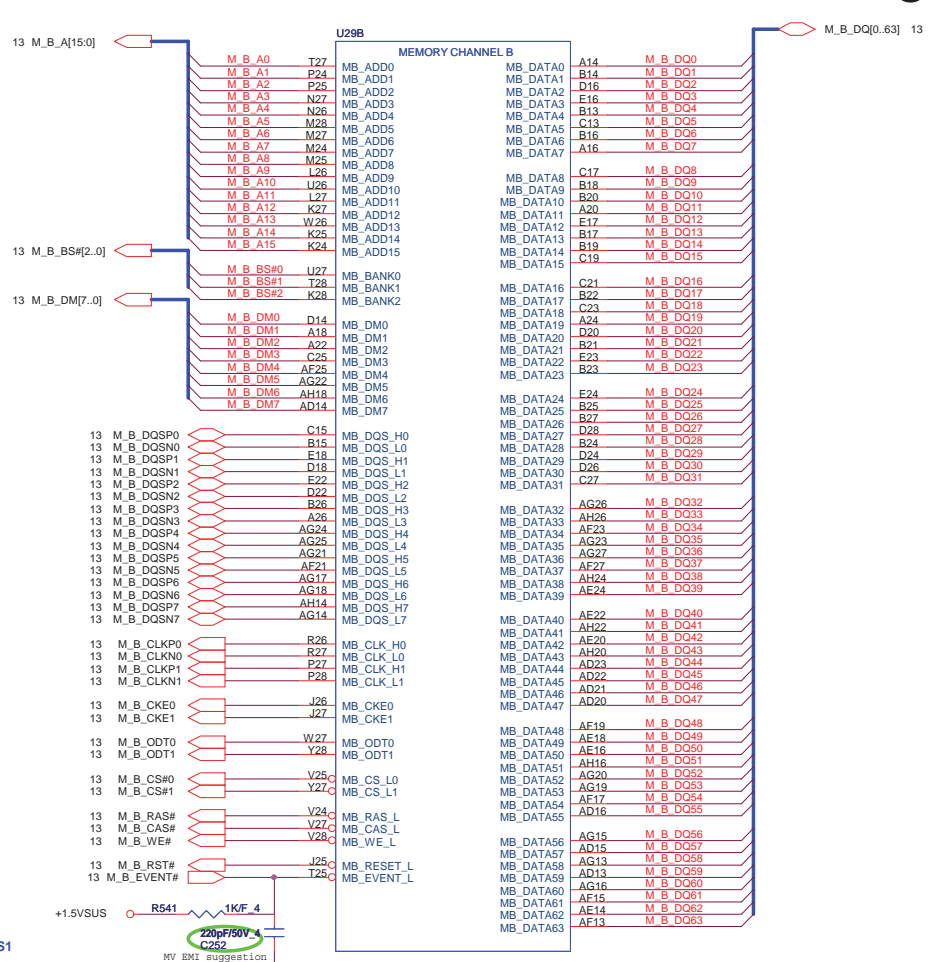
PROJECT : R23

Size Document Number **Liano PCIE/UMI/GPP** Rev. 1A

Date: Wednesday, May 04, 2011 Sheet 2 of 40

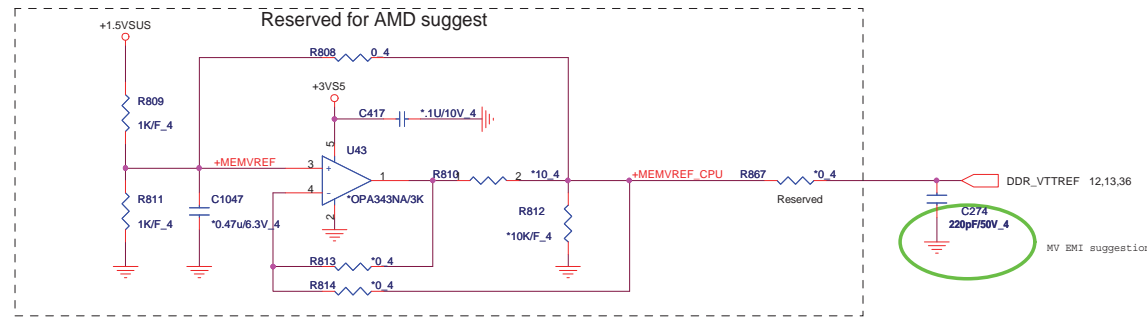


Llano APU



Llano APU

Soldermask openings for all bottom side vias/TPs under FS1

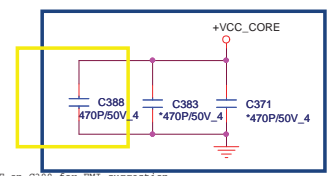


Quanta Computer Inc.
 PROJECT : R23

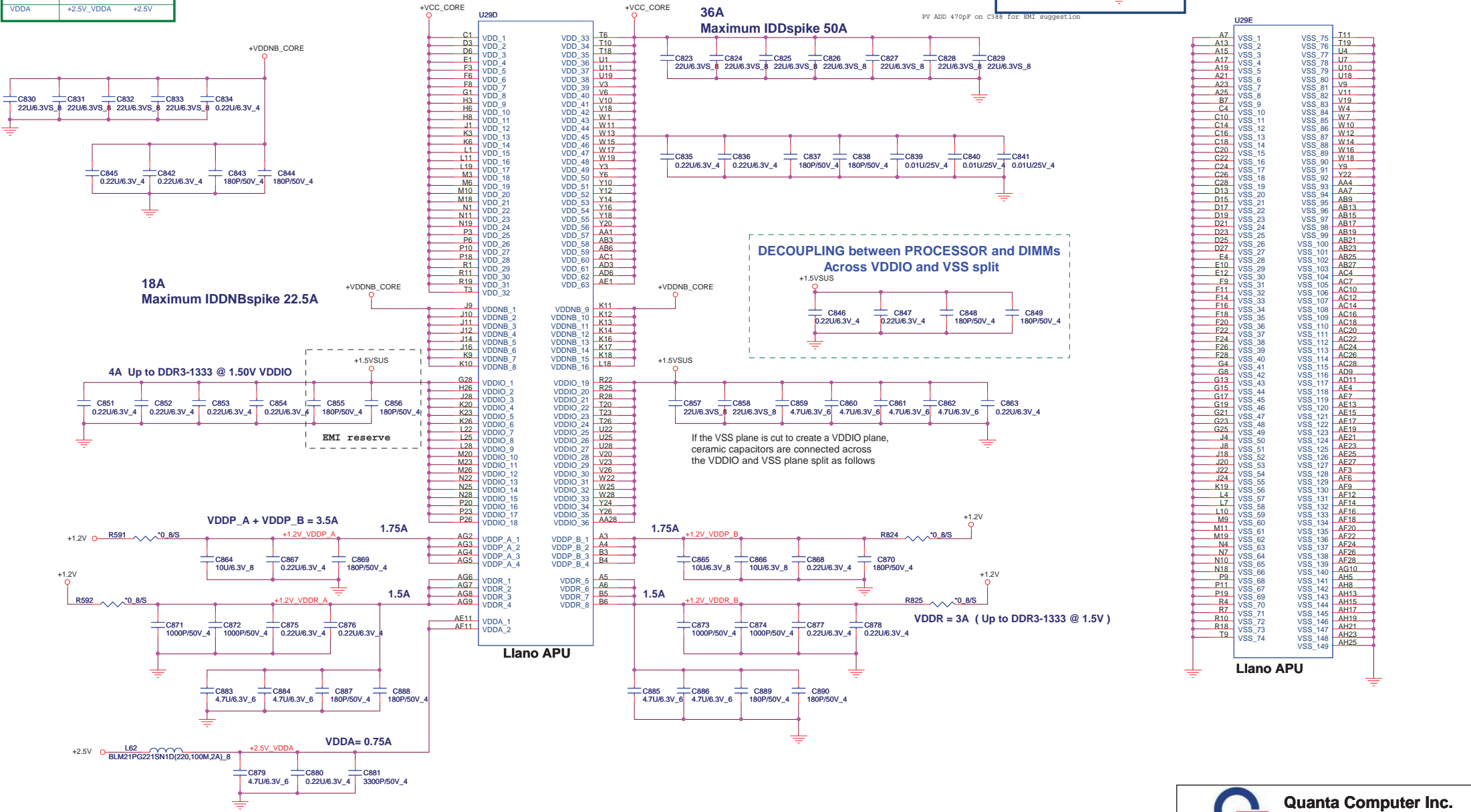
Size	Document Number	Rev
	Llano DDR3 MEM I/F	1A
Date:	Wednesday, May 04, 2011	Sheet 3 of 40

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



SI EMI

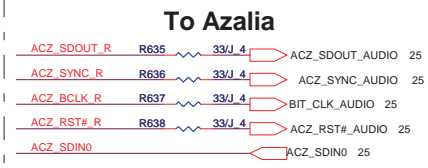
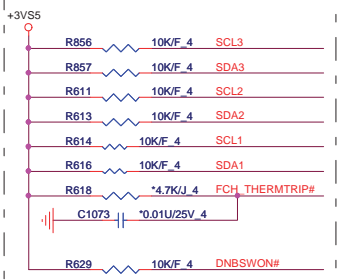
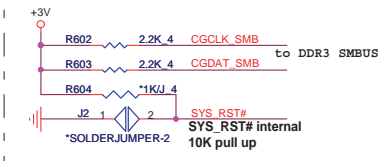
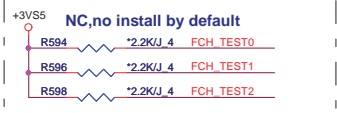


U29E

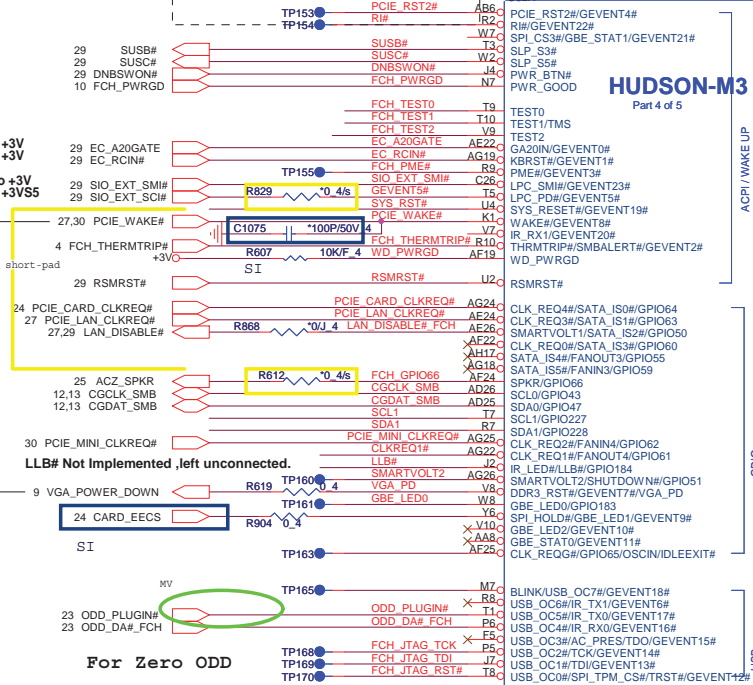
A7	VSS_1	VSS_75	T11
A13	VSS_2	VSS_76	T19
A15	VSS_3	VSS_77	U4
A17	VSS_4	VSS_78	U7
A19	VSS_5	VSS_79	U10
A21	VSS_6	VSS_80	U18
A23	VSS_7	VSS_81	V9
A25	VSS_8	VSS_82	V11
B7	VSS_9	VSS_83	V19
C4	VSS_10	VSS_84	W4
C10	VSS_11	VSS_85	W7
C14	VSS_12	VSS_86	W10
C16	VSS_13	VSS_87	W12
C18	VSS_14	VSS_88	W14
C20	VSS_15	VSS_89	W16
C22	VSS_16	VSS_90	W18
C24	VSS_17	VSS_91	Y9
C26	VSS_18	VSS_92	Y22
C28	VSS_19	VSS_93	AA4
C32	VSS_20	VSS_94	AA7
D15	VSS_21	VSS_95	AB9
D17	VSS_22	VSS_96	AB13
D19	VSS_23	VSS_97	AB15
D21	VSS_24	VSS_98	AB17
D23	VSS_25	VSS_99	AB19
D25	VSS_26	VSS_100	AB21
D27	VSS_27	VSS_101	AB23
E4	VSS_28	VSS_102	AB25
E10	VSS_29	VSS_103	AB27
E12	VSS_30	VSS_104	AC4
F9	VSS_31	VSS_105	AC7
F11	VSS_32	VSS_106	AC10
F14	VSS_33	VSS_107	AC12
F16	VSS_34	VSS_108	AC14
F18	VSS_35	VSS_109	AC16
F20	VSS_36	VSS_110	AC18
F22	VSS_37	VSS_111	AC20
F24	VSS_38	VSS_112	AC22
F26	VSS_39	VSS_113	AC24
F28	VSS_40	VSS_114	AC26
G4	VSS_41	VSS_115	AC28
G8	VSS_42	VSS_116	AD9
G13	VSS_43	VSS_117	AD11
G15	VSS_44	VSS_118	AE4
G17	VSS_45	VSS_119	AE7
G21	VSS_46	VSS_120	AE15
G23	VSS_47	VSS_121	AE17
G25	VSS_48	VSS_122	AE19
J4	VSS_49	VSS_123	AE21
J8	VSS_50	VSS_124	AE23
J18	VSS_51	VSS_125	AE25
J20	VSS_52	VSS_126	AE27
J22	VSS_53	VSS_127	AE29
J24	VSS_54	VSS_128	AF3
K19	VSS_55	VSS_129	AF6
L4	VSS_56	VSS_130	AF9
L7	VSS_57	VSS_131	AF12
L10	VSS_58	VSS_132	AF14
M3	VSS_59	VSS_133	AF16
M11	VSS_60	VSS_134	AF18
M19	VSS_61	VSS_135	AF20
N4	VSS_62	VSS_136	AF22
N7	VSS_63	VSS_137	AF24
N10	VSS_64	VSS_138	AF26
N18	VSS_65	VSS_139	AF28
P9	VSS_66	VSS_140	AG10
P11	VSS_67	VSS_141	AH5
P19	VSS_68	VSS_142	AH8
R4	VSS_69	VSS_143	AH13
R7	VSS_70	VSS_144	AH15
R10	VSS_71	VSS_145	AH17
R18	VSS_72	VSS_146	AH19
T9	VSS_73	VSS_147	AH21
	VSS_74	VSS_148	AH23
		VSS_149	AH25

Quanta Computer Inc.
PROJECT : R23

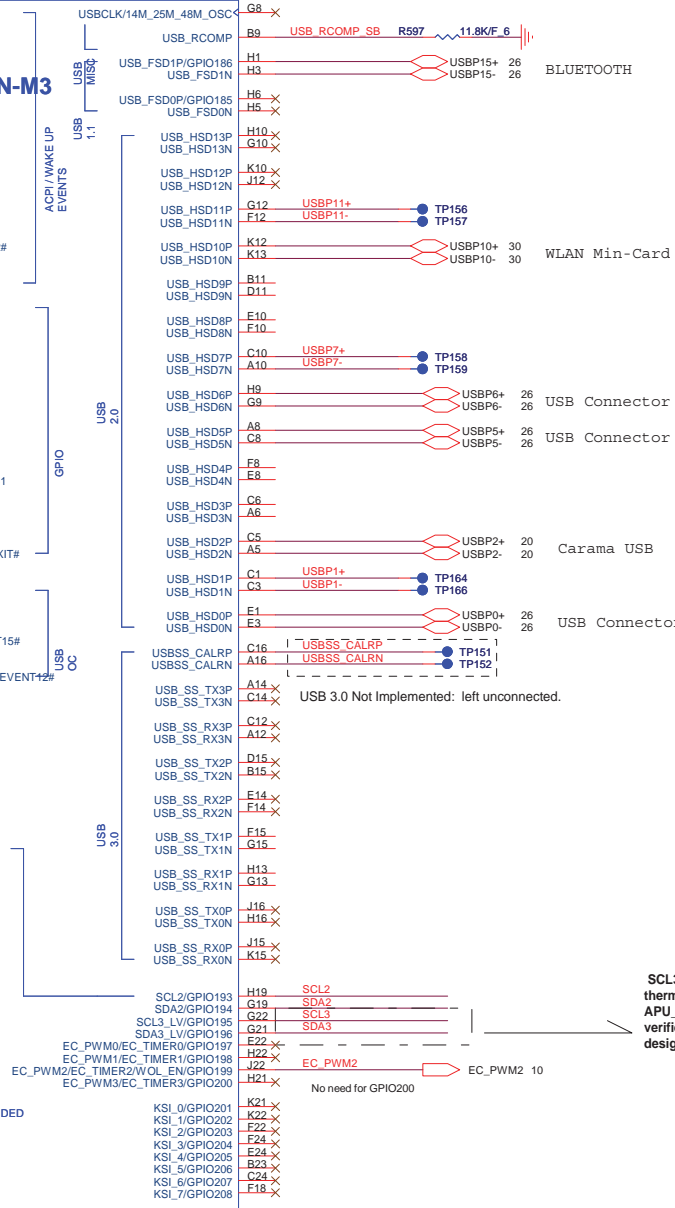
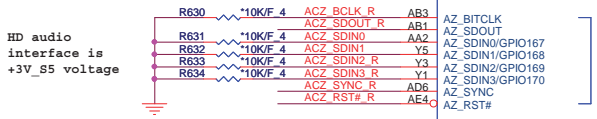
Size: Document Number: Liano POWER/GND Rev: 1A
Date: Wednesday, May 04, 2011 Sheet: 5 of 40



remove PCIE_RST2# from AMD recommend



For Zero ODD

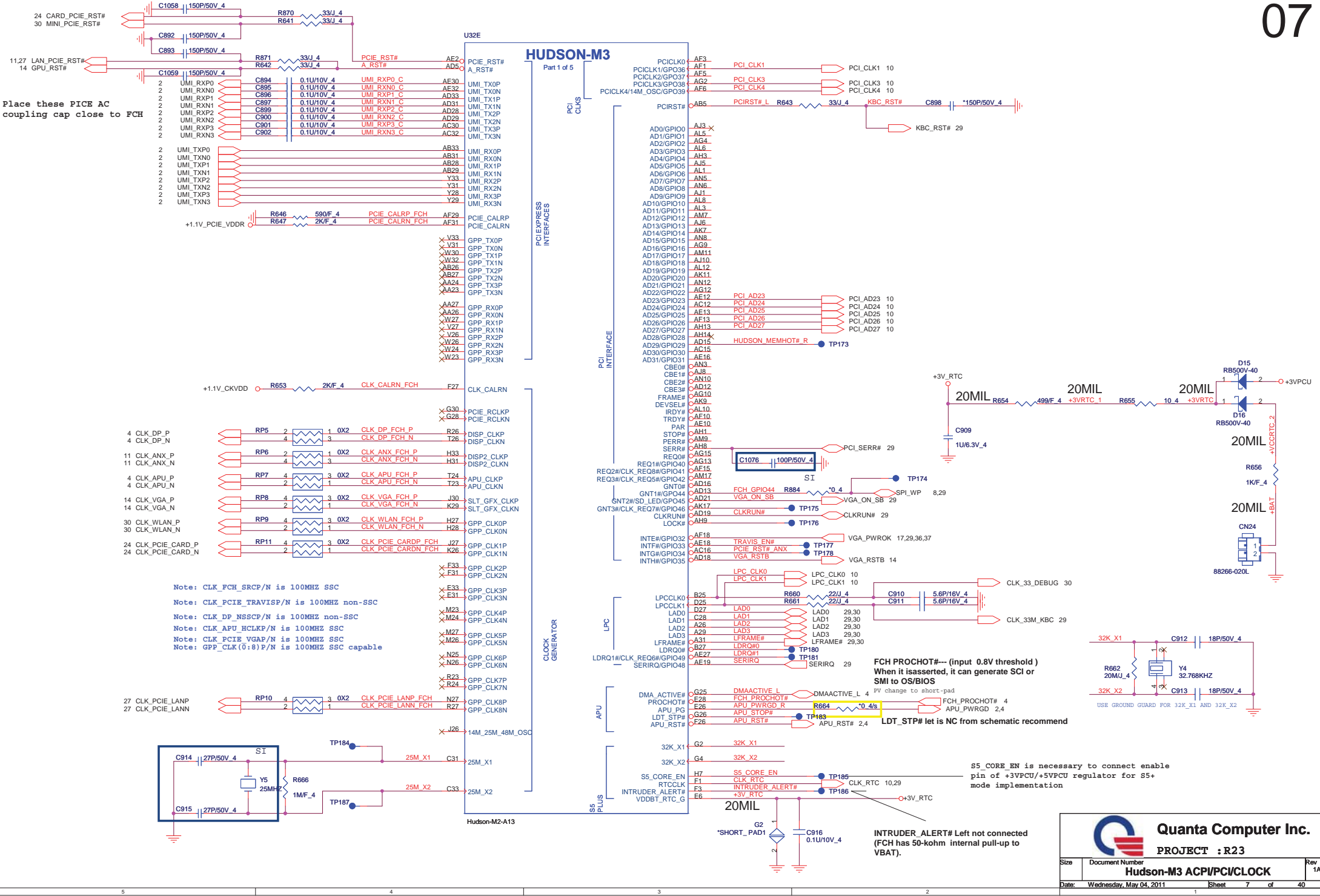


SCL3 of a TSI-capable APU's thermal bus, Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

Hudson-M2-A13

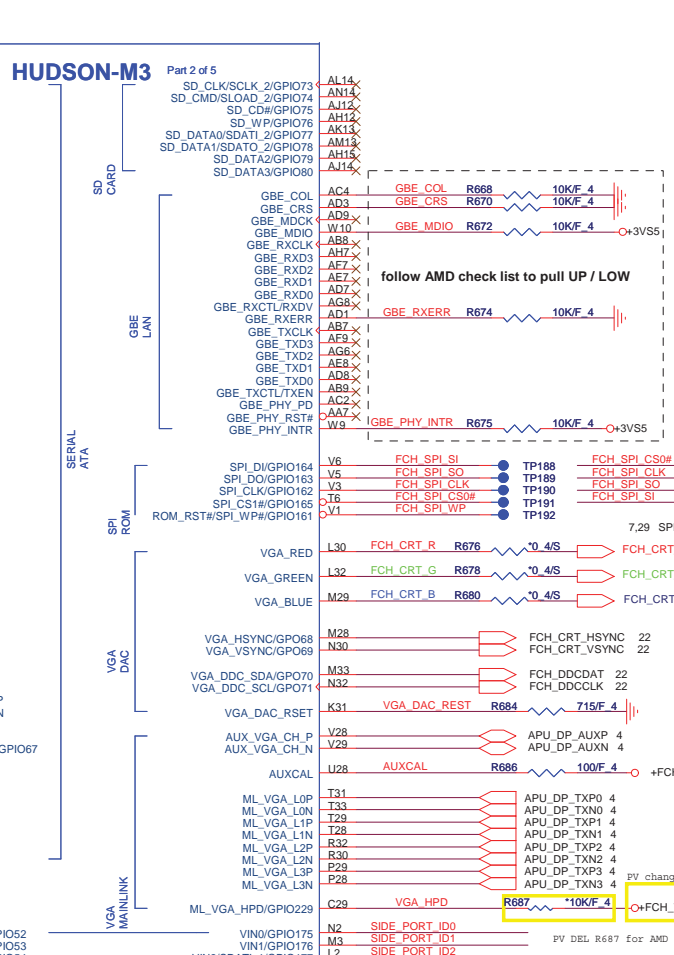
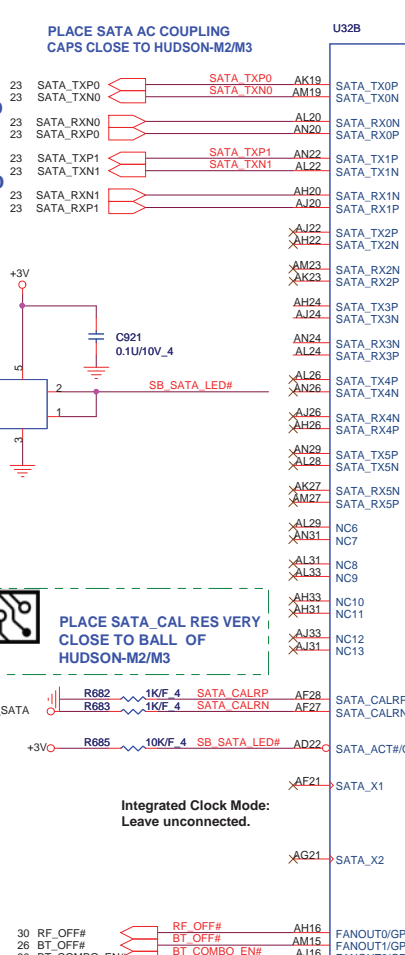
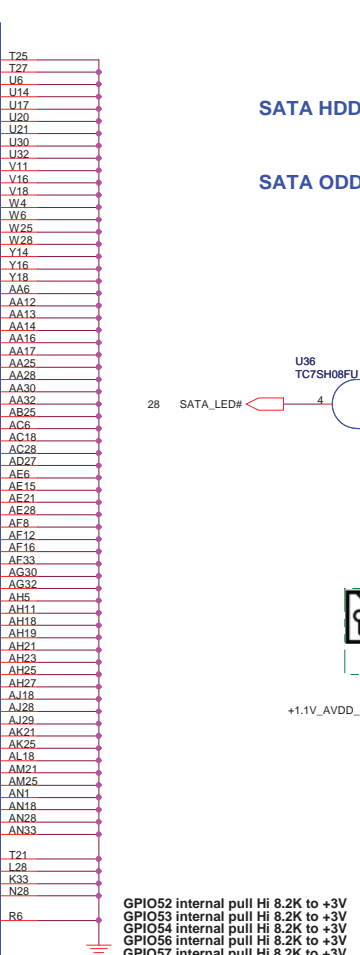
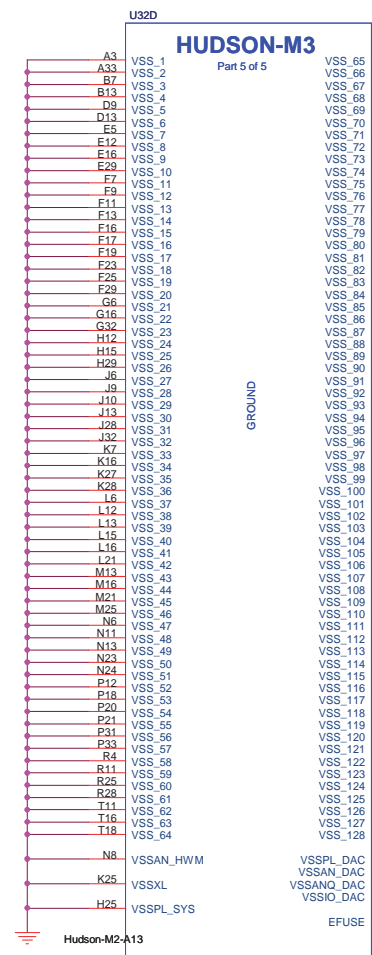
Quanta Computer Inc.
PROJECT : R23

Size	Document Number	Hudson-M3 GPIO/USB/AZ/RGMII	Rev	1A
Date:	Wednesday, May 04, 2011	Sheet	6	of 40

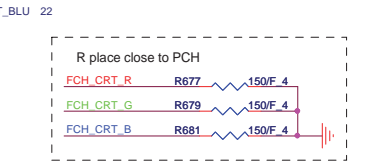
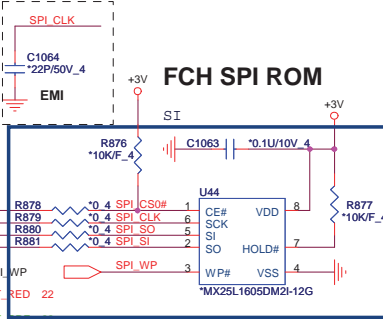


Quanta Computer Inc.
PROJECT : R23

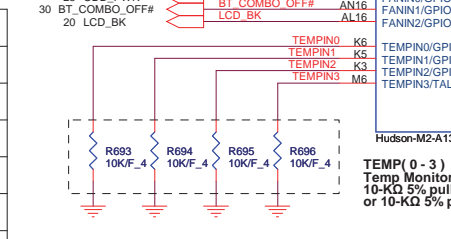
Size	Document Number	Rev
	Hudson-M3 ACP/PCI/CLOCK	1A
Date:	Wednesday, May 04, 2011	Sheet 7 of 40



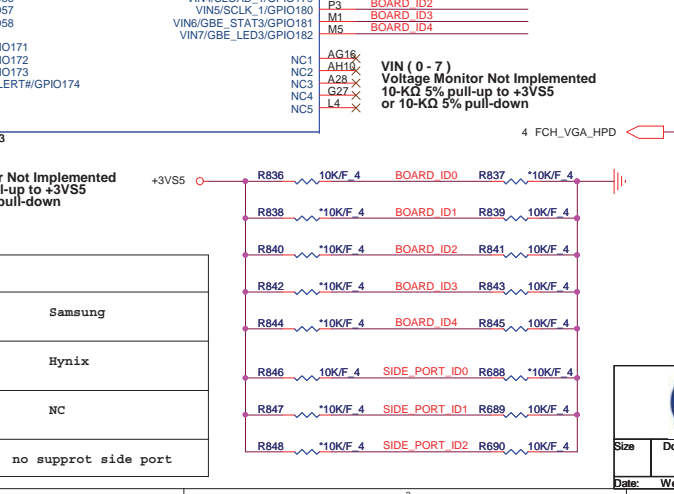
Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023



ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12



SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

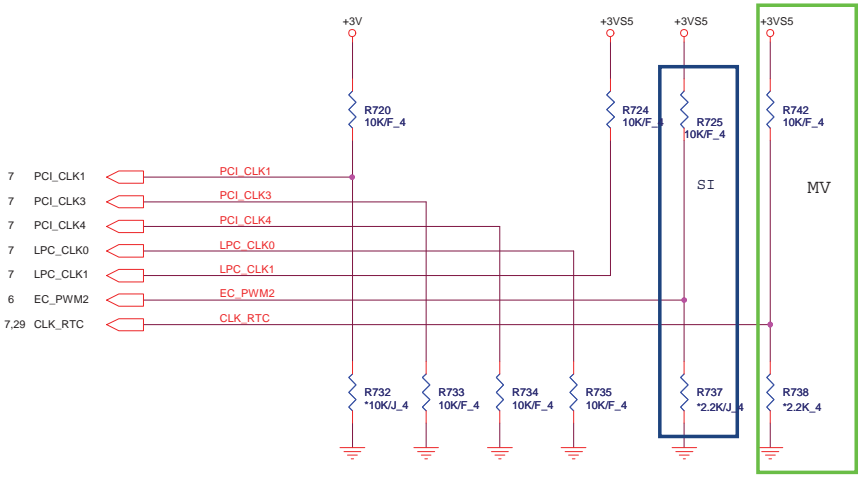


Quanta Computer Inc.
PROJECT : R23

Size Document Number Hudson-M3 SATA/HWM/SPI Rev 1A
Date: Wednesday, May 04, 2011 Sheet 8 of 40

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIe Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIe Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

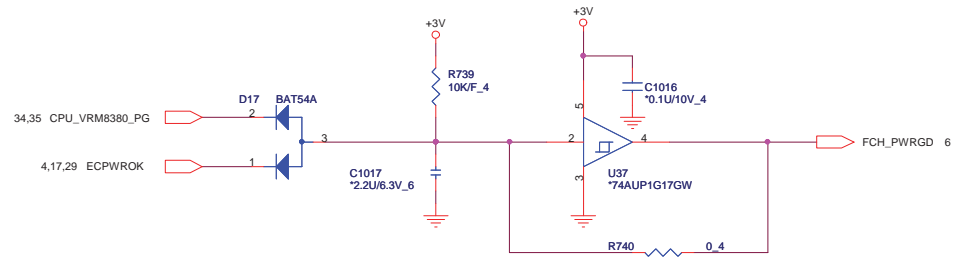
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

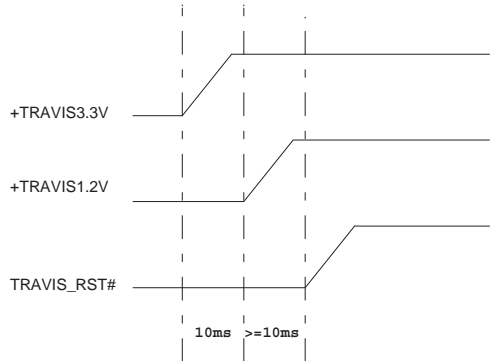


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

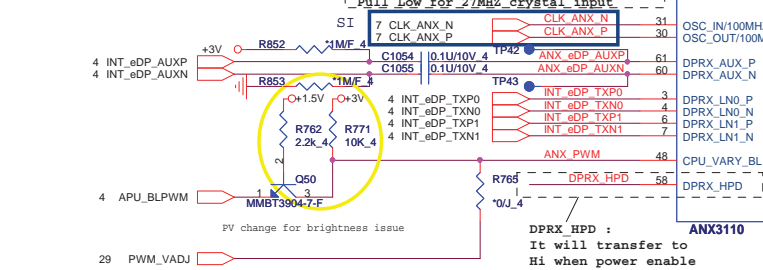
FCH_PWRGD



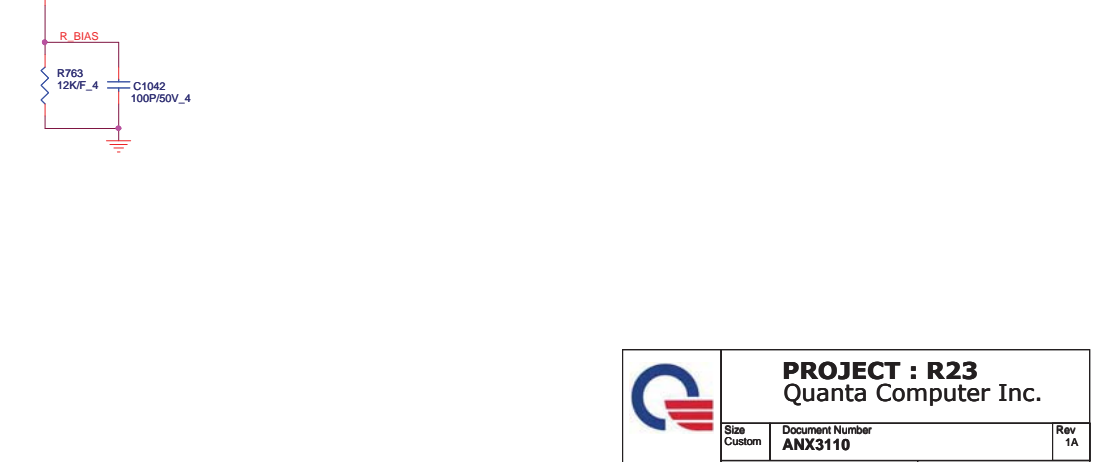
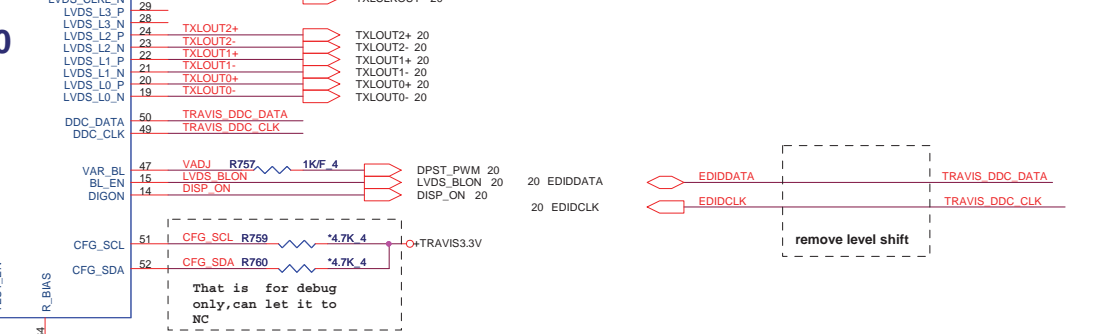
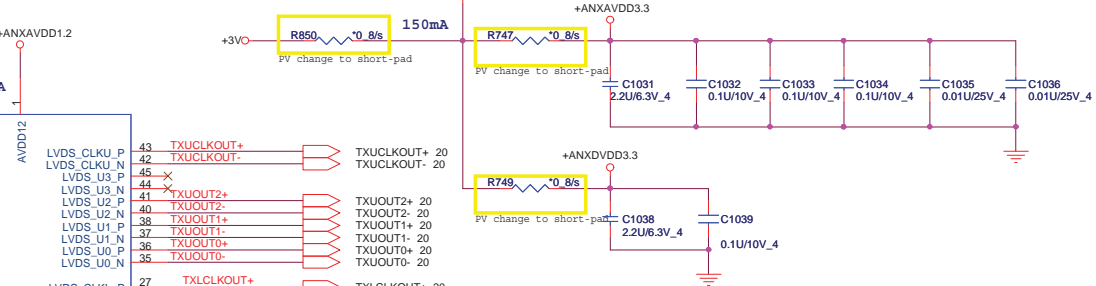
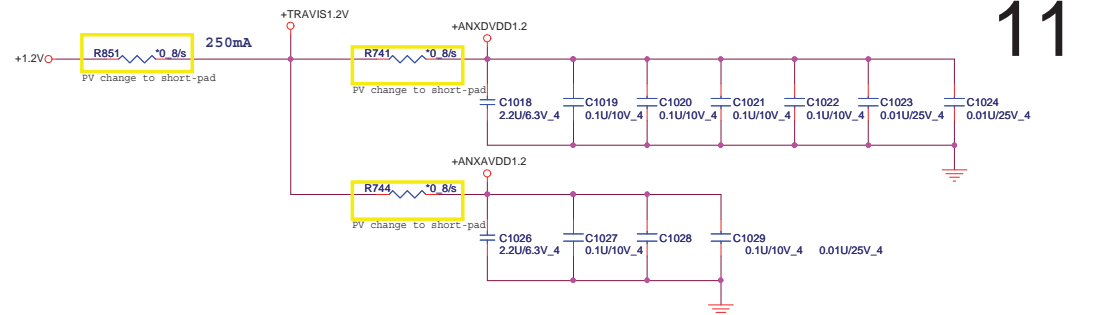
ANX3110 Power Up Sequence



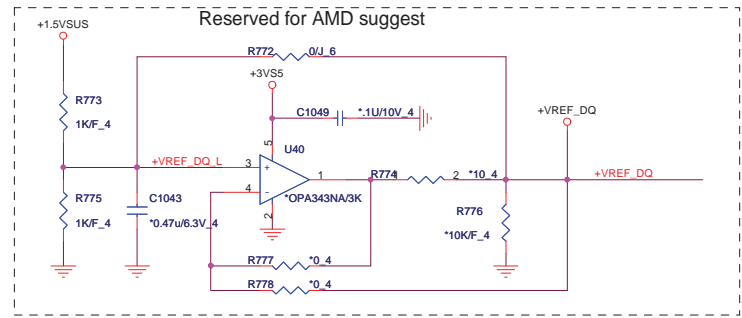
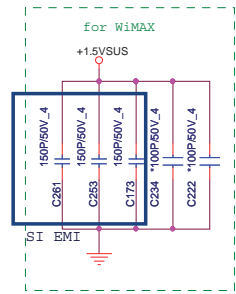
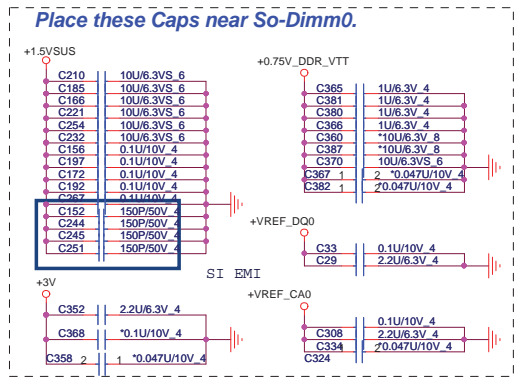
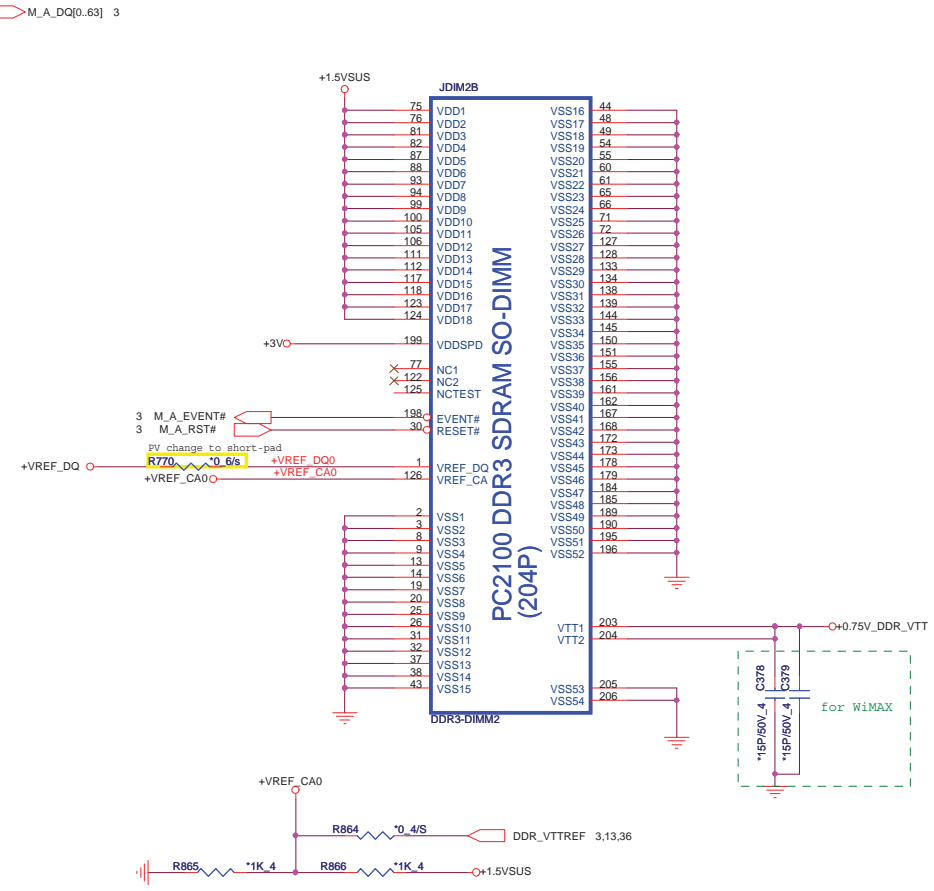
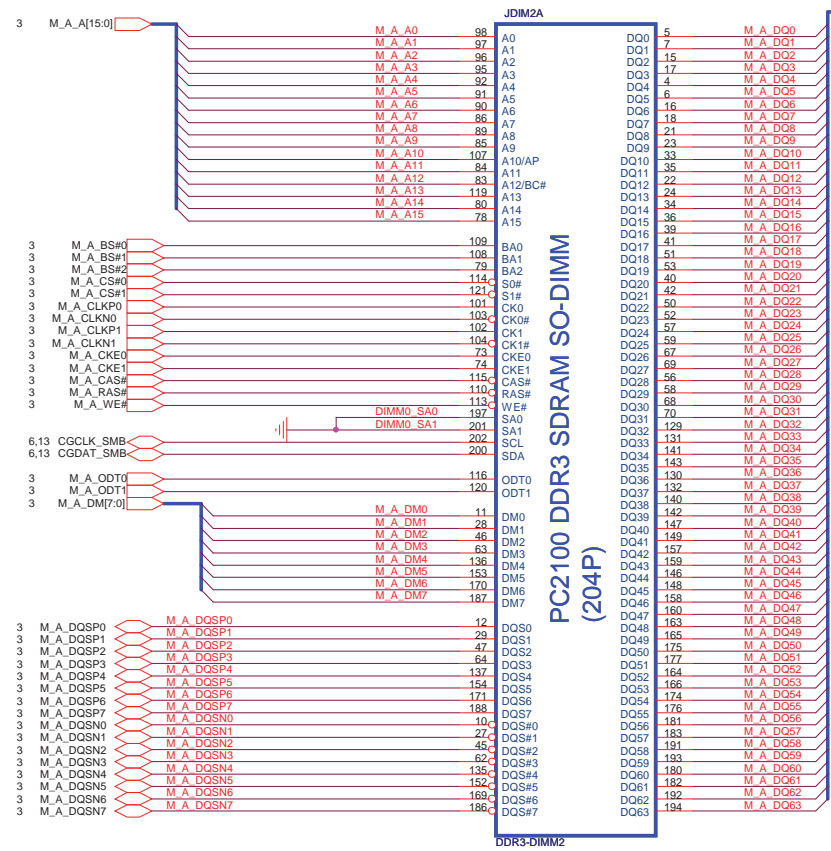
GPIO 0 : Define VAR_BL & BL_EN & DIGON H/W or S/W control power up timing
 Pull Hi for H/W mode
 ---chip have defined power up timing
 Pull Low for S/W mode -- APU through DPRX port to program it



ANALOGIX ANX3110



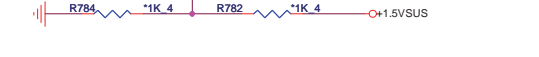
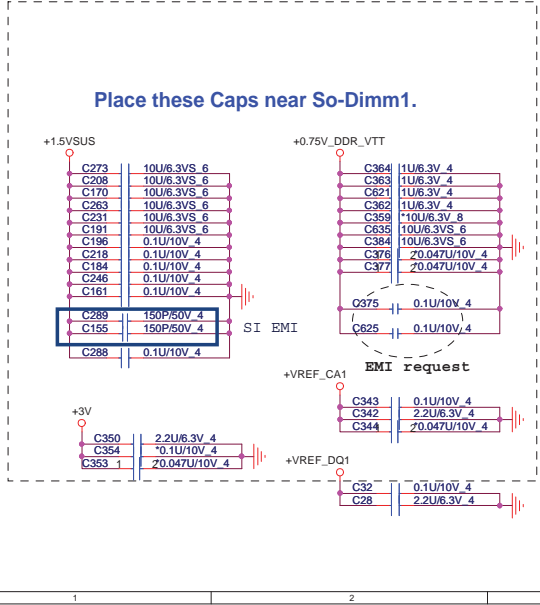
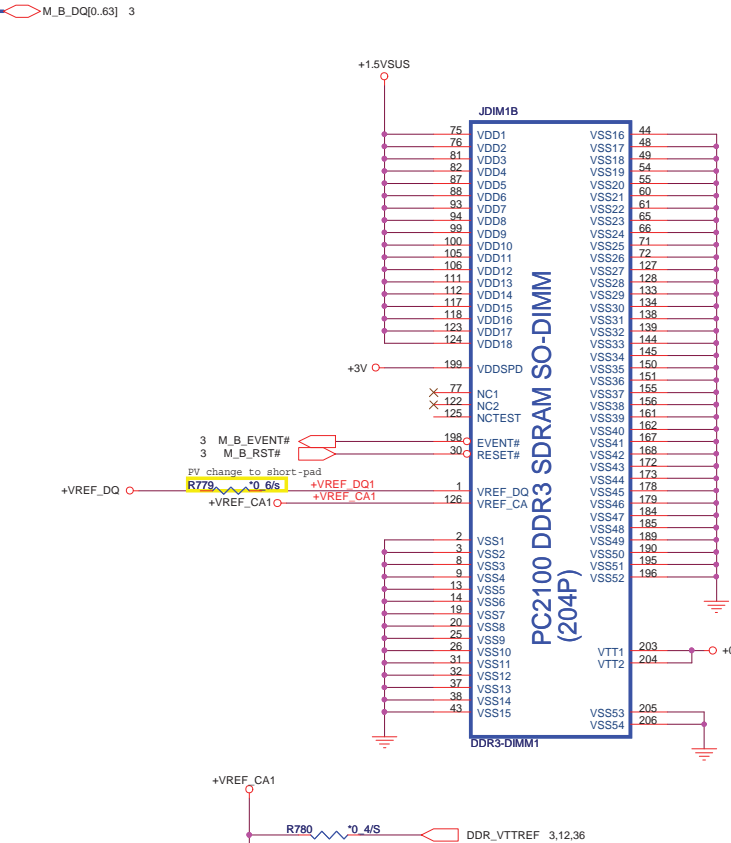
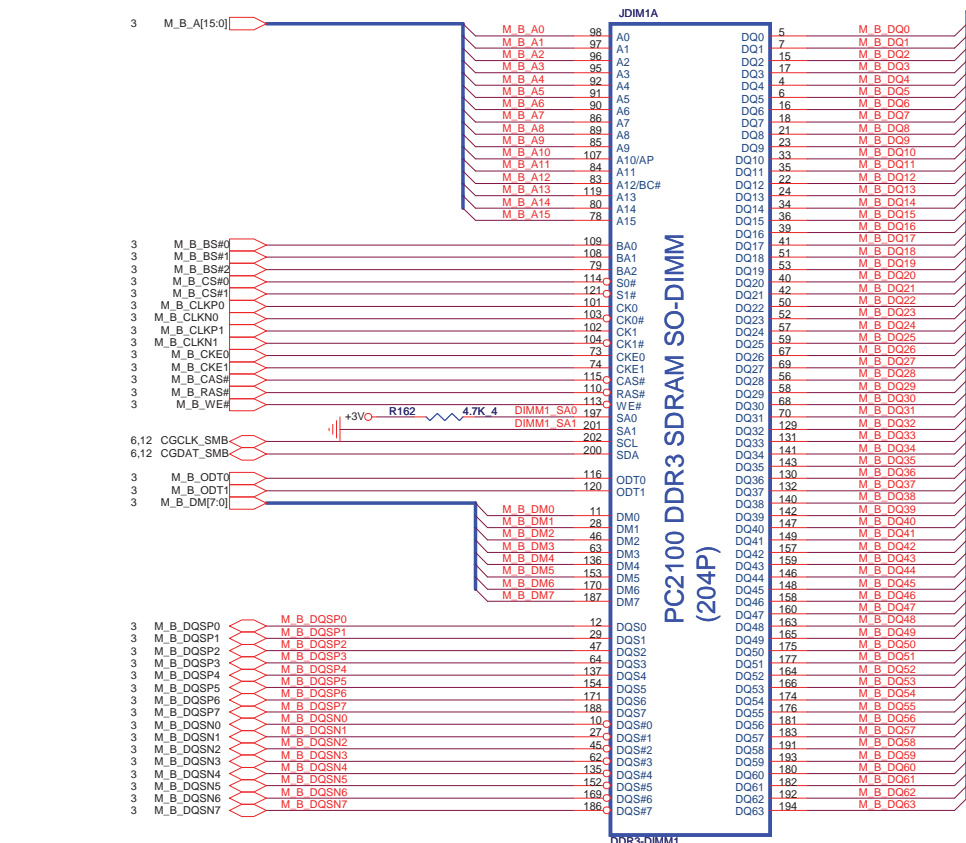
PROJECT : R23 Quanta Computer Inc.		
Size Custom	Document Number ANX3110	Rev 1A
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13.36 +0.75V_DDR_VTT
 2.3,4,5,13,36,37,39 +1.5VSUS
 2,4,6,8,9,10,11,13,14,17,20,22,23,24,25,27,28,29,30,34,37,39 +3V

PROJECT : R23
 Quanta Computer Inc.

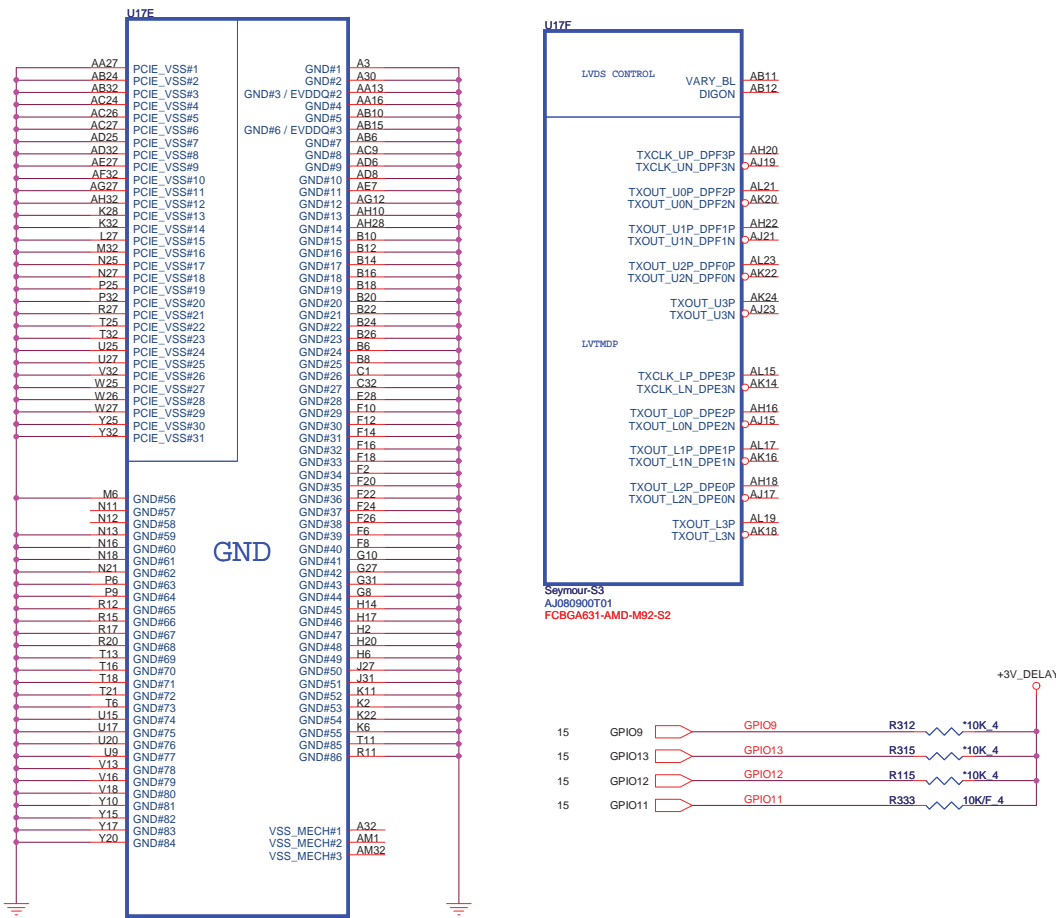
Size Custom	Document Number DDR3 DIMM-0	Rev 1A
Date: Tuesday, May 03, 2011		Sheet 12 of 40



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Quanta Computer Inc.

Size Custom Document Number **DDR3 DIMM-1** Rev 1A

Date: Tuesday, May 03, 2011 Sheet 13 of 40



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

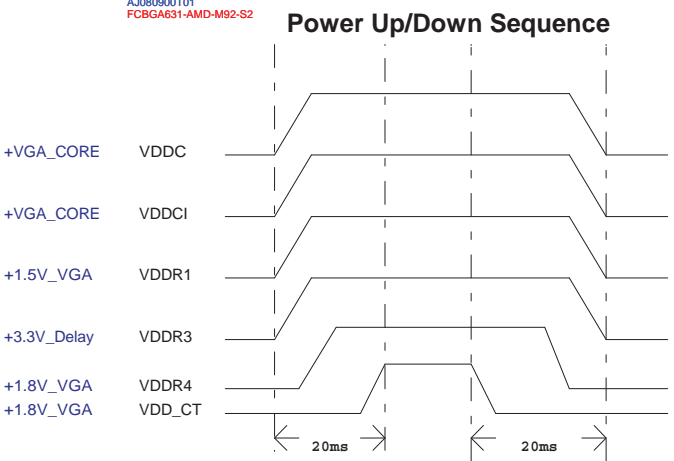
RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

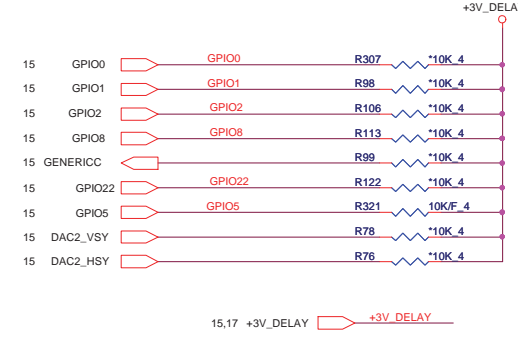
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

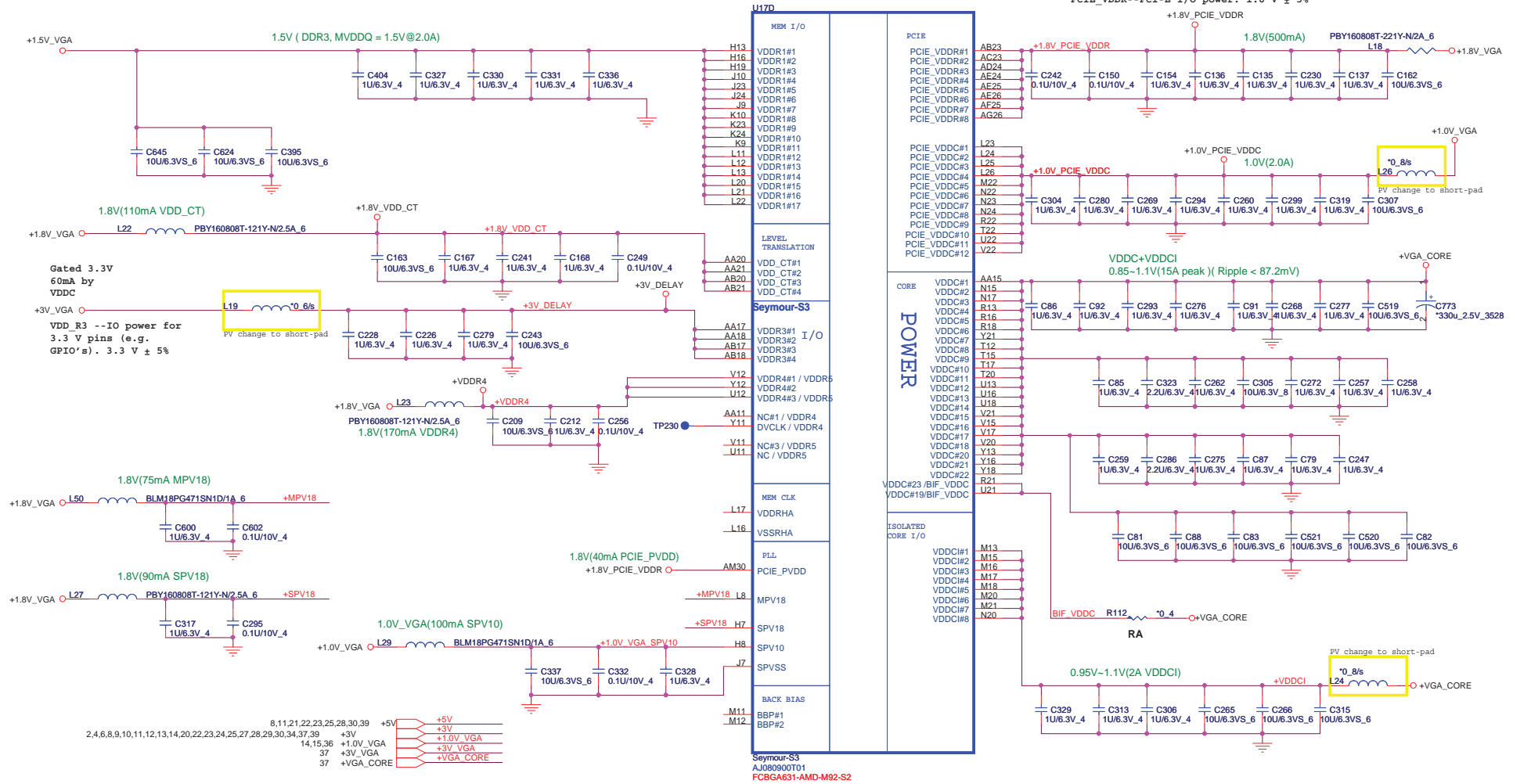
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



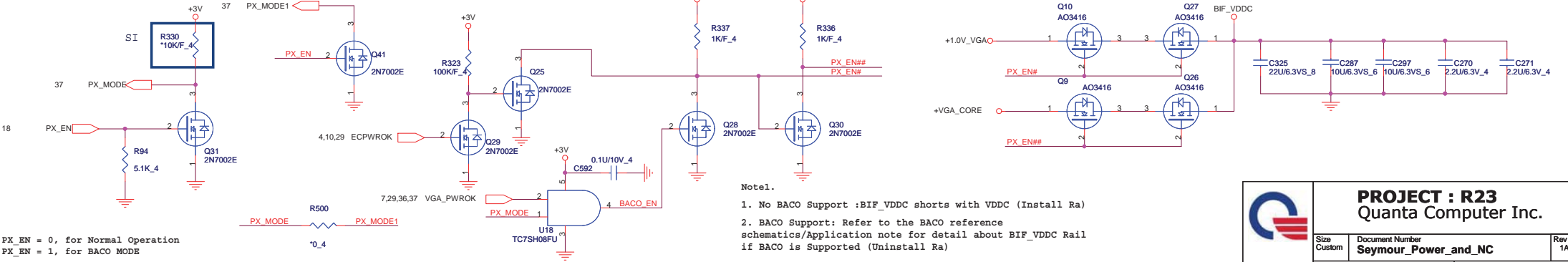
PROJECT : R23
Quanta Computer Inc.

Size Custom	Document Number Seymour GND / LVDS/ Straps	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 16	of 40

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



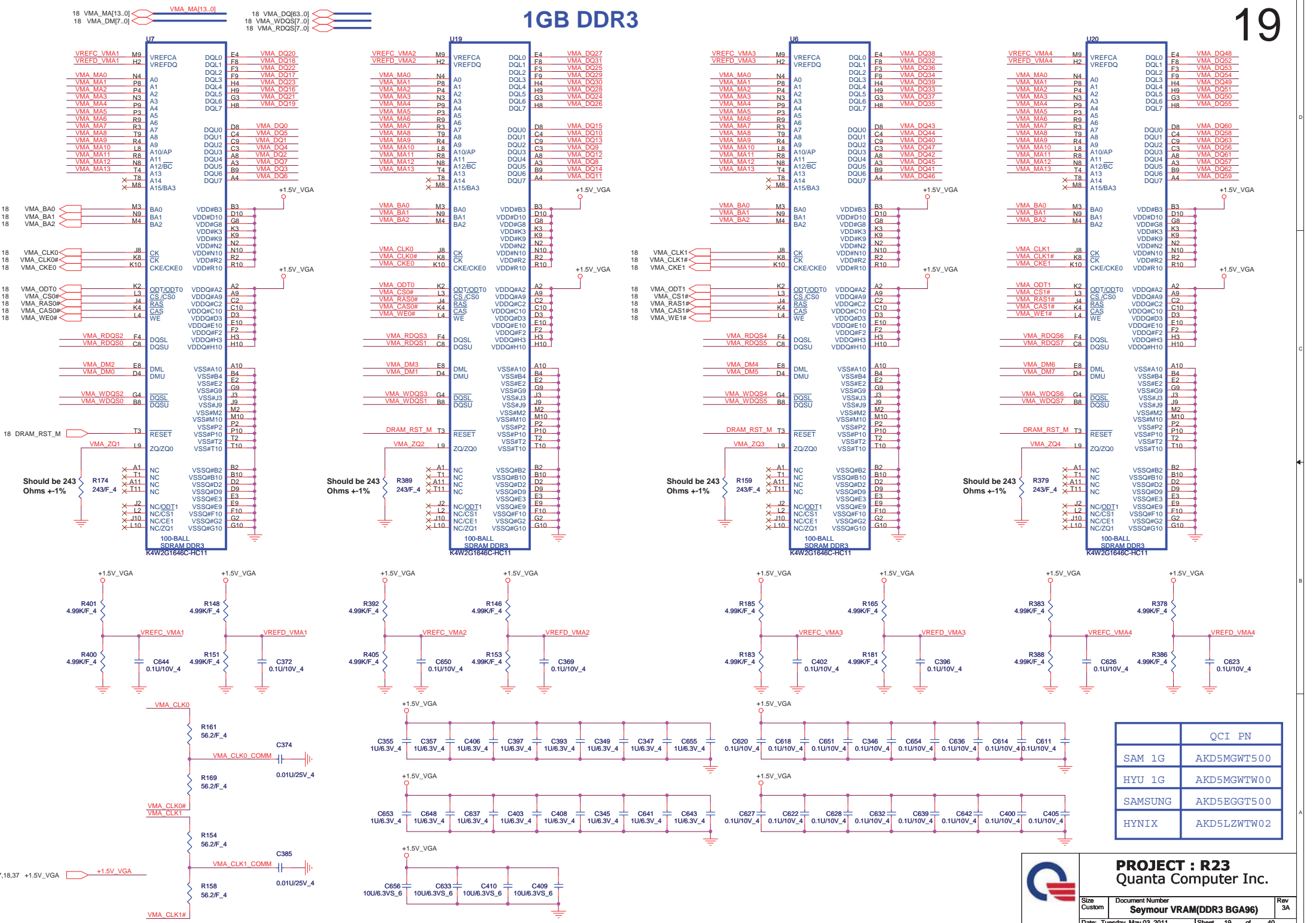
Support BACO Mode



PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour_Power_and_NC	1A
Date: Tuesday, May 03, 2011	Sheet 17 of 40	

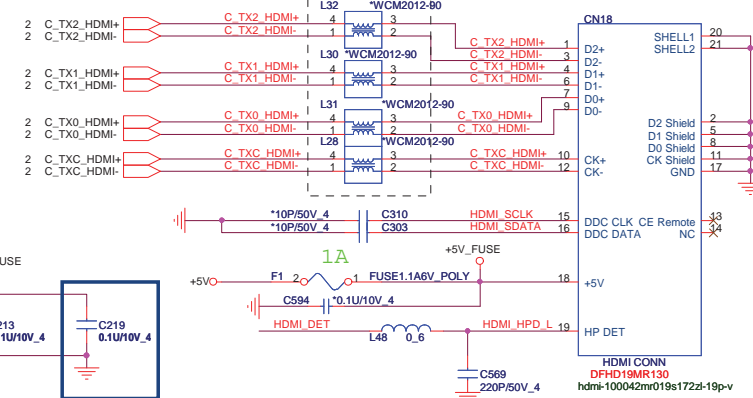
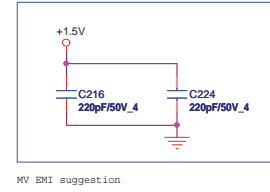
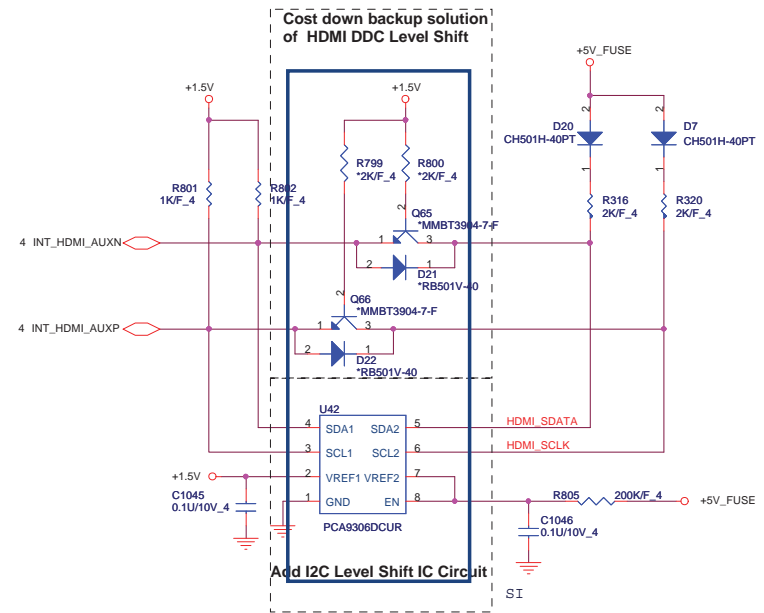
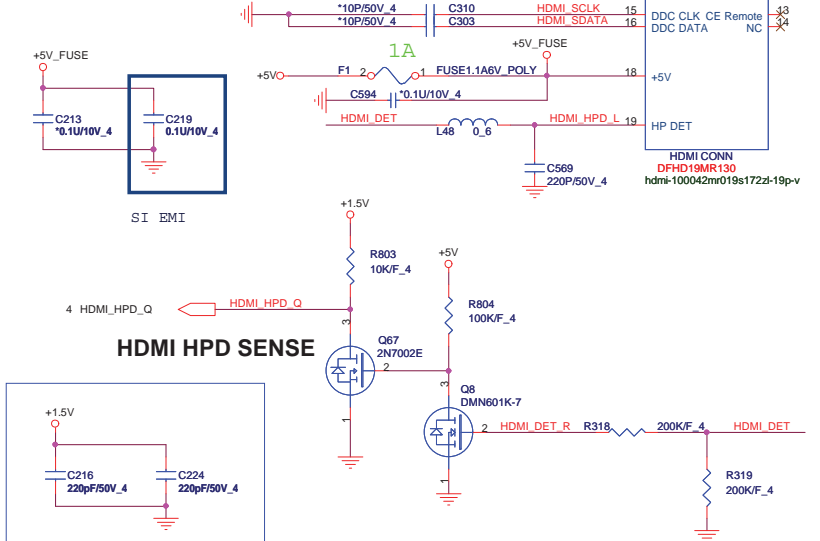
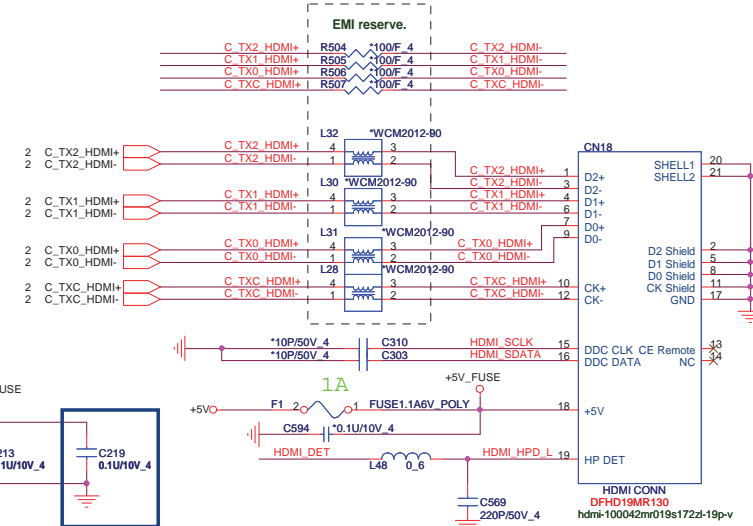
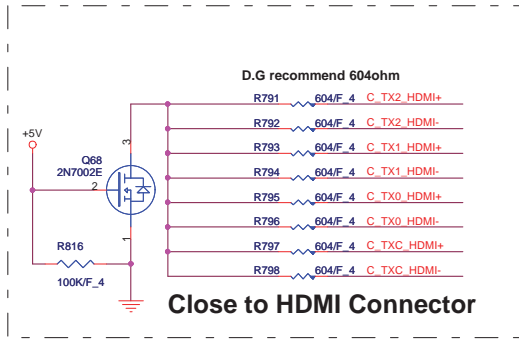
1GB DDR3



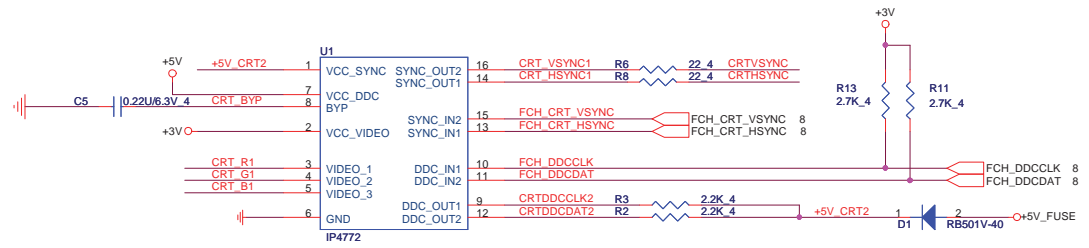
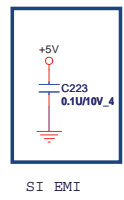
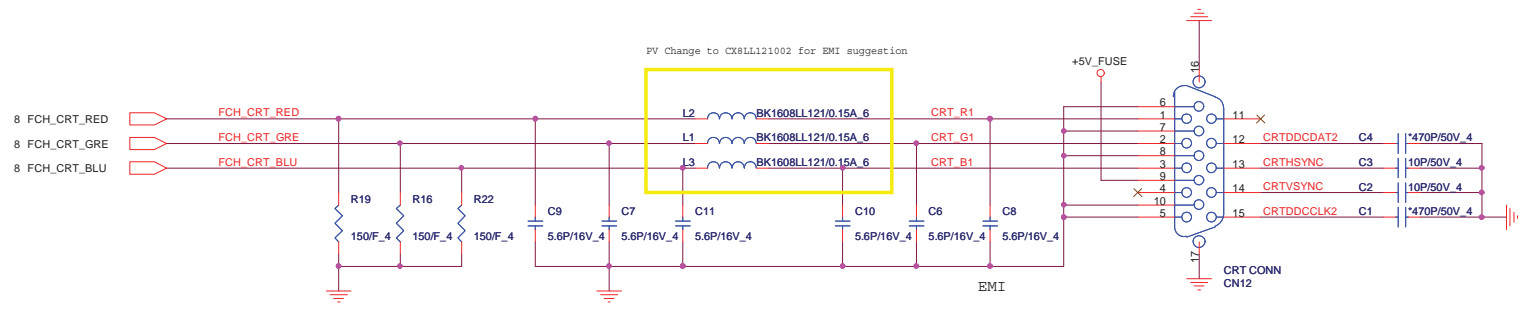
QCI PN	
SAM 1G	AKD5MGWT500
HYU 1G	AKD5MGWTW00
SAMSUNG	AKD5EGGT500
HYNIX	AKD5LZTWT02

PROJECT : R23
Quanta Computer Inc.

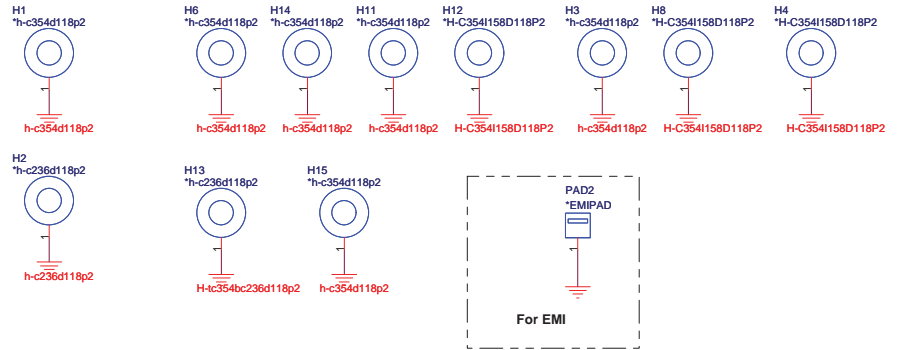
Size Custom	Document Number	Rev 3A
	Seymour VRAM(DDR3 BGA96)	
Date: Tuesday, May 03, 2011	Sheet 19 of 40	



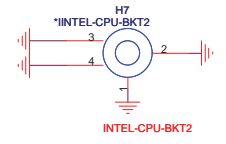
CRT PORT



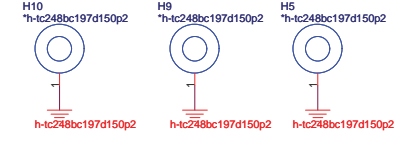
HOLE



CPU

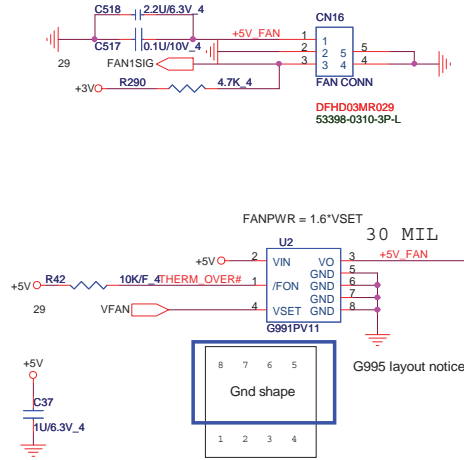


VGA

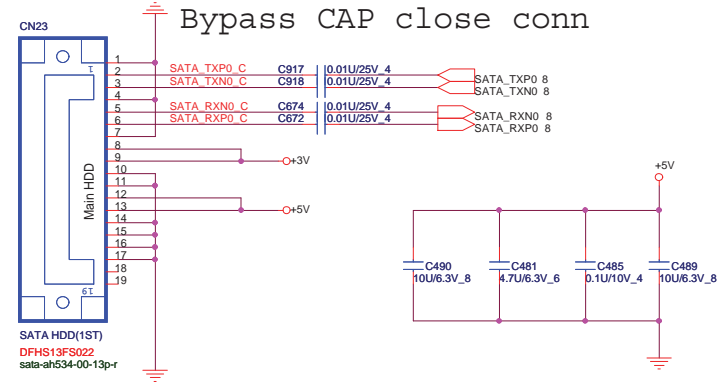


	PROJECT : R23		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number CRT,Hole	
Date: Tuesday, May 03, 2011		Sheet 22 of 40	

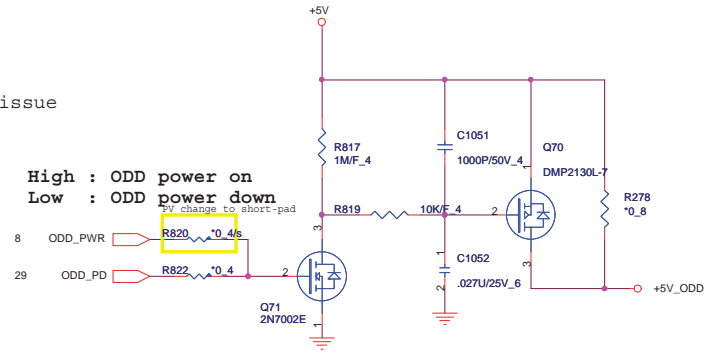
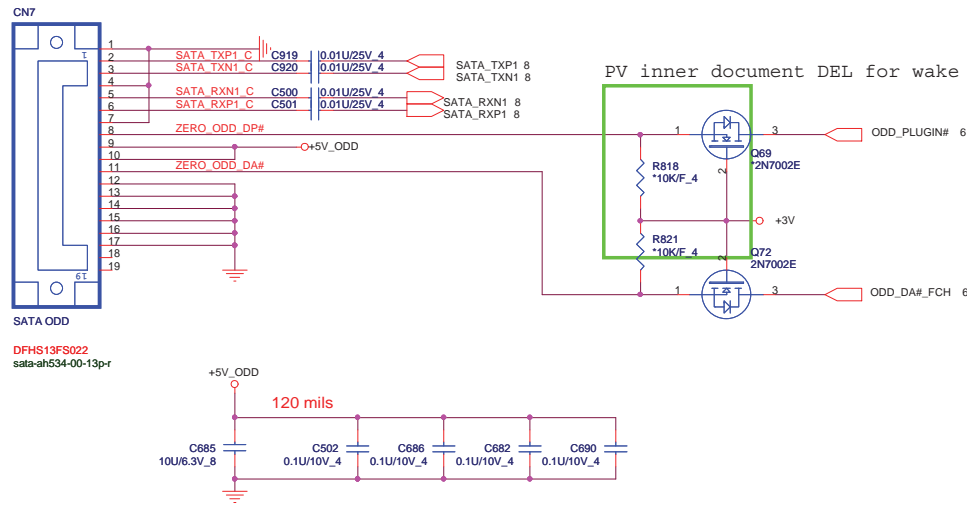
CPU FAN

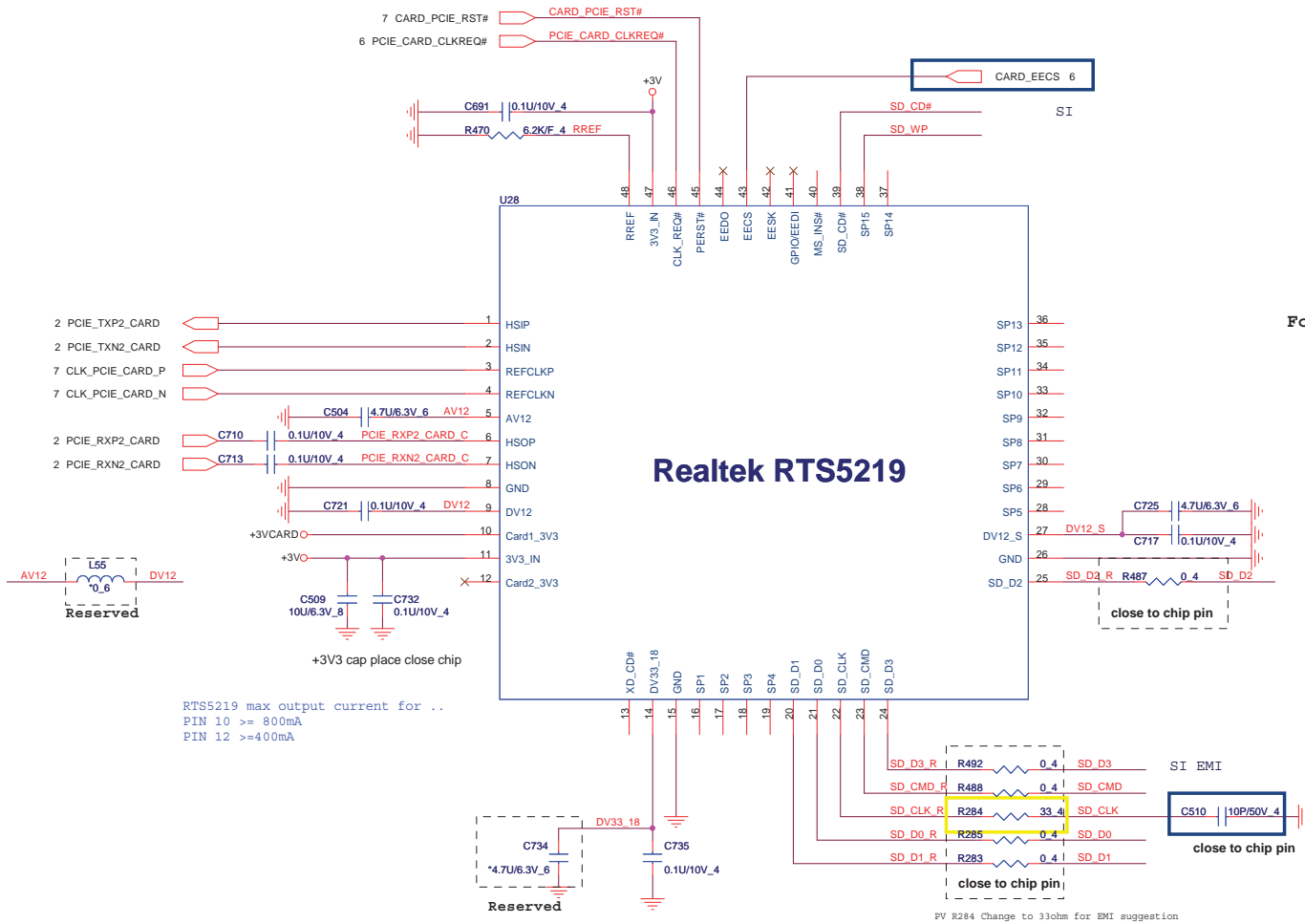


SATA HDD CONNECTOR

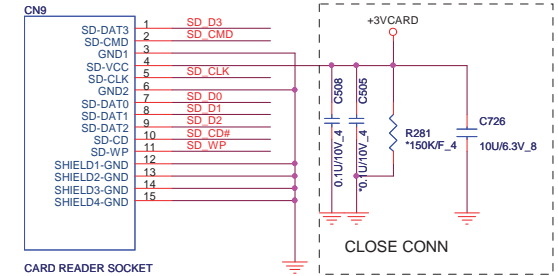


SATA ODD CONNECTOR SATA ODD






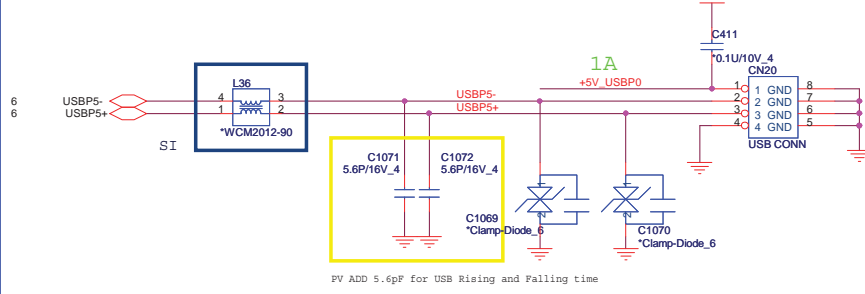
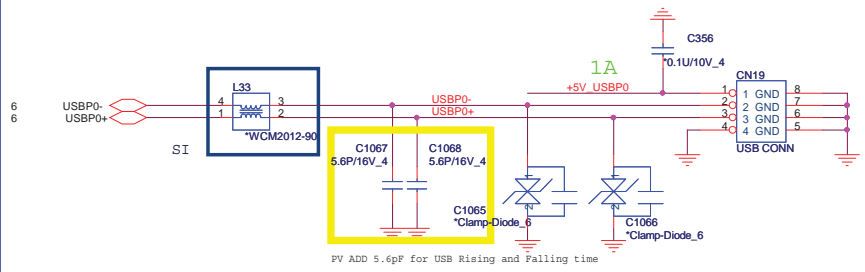
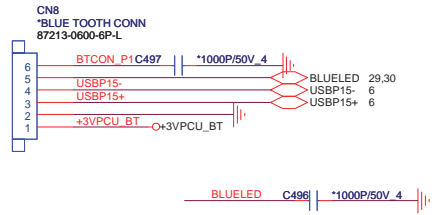
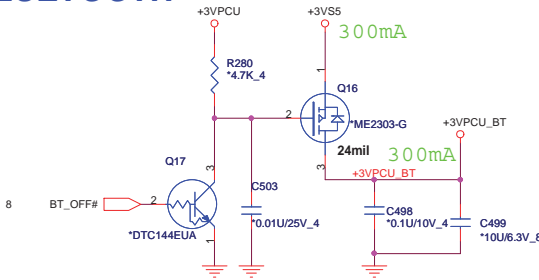
Footprint lqfp48-9x9-5-1_6h



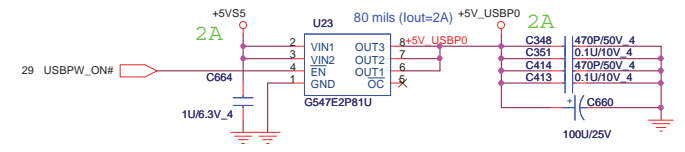
PV R284 Change to 33ohm for EMI suggestion

 PROJECT : R23 Quanta Computer Inc.			Size	Document Number	Rev
			Custom	RTS5219 & CR SOCKET & HOLE	1A
Date: Tuesday, May 03, 2011			Sheet	24	of 40

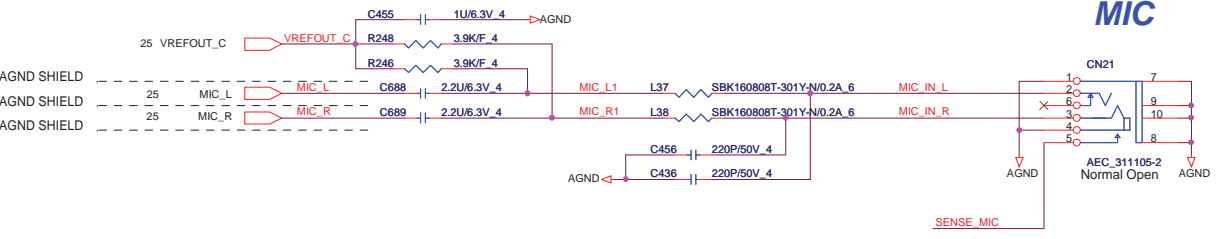
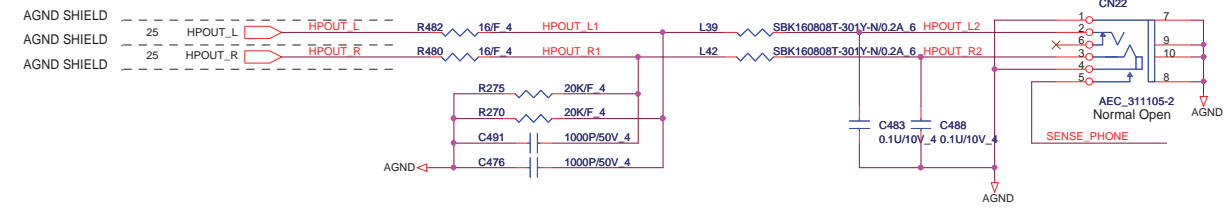
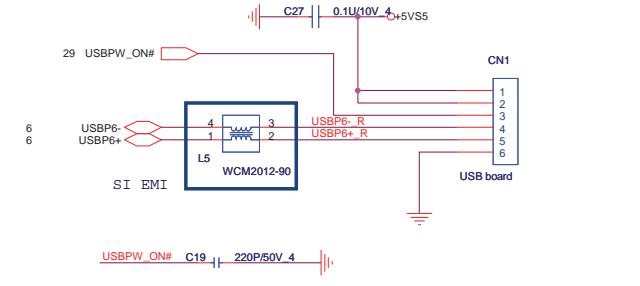
BLUETOOTH



LEFT SIDE USB2



Right SIDE USB1

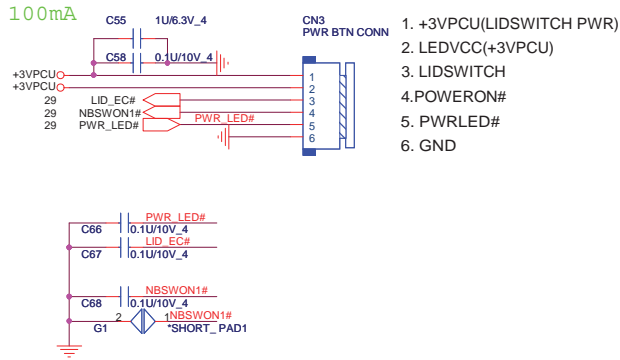


Line out

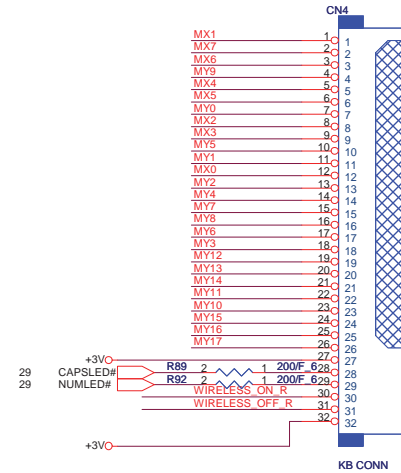
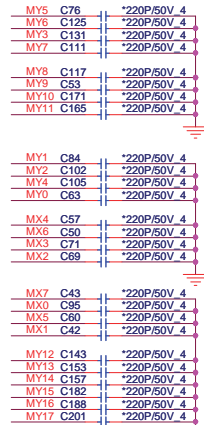
MIC

PROJECT : R23 Quanta Computer Inc.		
Size Custom	Document Number USB/BT/Audio Jack	Rev 1A
Date: Tuesday, May 03, 2011		Sheet 26 of 40

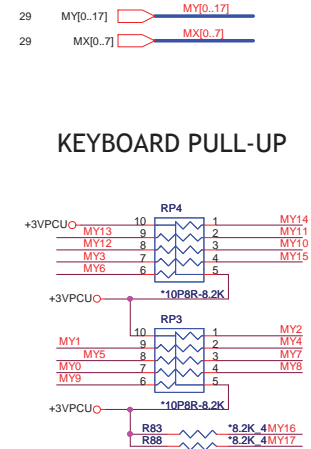
POWER BOTTON CONNECT



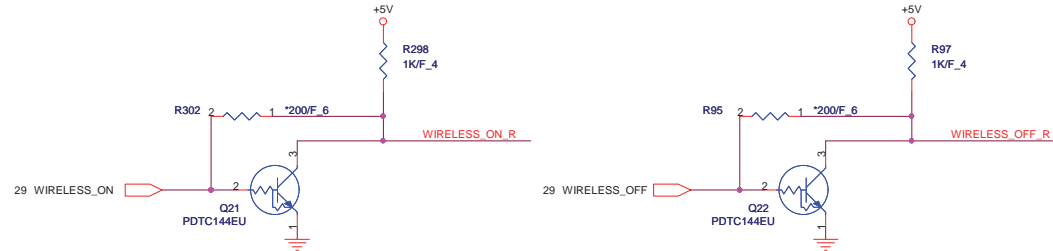
KEYBOARD Con.



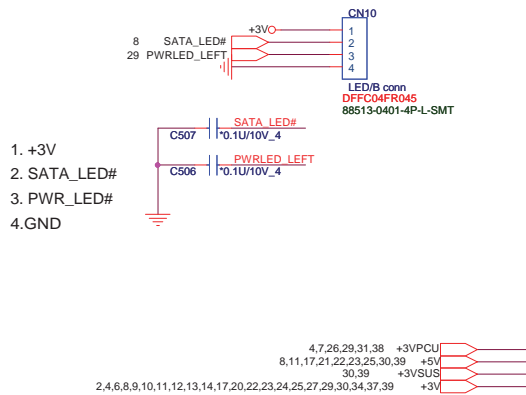
KEYBOARD PULL-UP



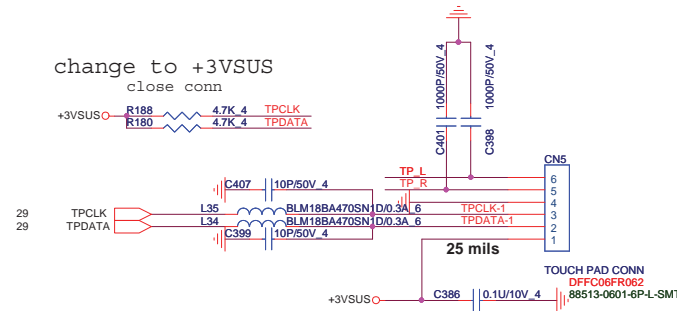
EC KB3930 has included K/B pull-up resistor and function



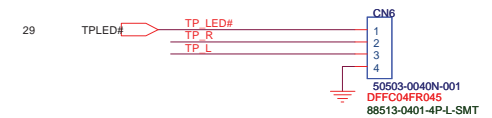
LED Con.



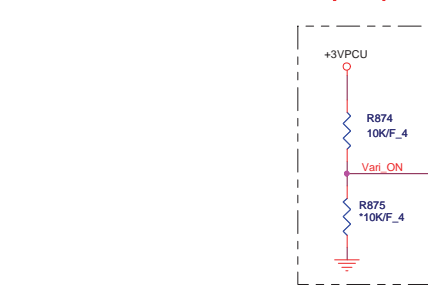
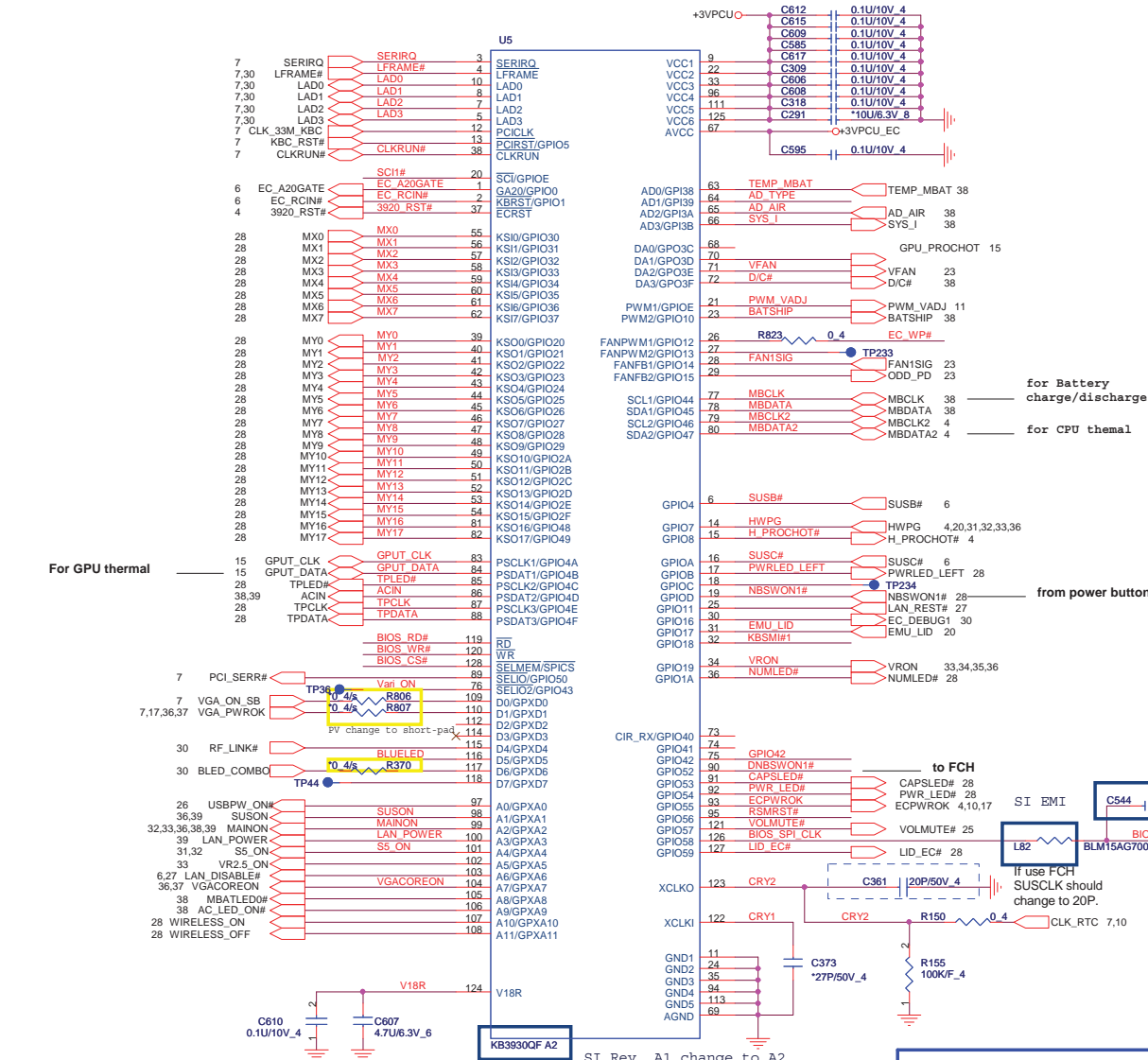
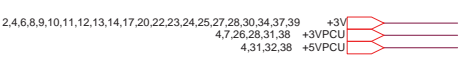
TOUCH PAD Con.



To TOUCH PAD SW board

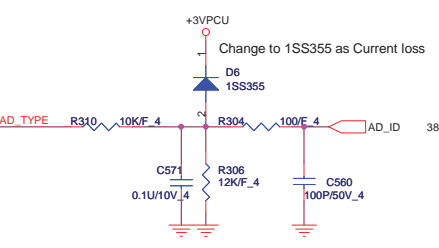


		PROJECT : R23 Quanta Computer Inc.	
Size Custom	Document Number LED/KB/SW/TP	Rev 1A	
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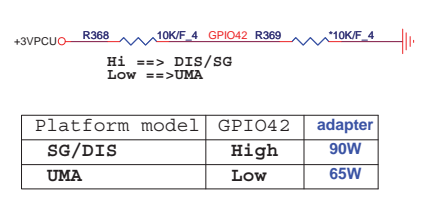


CPU Thermal SMBUS select	Vari_ON	project
SCL1/SDA1	Low	R22
SCL2/SDA2	High	R23,R24

Smart adapter Type check



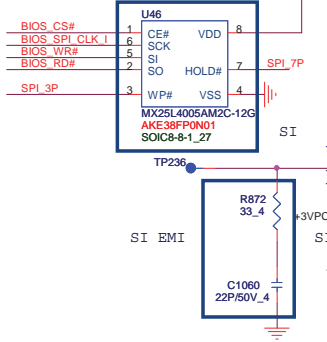
Adapter select



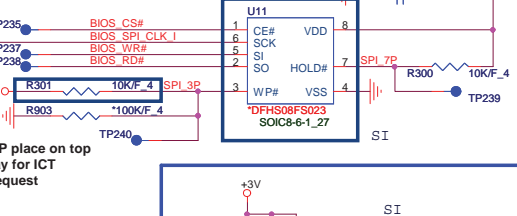
Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

Vender	Size	P/N
AMIC	128K	AKE35ZN0801
EON	128K	AKE35FN0Q00
Socket		DFHS08FS023

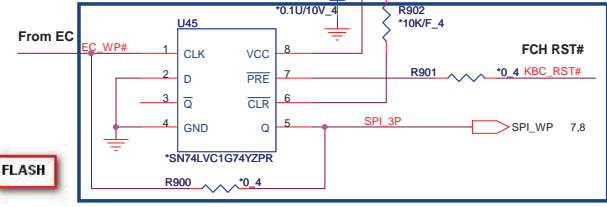
2M SPI EC ROM



128K byte SPI EC ROM



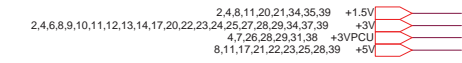
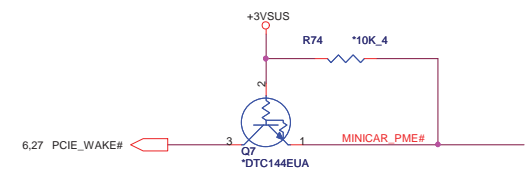
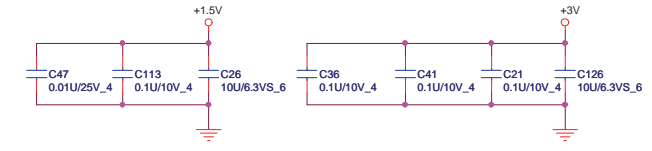
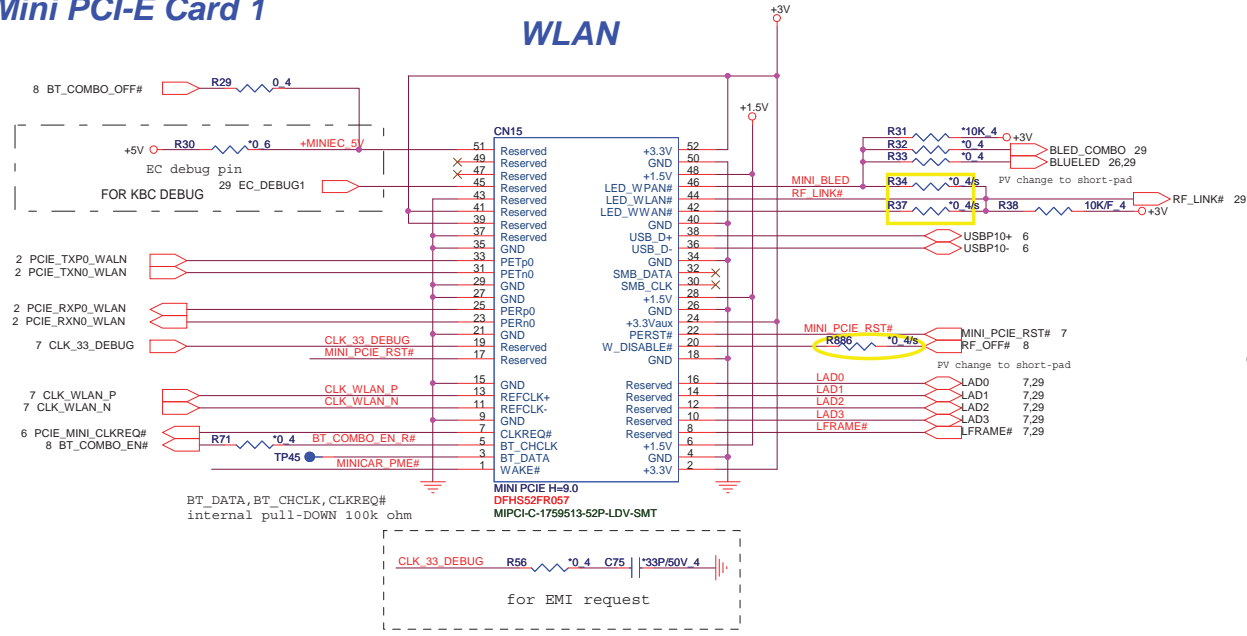
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (1)	H (1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀



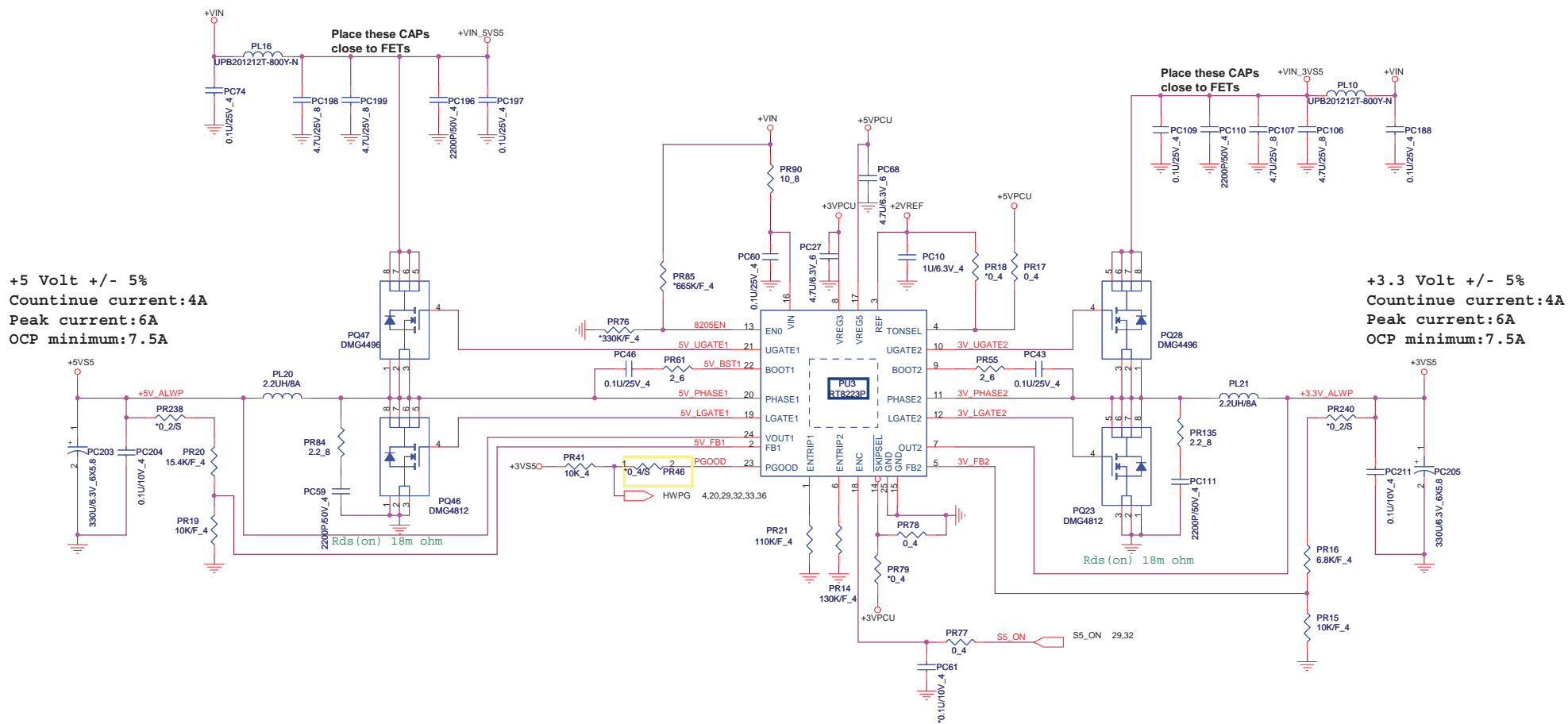
PROJECT : R23
Quanta Computer Inc.


Mini PCI-E Card 1

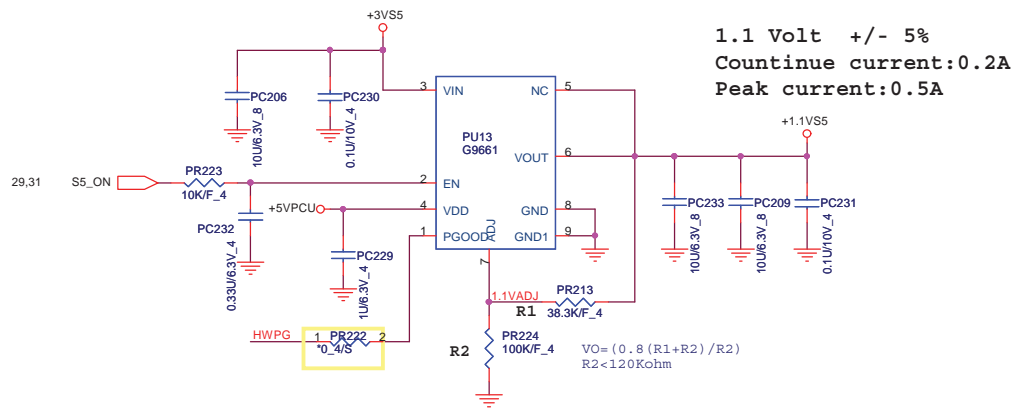
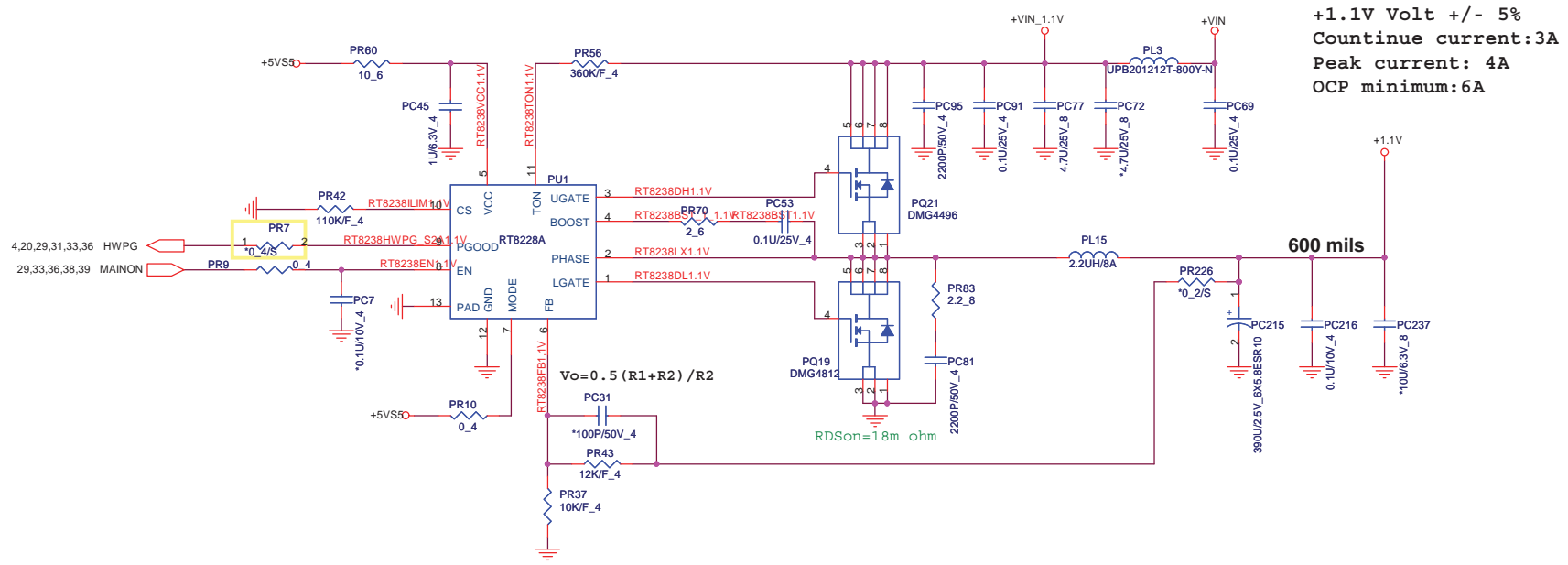
WLAN

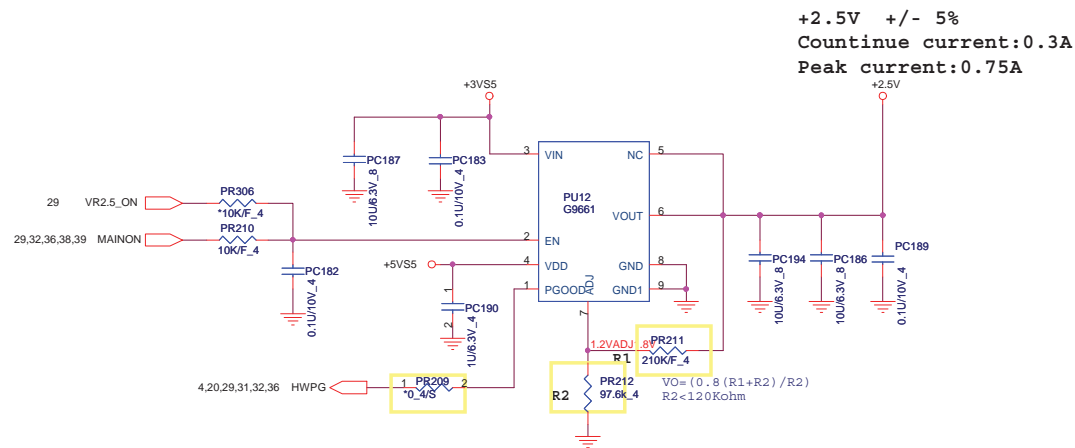
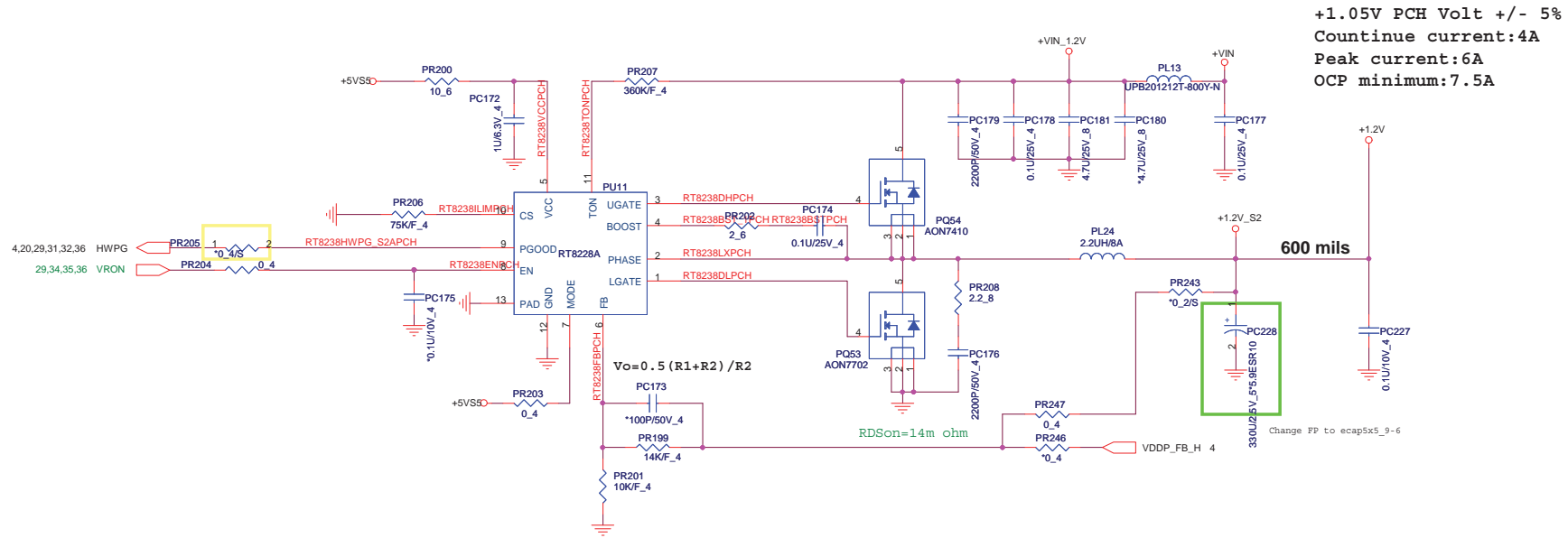



	PROJECT : R23		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number MINI PCIE CONN X1	
	Date: Tuesday, May 03, 2011	Sheet 30 of 40	

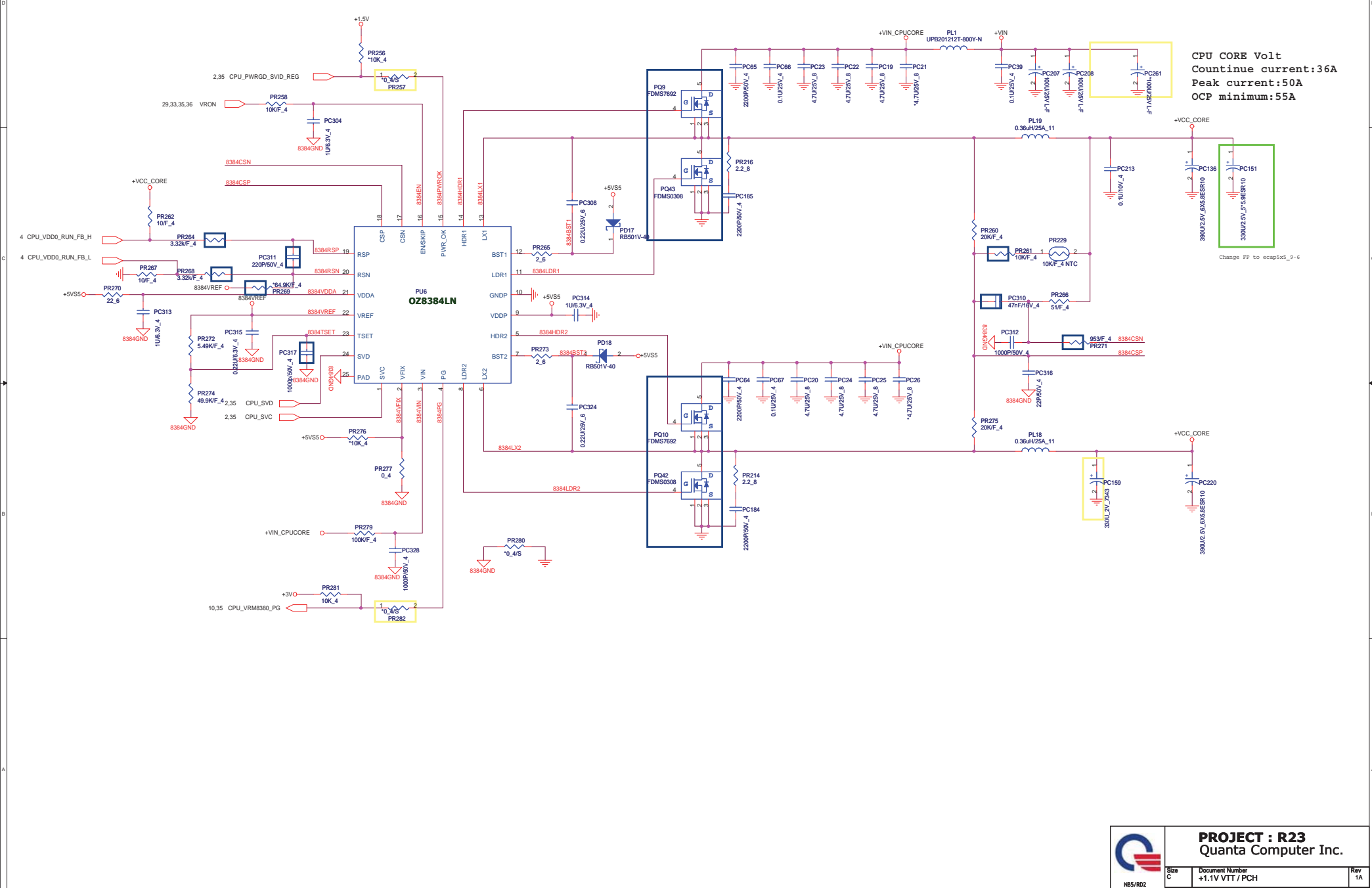


 PROJECT : R23 Quanta Computer Inc.		
Size Custom	Document Number +5V/+3V (RT8206B)	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 31	of 40



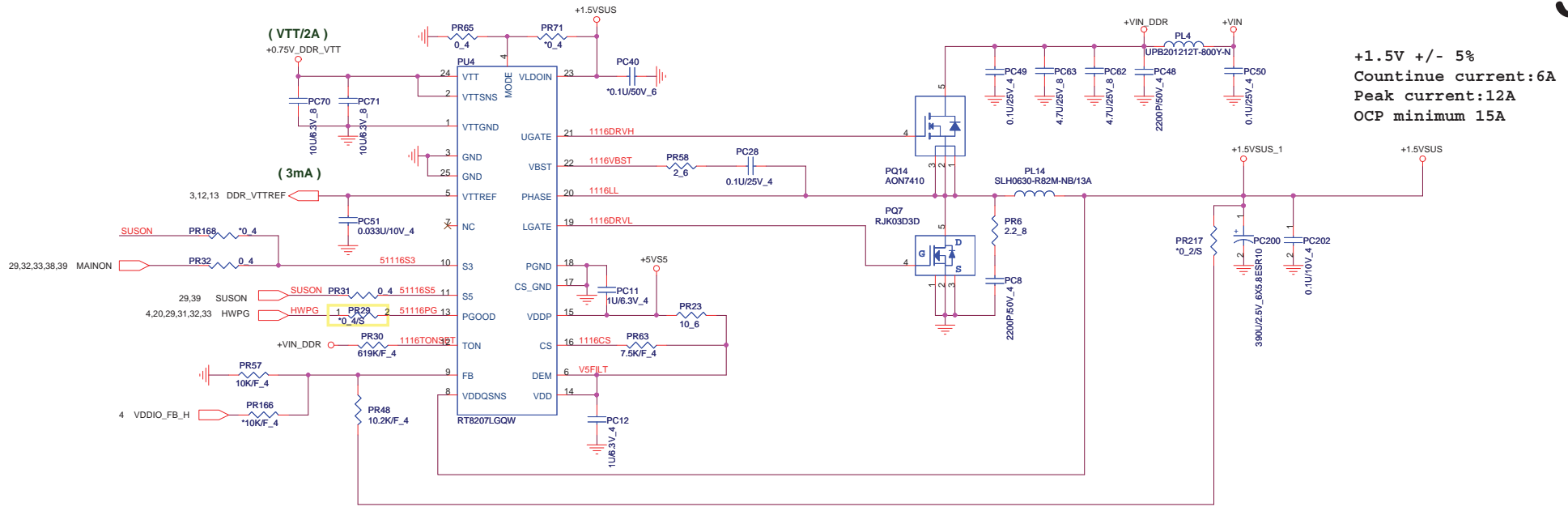


 PROJECT : R23 Quanta Computer Inc.		

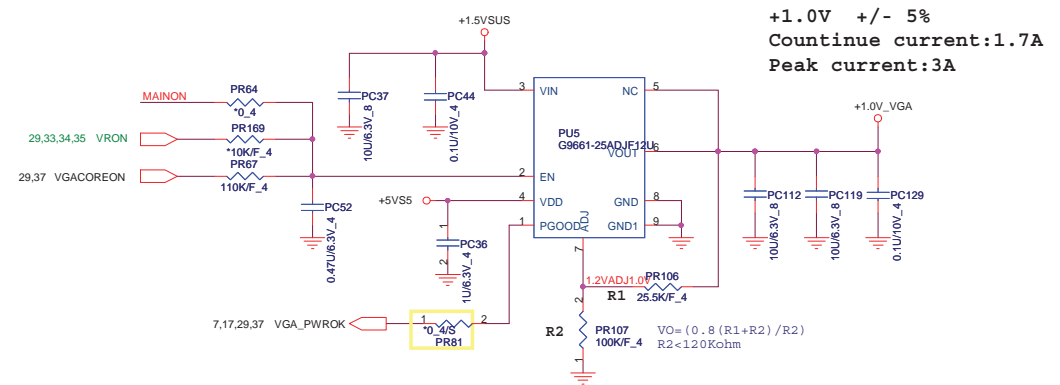
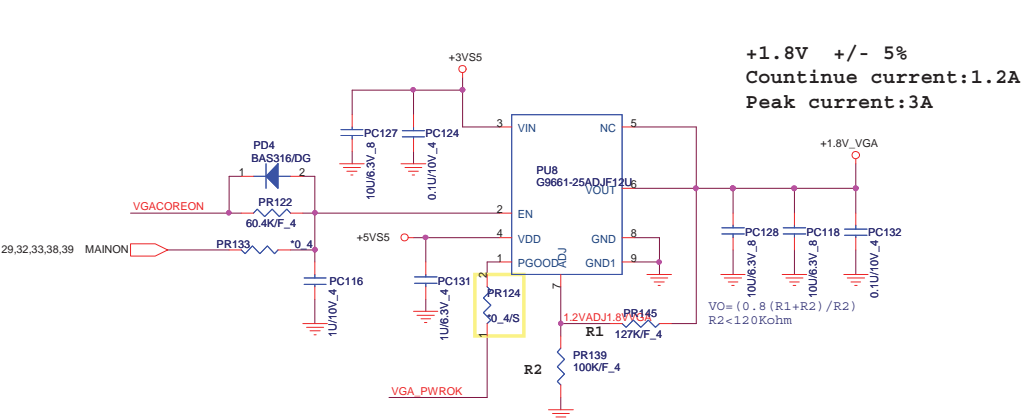


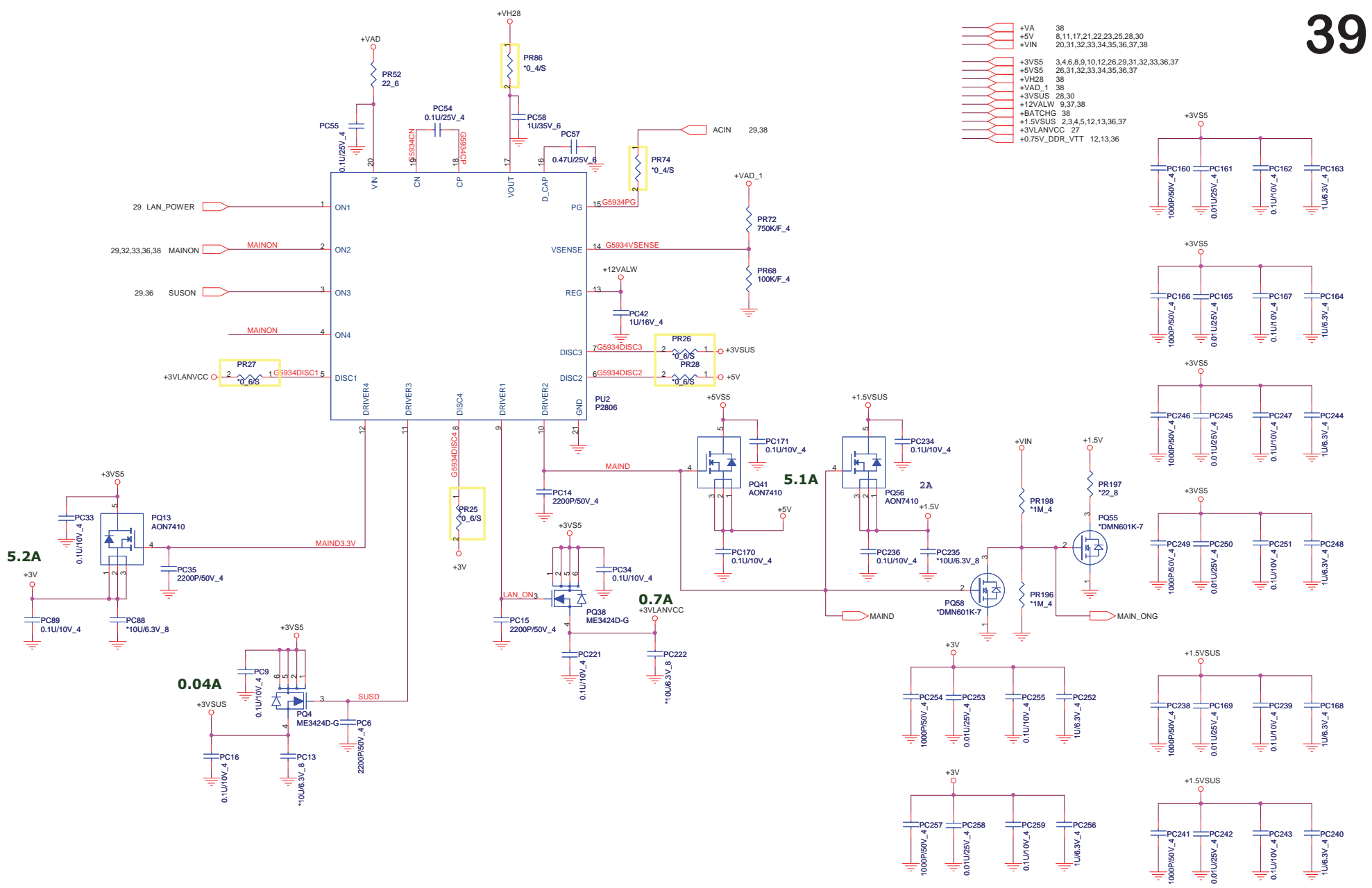
CPU CORE Volt
 Countinue current:36A
 Peak current:50A
 OCP minimum:55A

Change FP to escap5x1_9-6

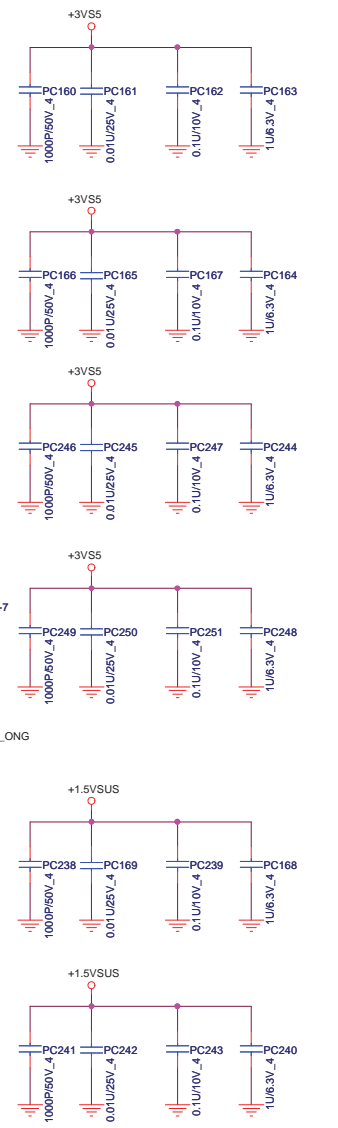



SG & Discrete Only





- +VA 38
- +5V 8,11,17,21,22,23,25,28,30
- +VIN 20,31,32,33,34,35,36,37,38
- +3VS5 3,4,6,8,9,10,12,26,29,31,32,33,36,37
- +5VS5 26,31,32,33,34,35,36,37
- +VH28 38
- +VAD_1 38
- +3VSUS 28,30
- +12VALW 9,37,38
- +BATCHG 38
- +1.5VSUS 2,3,4,5,12,13,36,37
- +3VLAVCC 27
- +0.75V_DDR_VTT 12,13,36



 PROJECT : R23 Quanta Computer Inc.			
			Size Custom
Date: Tuesday, May 03, 2011			Sheet 39 of 40