

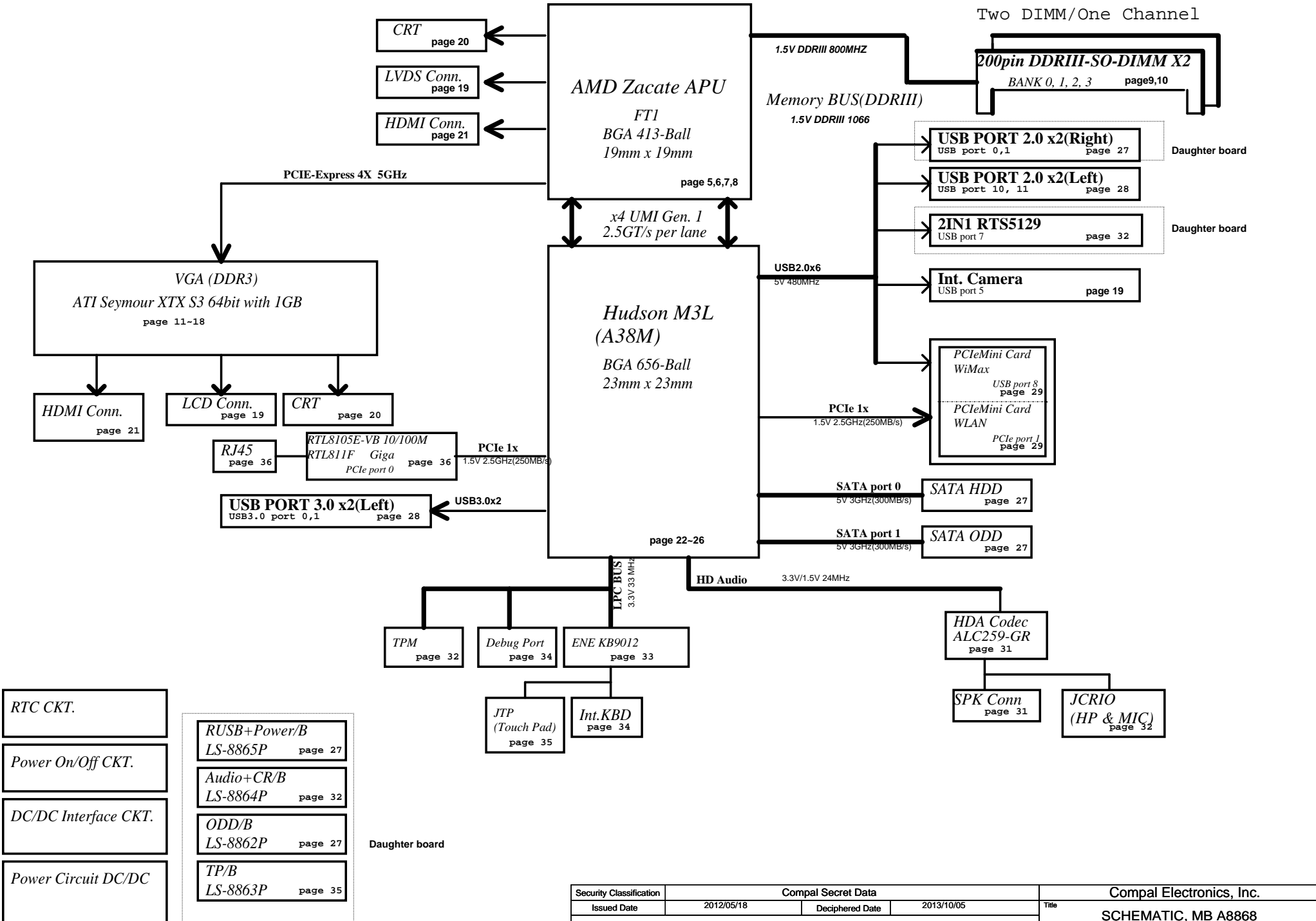
# VBLE4 / VBLE5

*Eureka*

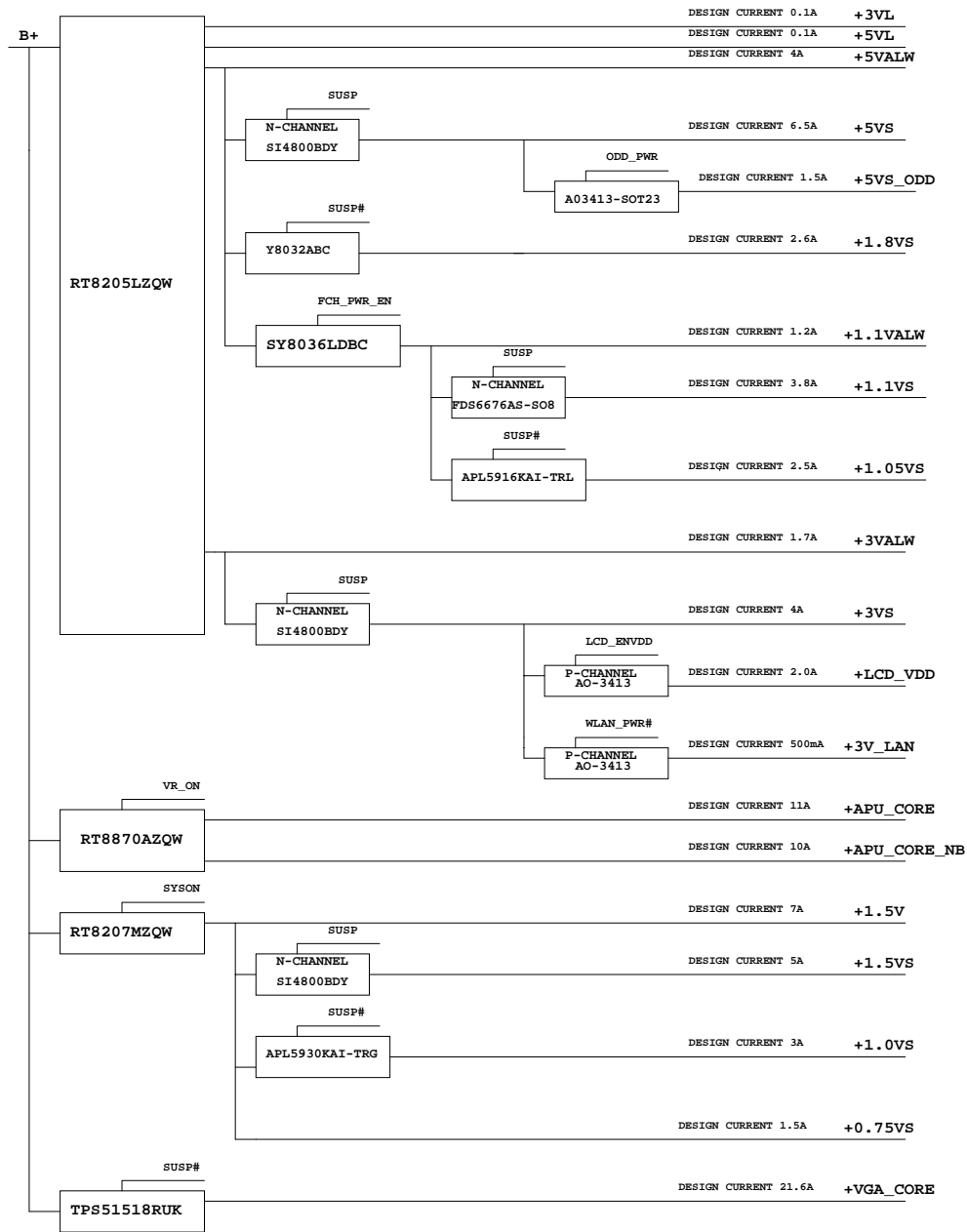
## LA-8868P REV 1.0 Schematic

AMD Brazos 2.0 / Zacate APU / Hudson-M3L FCH  
2012-07-12 Rev 1.0

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				4019K4	B
				Date:	Saturday, September 07, 2013
				Sheet	1 of 47



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Date:	Saturday, September 07, 2013		Sheet	2 of 47		





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Document Number 4019K4			Rev B	

### Voltage Rails

O MEANS ON X MEANS OFF

State	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +0.9VS +0.75VS +NB_CORE +VDDNB +CPU_CORE_0
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

### Symbol Note :

 : means Digital Ground  : means Analog Ground

@ : means just reserve , no build  
 K625R3@ : means just for 1.5G CPU  
 K125R3@ : means just for 1.7G CPU  
 K325R3@ : means just for 1.3G CPU  
 K625R1@ : means just for 1.5G CPU  
 K125R1@ : means just for 1.7G CPU  
 K325R1@ : means just for 1.3G CPU  
 M@ : means just reserve for  
~~S@3 control~~  
 @3 control : means just reserve for 11.6 control  
 GSENSOR@ : means just reserve for G sensor  
 part 1ST@ : means just reserve 1st G sensor  
 1STGSENSOR@ : means just reserve 1st G sensor IC  
 2ND@ : means just reserve 2nd G sensor IC  
~~2NDGSENSOR@ : means just reserve 2nd G sensor IC~~  
 NOSIDE@ : means just reserve NOSIDE  
 SIDE@ : means just reserve SIDE  
 RS880MR1@ : means just for  
 RS880MR3@ : means just for  
~~SB820MR1@ : means just for SB820MR1~~  
 SB820MR3@ : means just for SB820MR3

### SB SM Bus1 Address

### SB SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				

### SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM 0	CLK GEN	WLAN WWAN	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB926	V							
EC_SMB_CK2 EC_SMB_DA2	KB926								V
LCD_EDID_CLK LCD_EDID_DATA	APU FT1						V		
HDMICLK HDMIDAT	APU FT1							V	
SMB_CK_CLK0 SMB_CK_DAT0	FCH M1			V					
SMB_CK_CLK1 SMB_CK_DAT1	FCH M1					V			

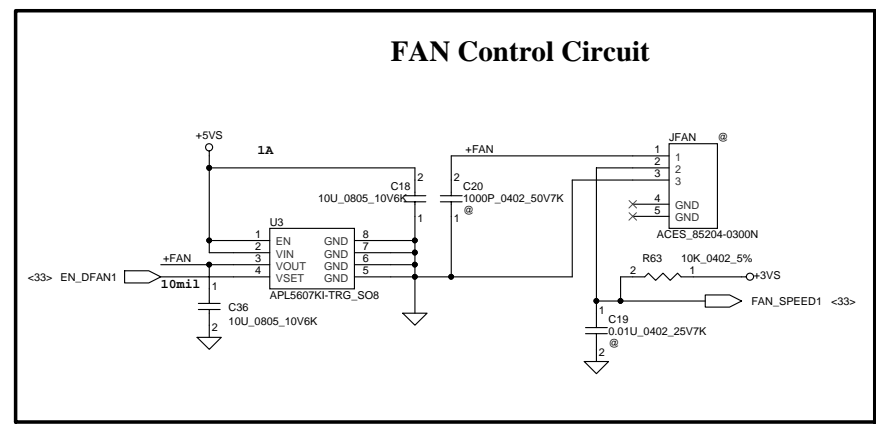
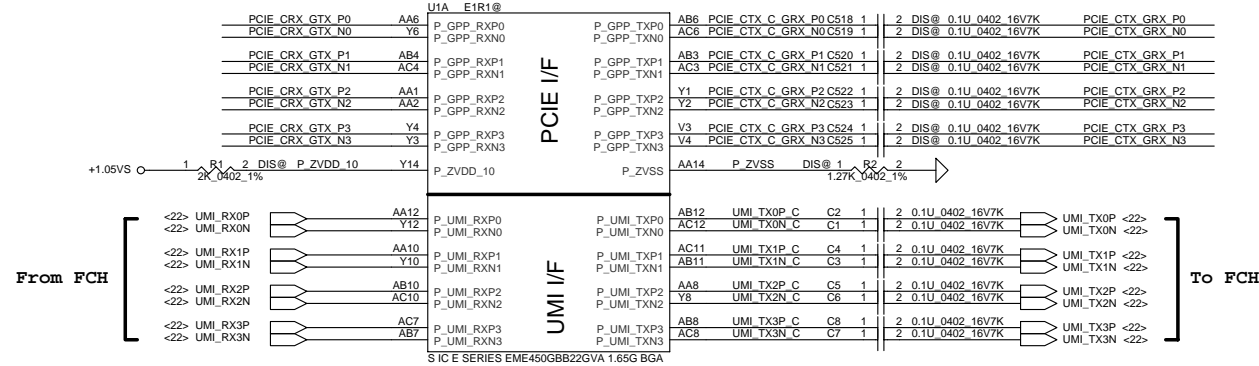
### EC SM Bus1 Address

### EC SM Bus2 Address

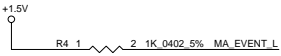
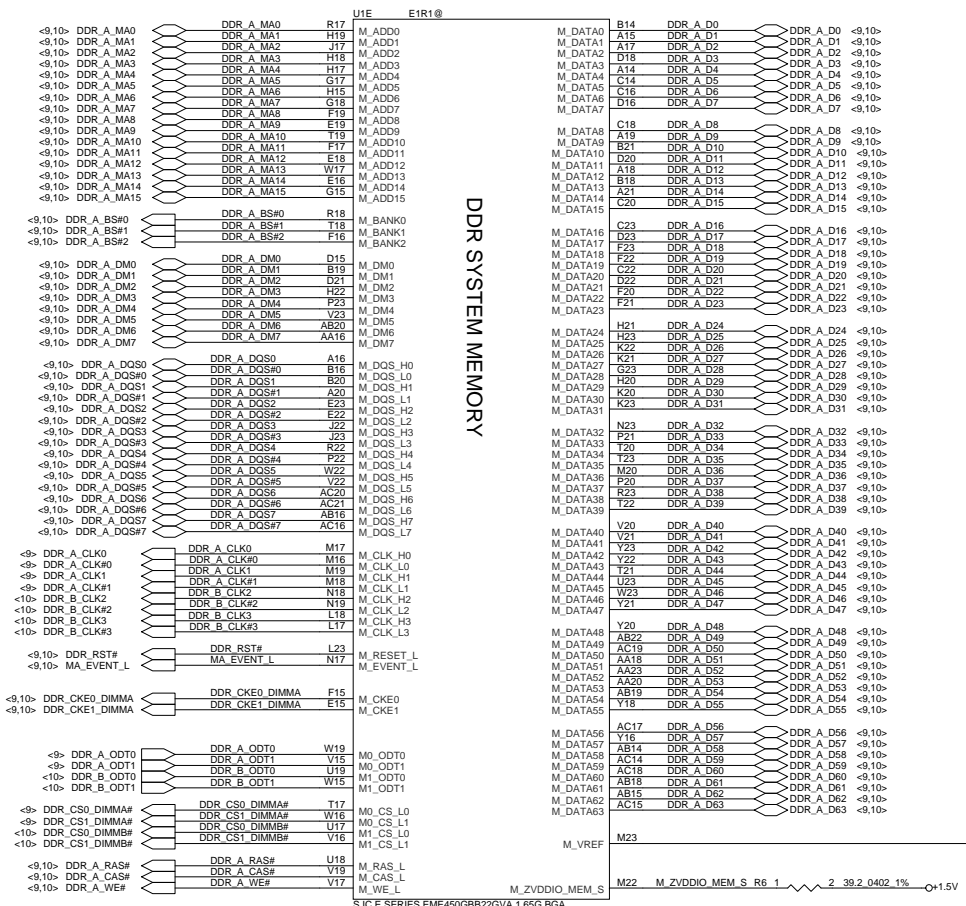
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b
				+3VS	G-Sensor		

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				4019K4	B	
Date: Saturday, September 07, 2013				Sheet	4 of 47	

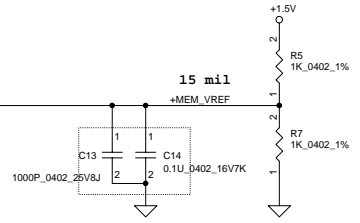
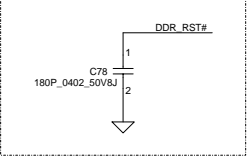
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 <11> PCIE\_CTX\_GRX\_N[3..0] ← PCIE\_CTX\_GRX\_N[3..0]  
 <11> PCIE\_CRX\_GTX\_P[3..0] ← PCIE\_CRX\_GTX\_P[3..0]  
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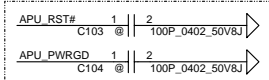
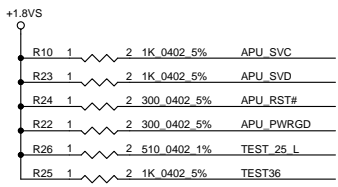
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Date:				Saturday, September 07, 2013	Sheet 5 of 47



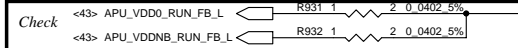
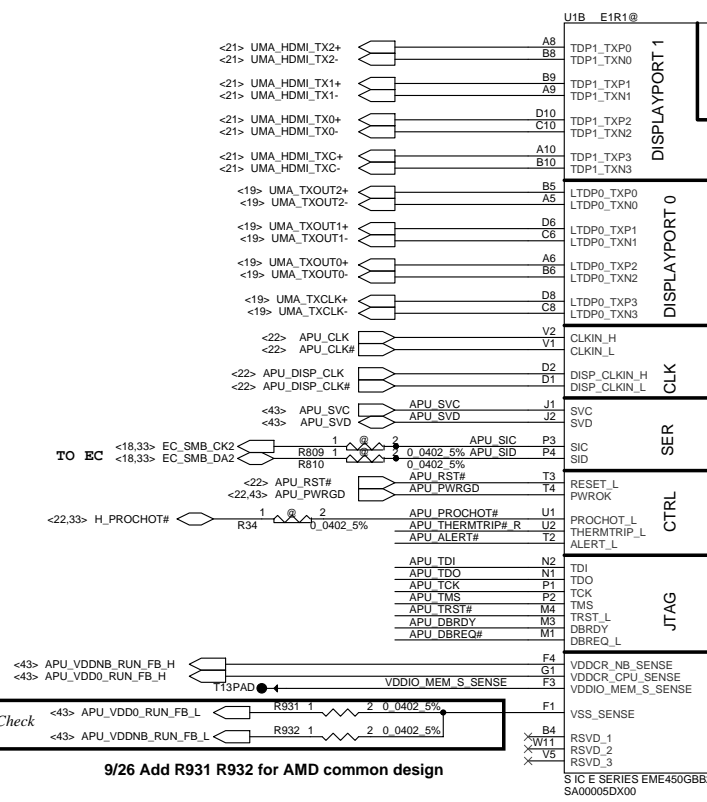
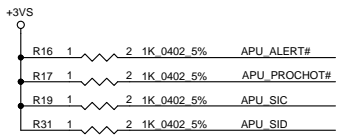
8/6 Add C78 for ESD request



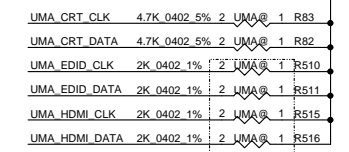
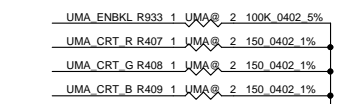
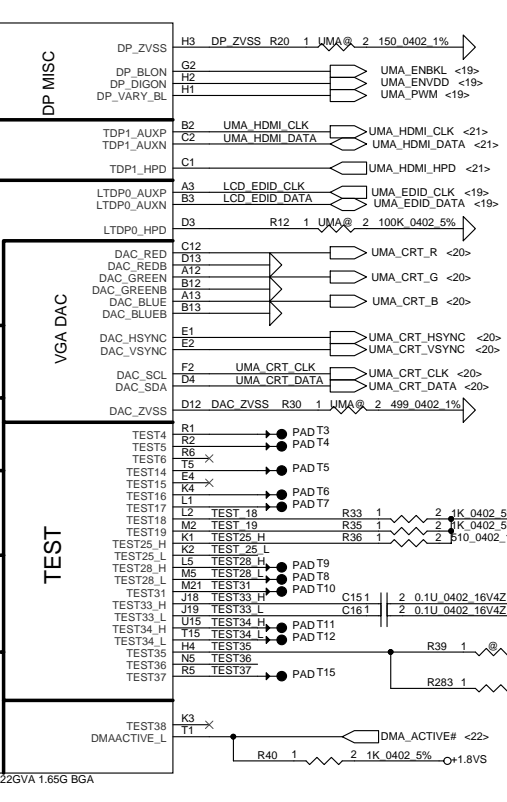
Close to CPU within 1"



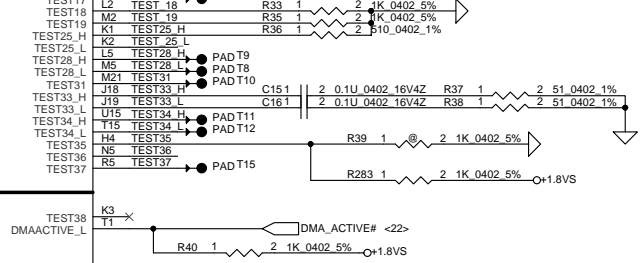
12/13 For debug if layout cross mote



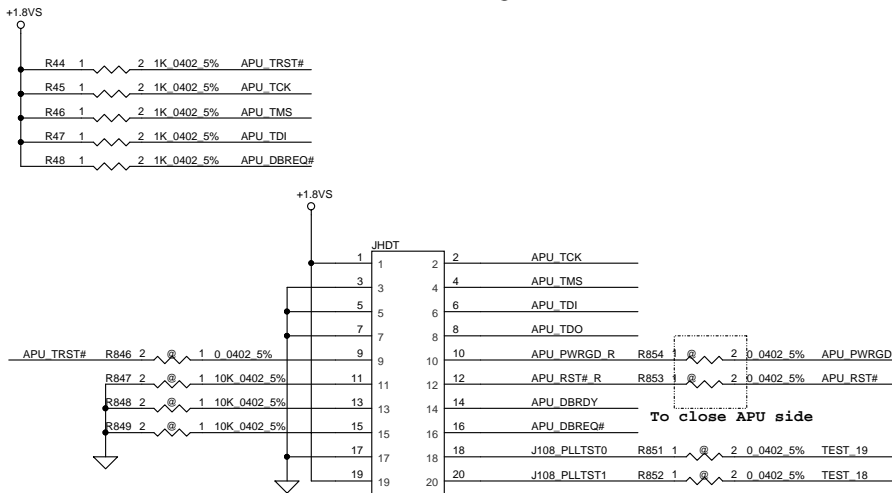
9/26 Add R931 R932 for AMD common design



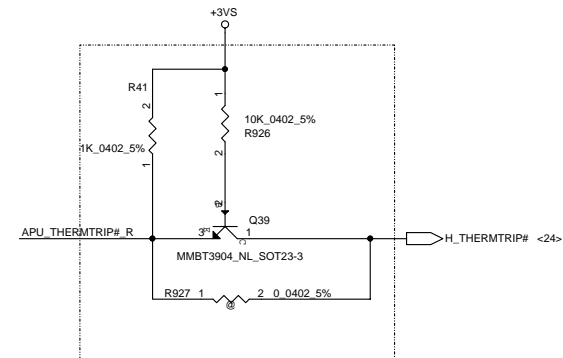
12/22 Change R510, R511, R515, R516 to 2k that meet AMD check list



# AMD HDT Debug Conn

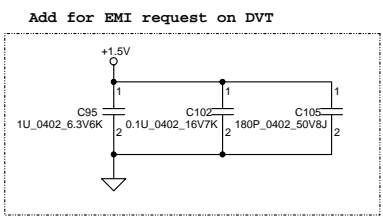
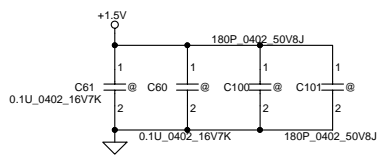
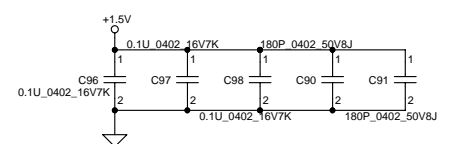
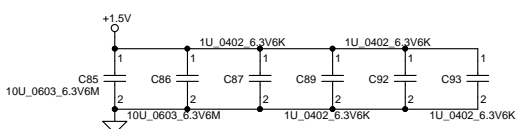
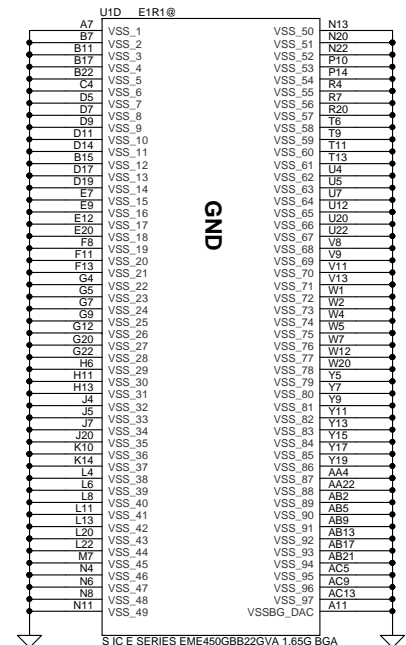
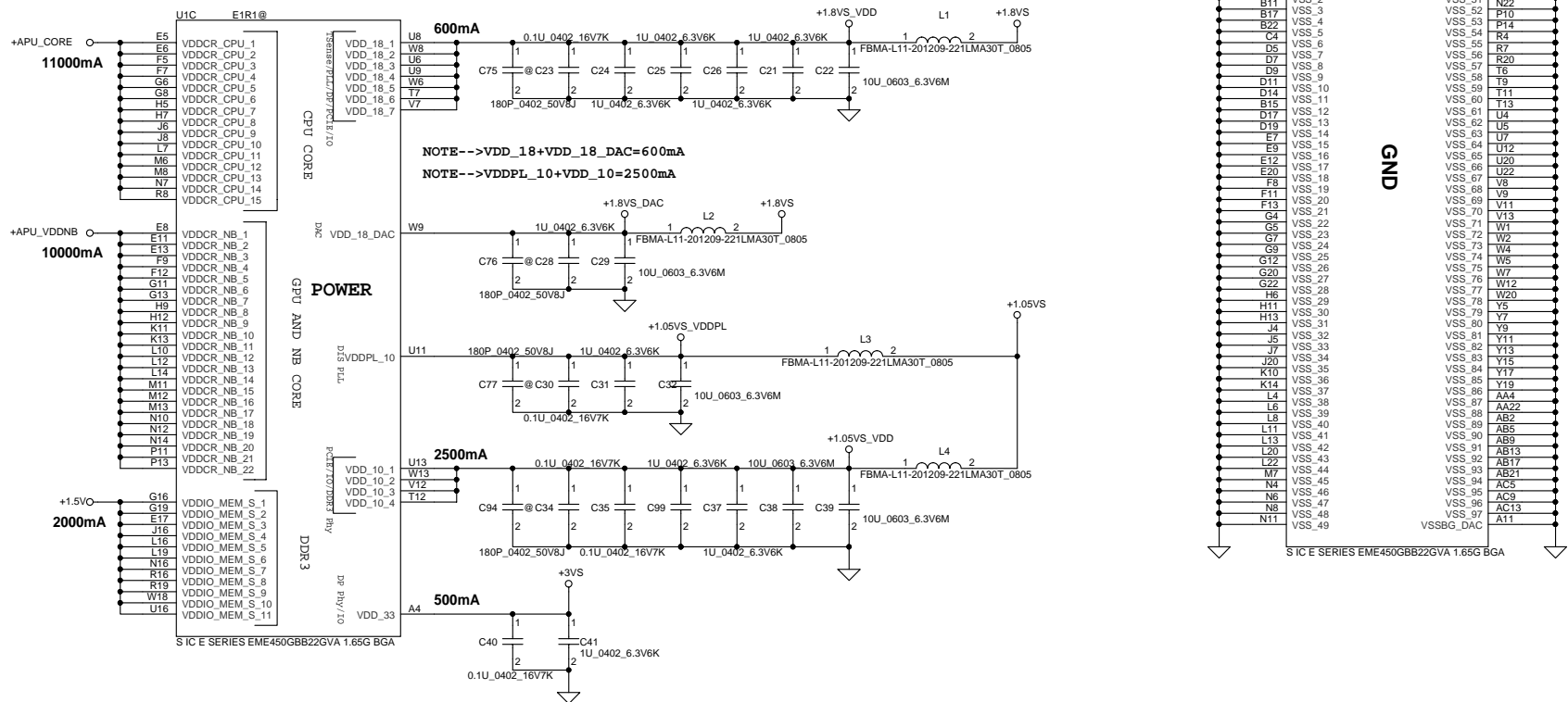


To close APU side



12/22 PCH side has internal pull up +3VLAW\_PCH, so need to level shift

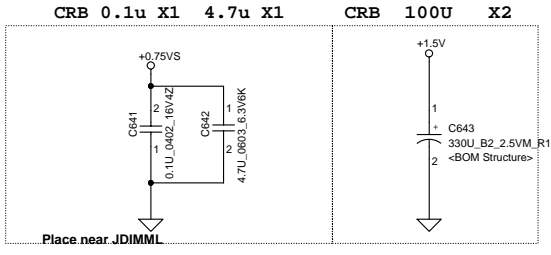
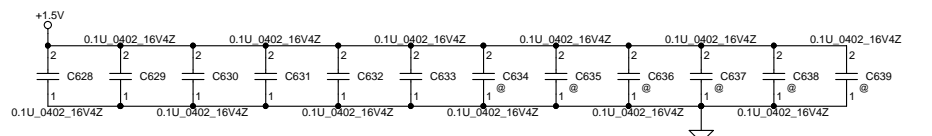
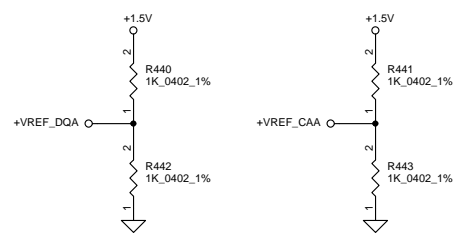
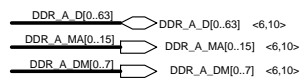
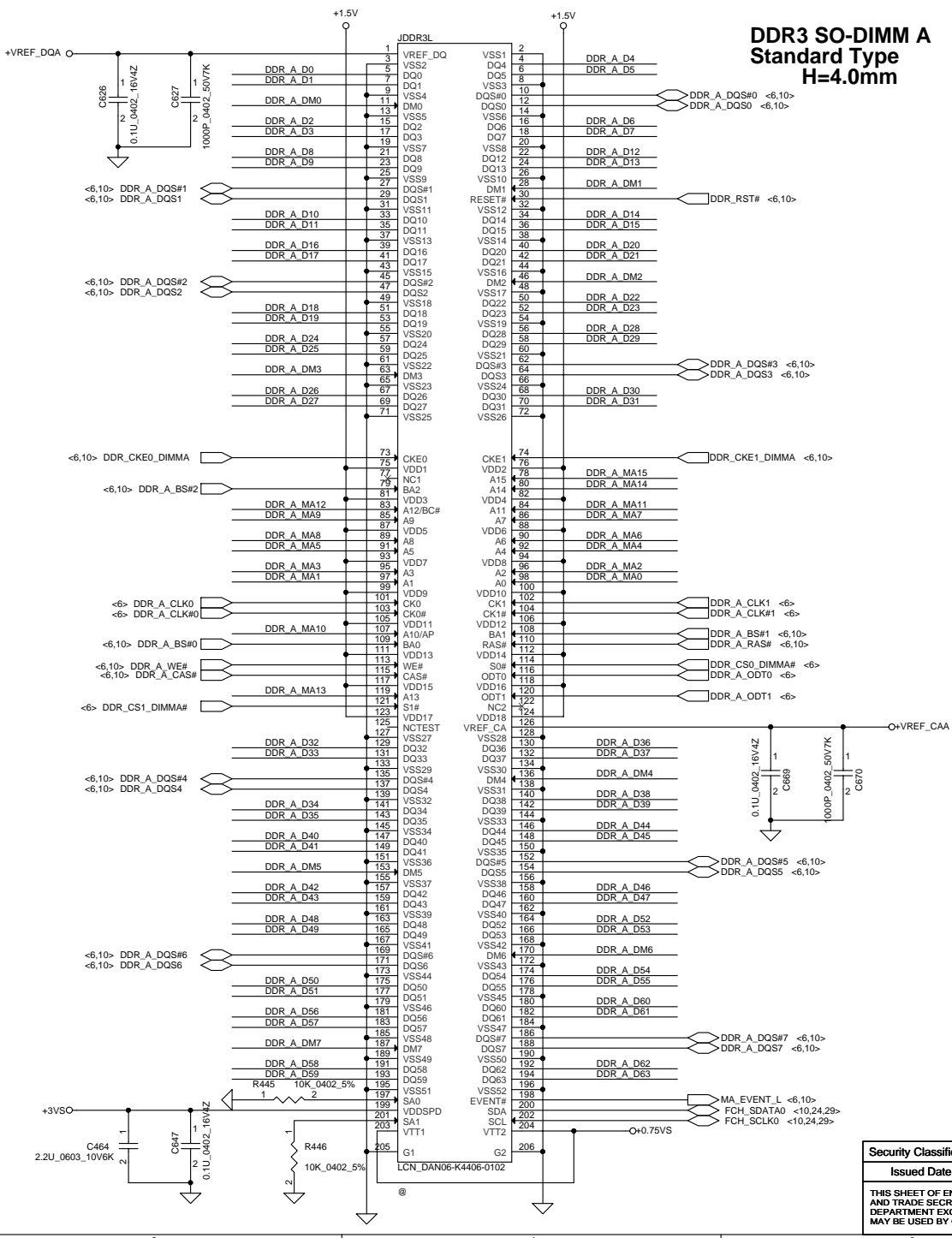
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				4019K4	B
				Date:	Sheet
				Saturday, September 07, 2013	7 of 47



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				4019K4	B
Date: Saturday, September 07, 2013				Sheet	8 of 47



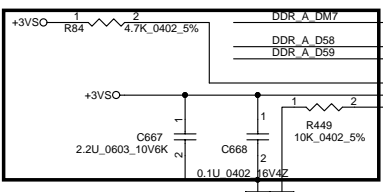
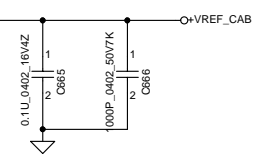
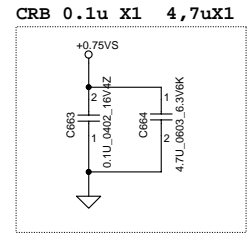
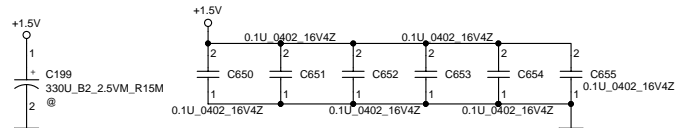
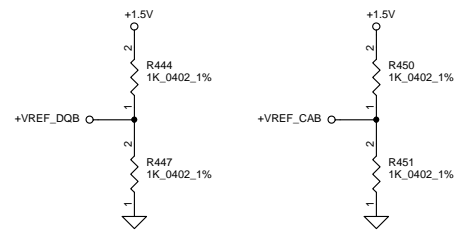
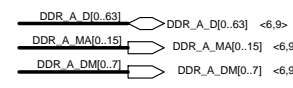
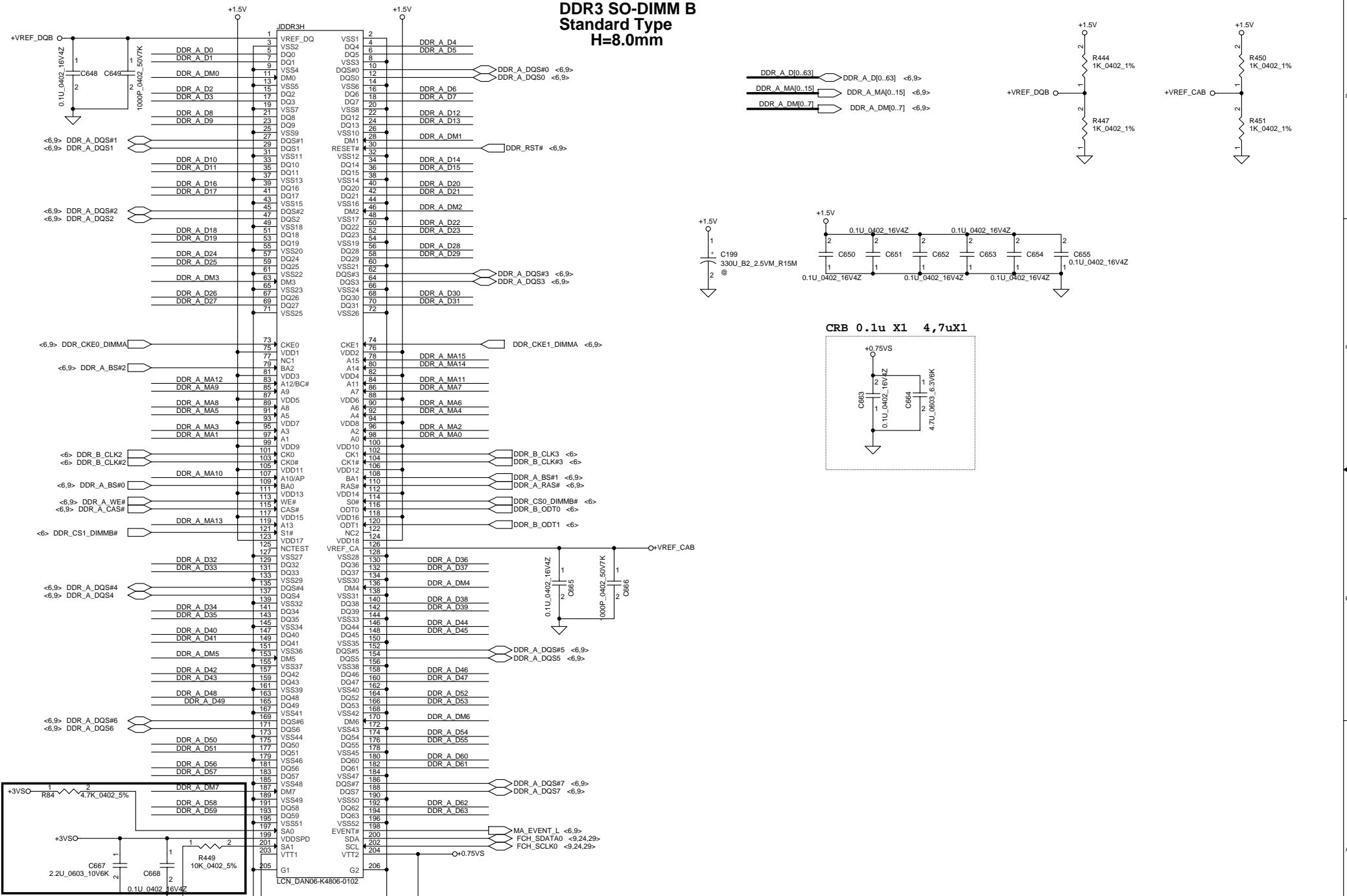
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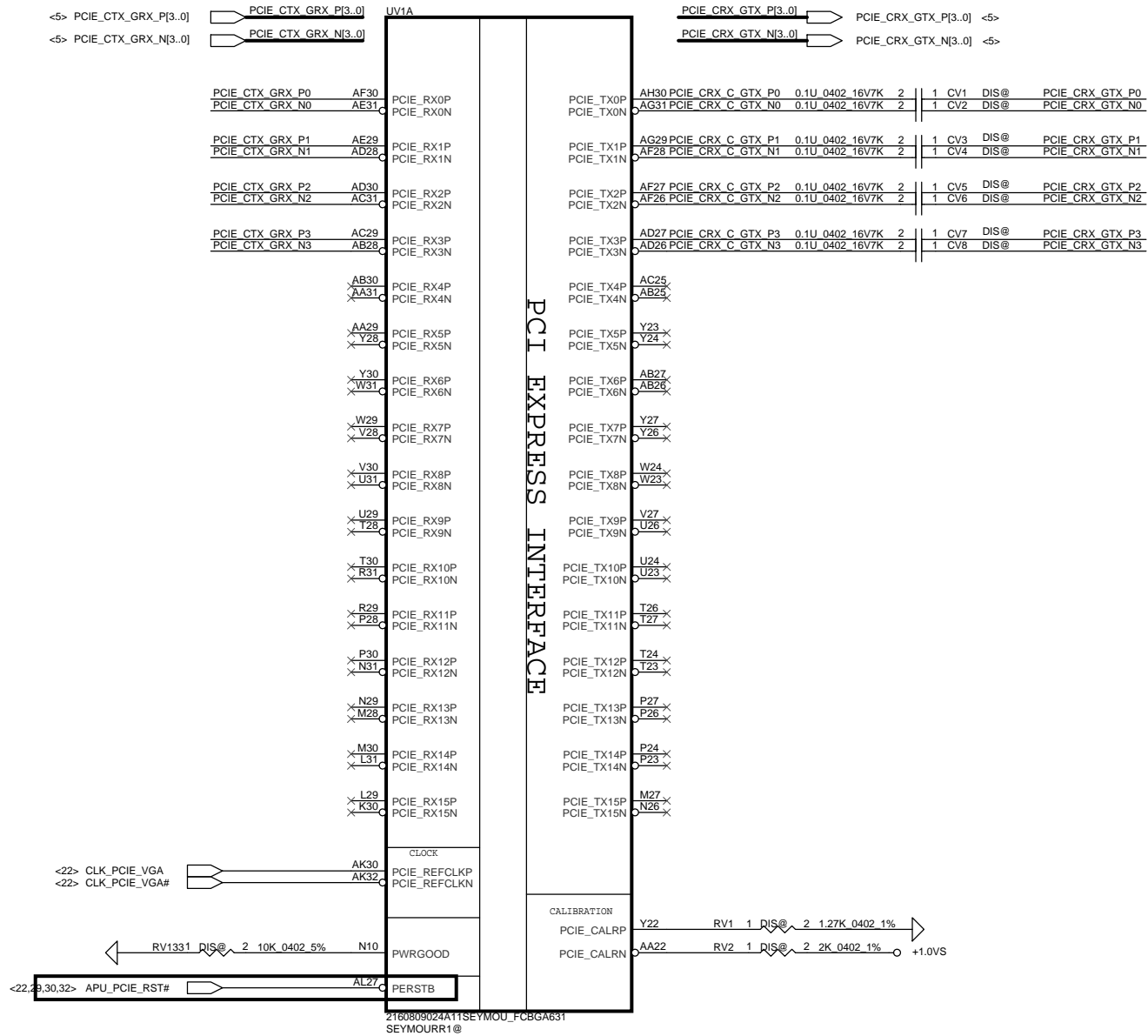
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<b>Rev</b> B							
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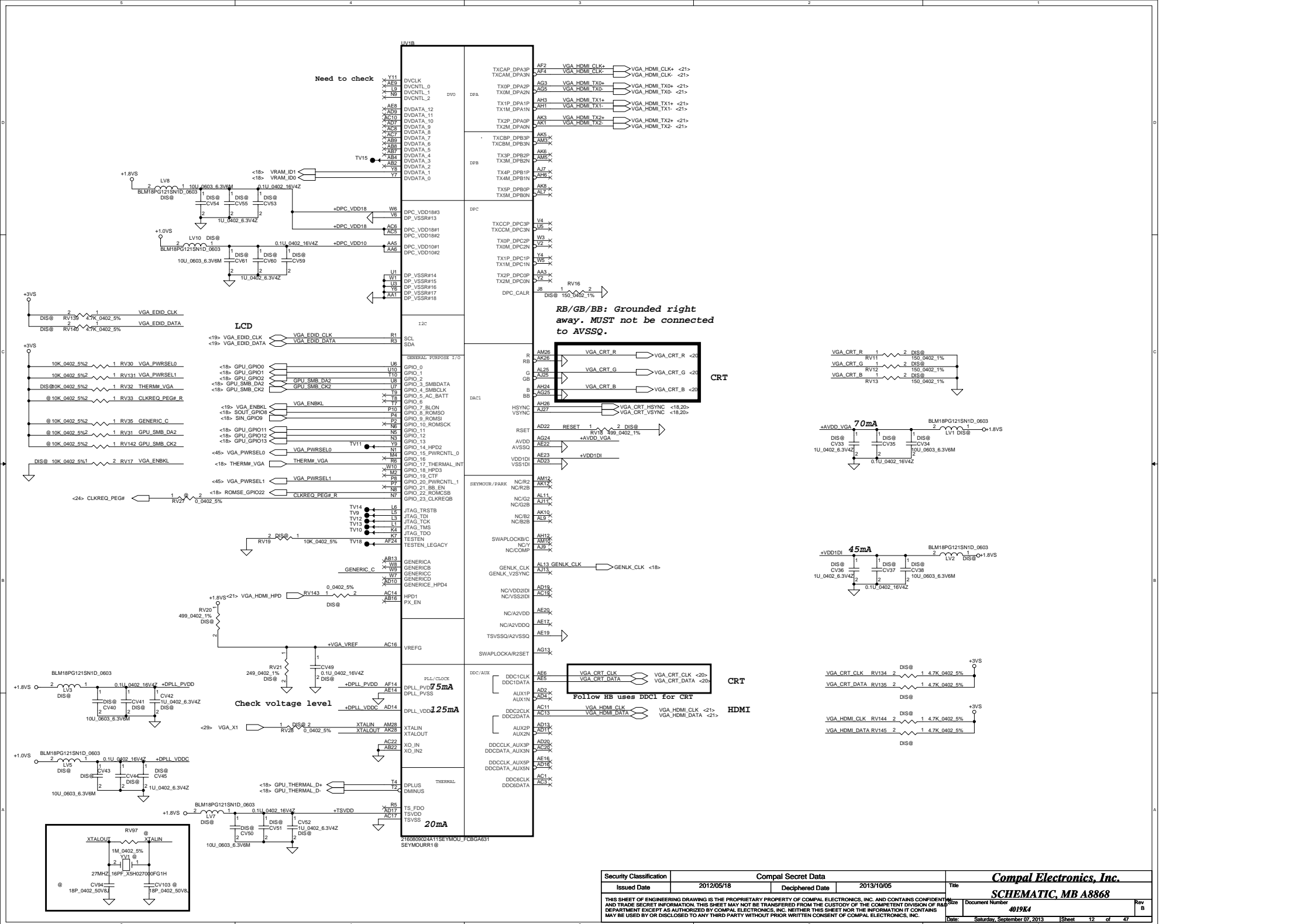
# DDR3 SO-DIMM B Standard Type H=8.0mm



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Customer	4019K4	Rev	B	Date:	Saturday, September 07, 2013
Sheet	10	of	47		



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				4019K4	
Date:				Saturday, September 07, 2013	Sheet 11 of 47



Need to check

LCD

Check voltage level

RB/GB/BB: Grounded right away. MUST not be connected to AVSSQ.

CRT

CRT

HDMI

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Issued Date

2012/05/18

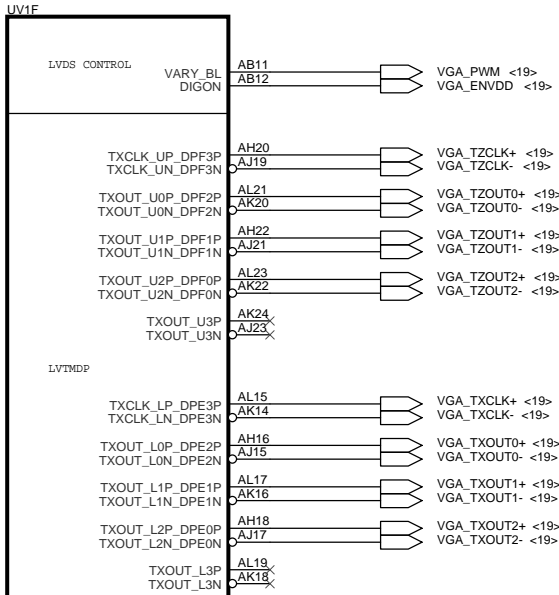
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2013/10/05

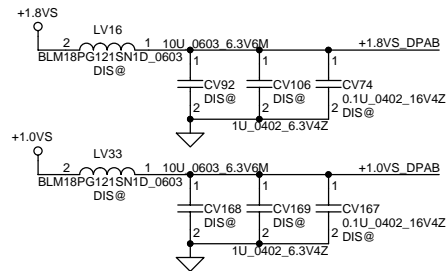
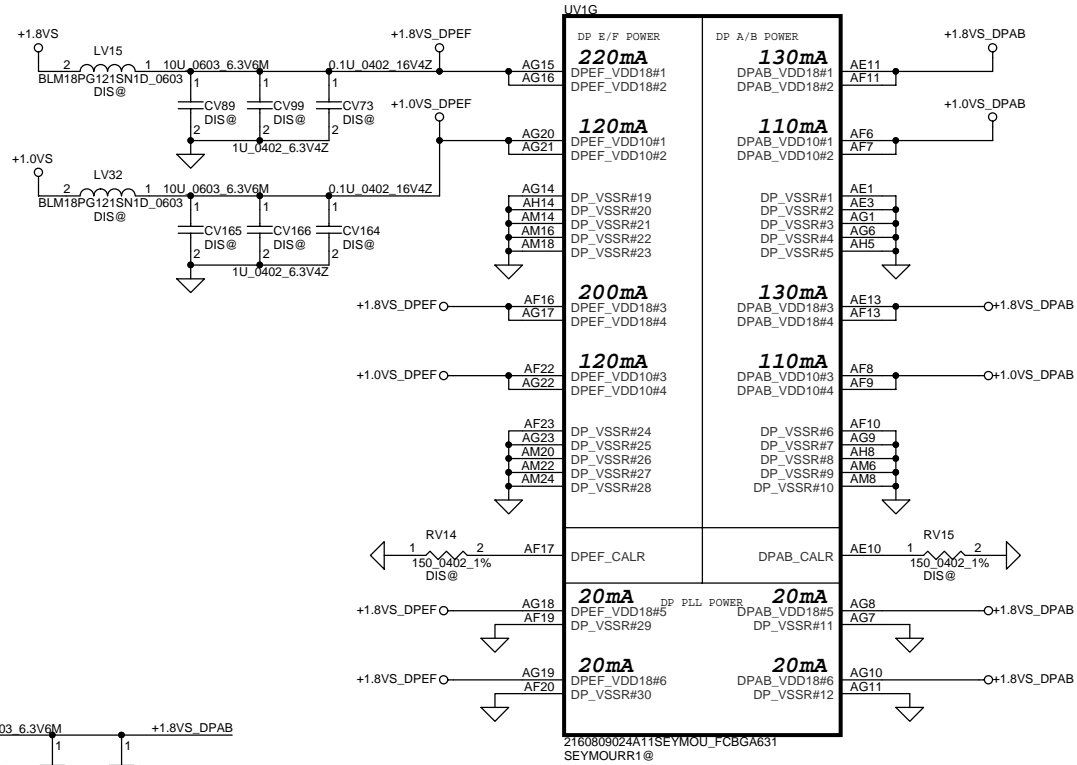
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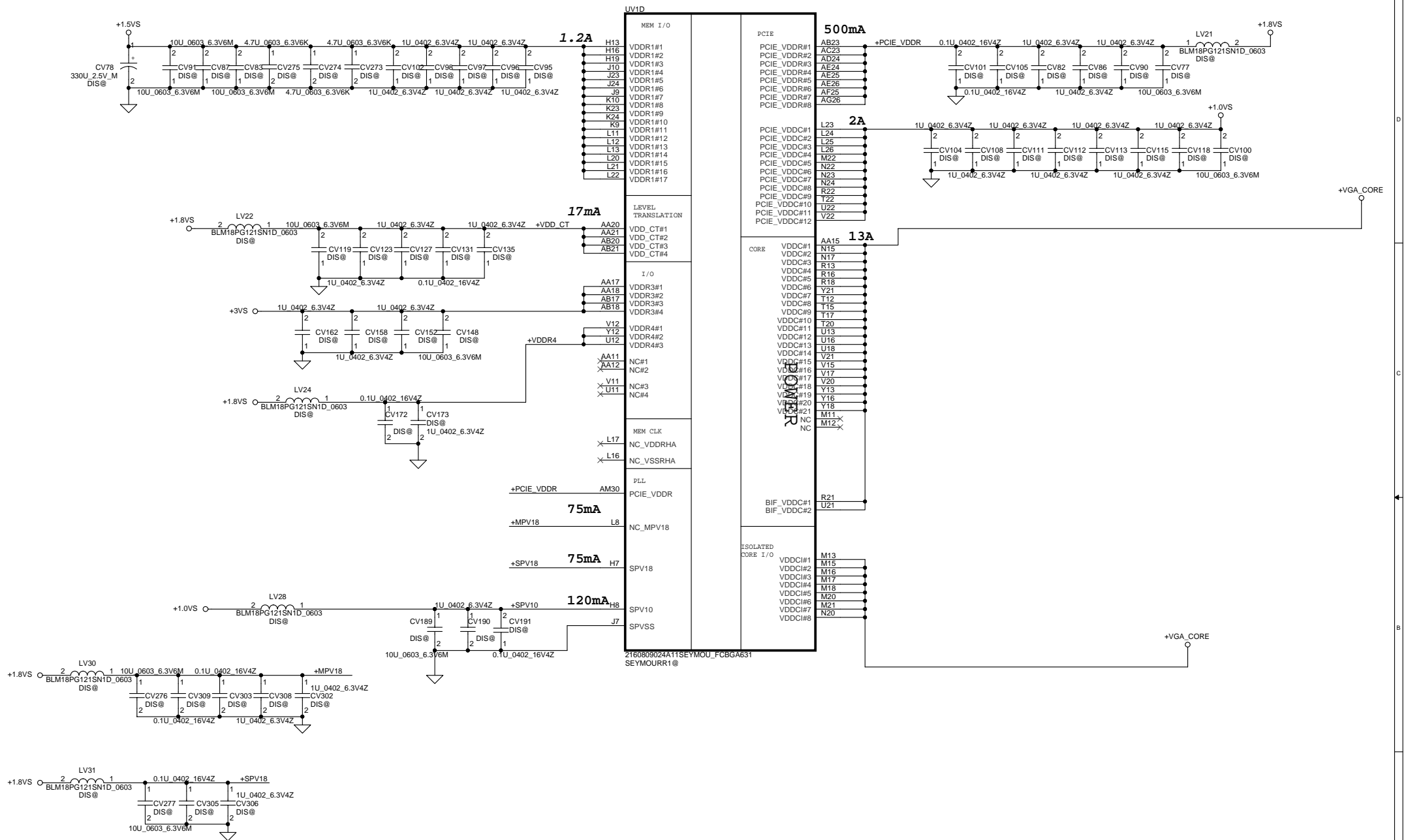
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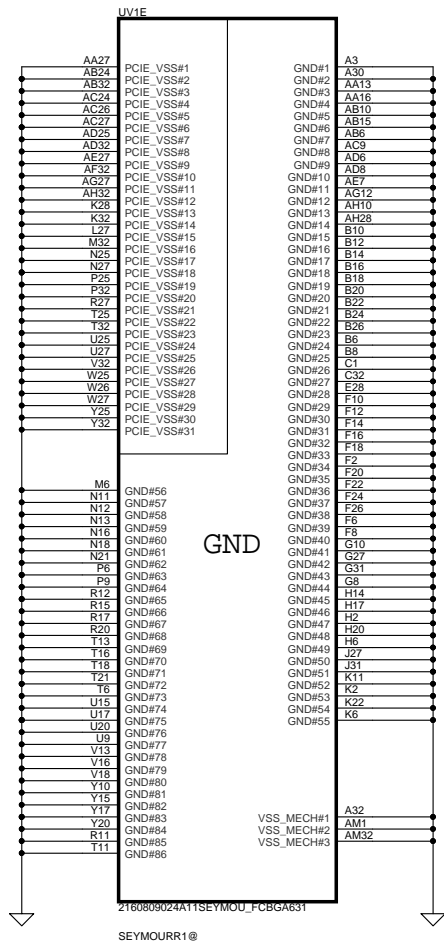
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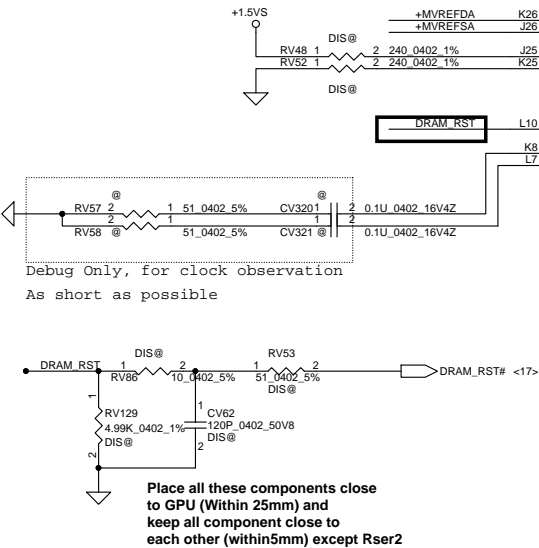
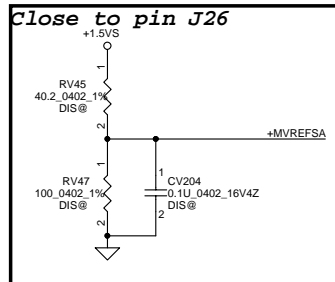
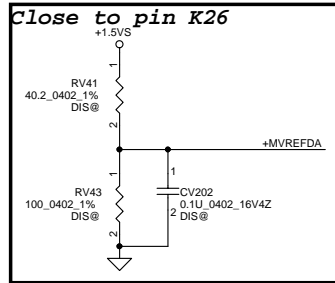
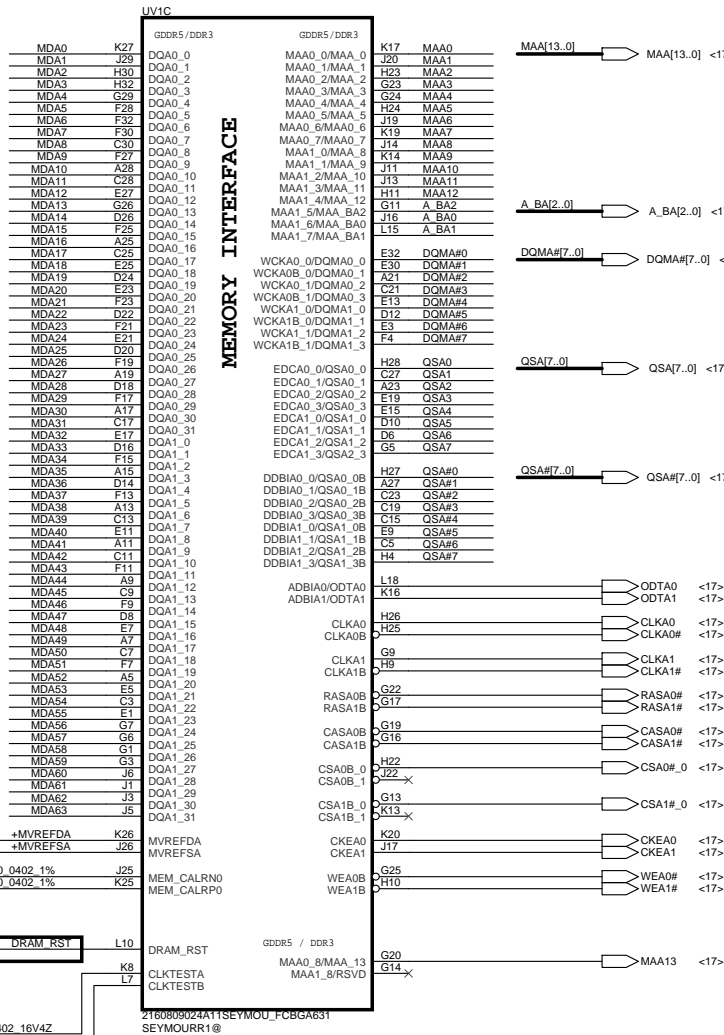
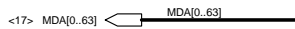
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				4019K4	B
Date: Saturday, September 07, 2013				Sheet	13 of 47



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Size	Document Number	4019K4		Rev	B
Date:	Saturday, September 07, 2013	Sheet	14	of	47



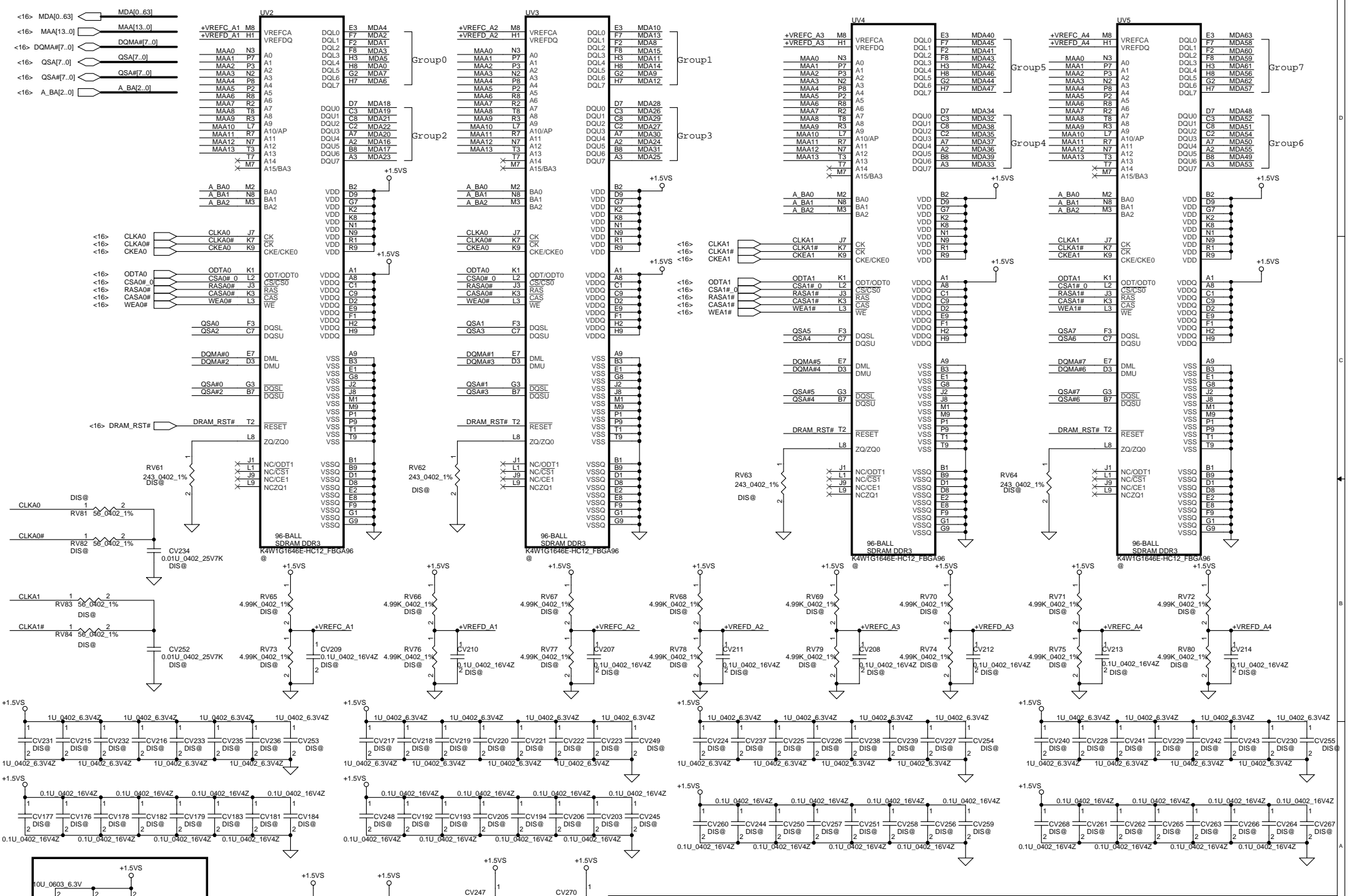
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				4019K4	B
				Date:	Sheet
				Saturday, September 07, 2013	15 of 47



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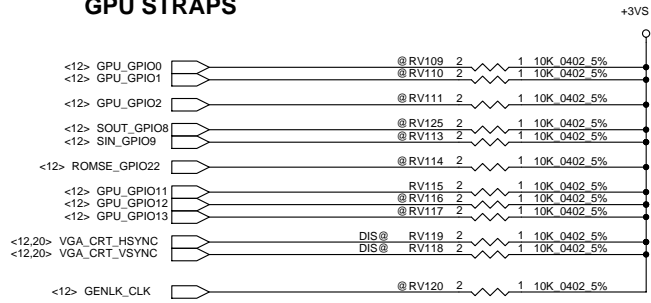
<b>Compal Electronics, Inc.</b>	
<b>SCHEMATIC, MB A8868</b>	
Document Number	Rev B
4019K4	
Date:	Saturday, September 07, 2013
Sheet	16 of 47





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Date:	Saturday, September 07, 2013	Sheet	17	of	47

### GPU STRAPS



GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0
0 0 1	256MB	(M25P05A)
0 1 0	64MB	

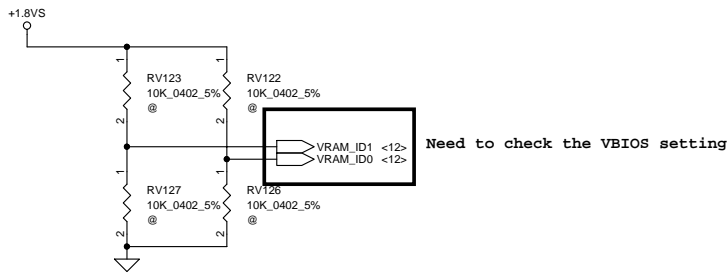
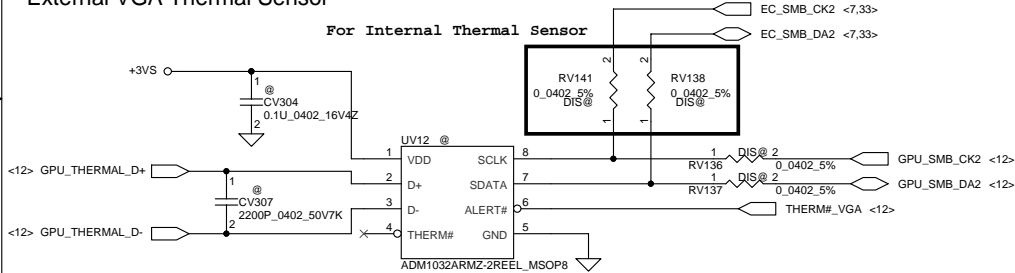
### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPI00	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPI01	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPI02	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (Internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPI011 GPU_GPI012 GPU_GPI013	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
RESERVED	GENLK_CLK	GENLK_CLK		0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

### External VGA Thermal Sensor

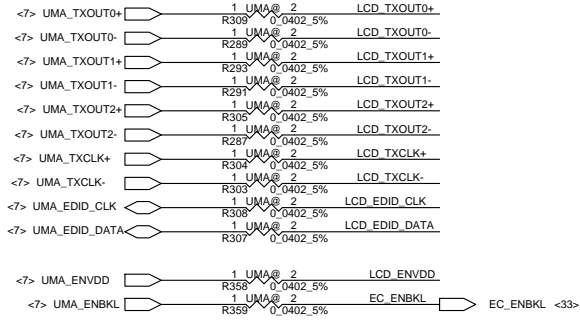
For Internal Thermal Sensor



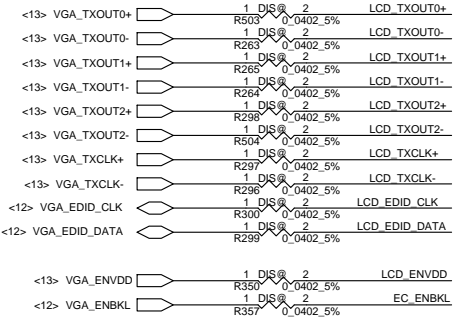
STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 1,0
VRAM_ID[1:0]	DVDATA (1,0)	Seymour-S3	512M 64Mx16 (x4)	SAM K4W1G1646G-BC11	SA00004GS00	1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC11	SA000047Q00	1 1

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Date:	Saturday, September 07, 2013	Sheet	18	of 47

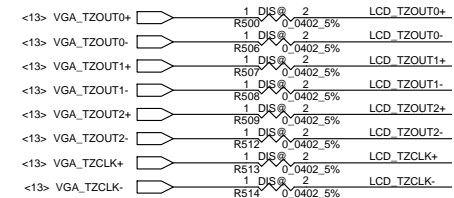
**UMA**



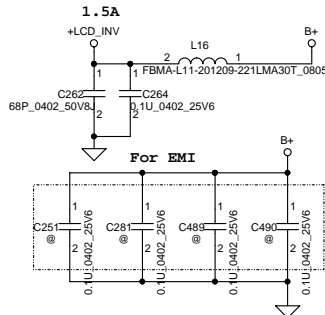
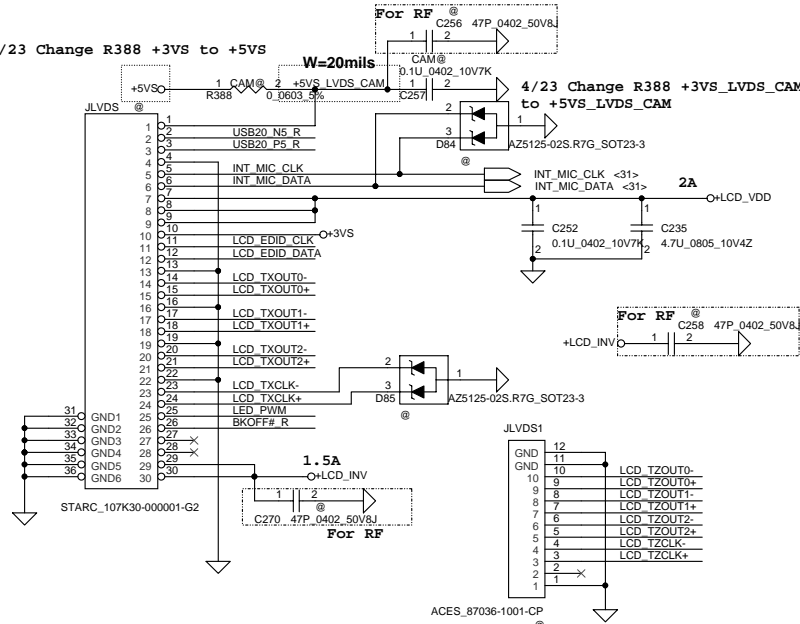
**DISCRETE**



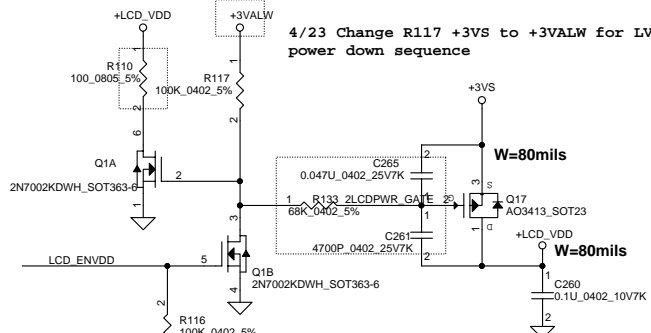
Close to LVDS Connector



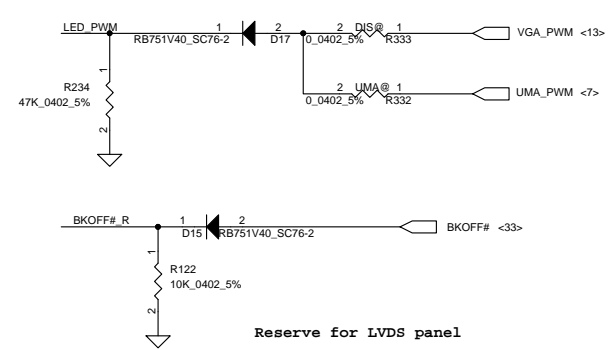
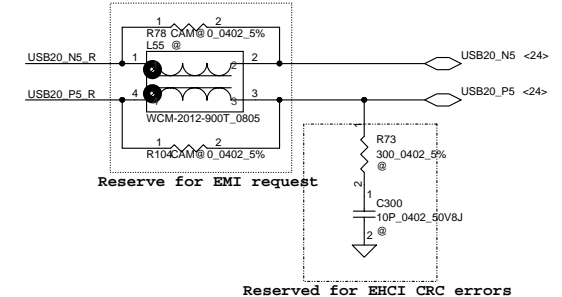
4/23 Change R388 +3VS to +5VS



4/23 Change R117 +3VS to +3VALW for LVDS power down sequence



4/23 Change R110, R133, C265, C261 for LVDS power down sequence

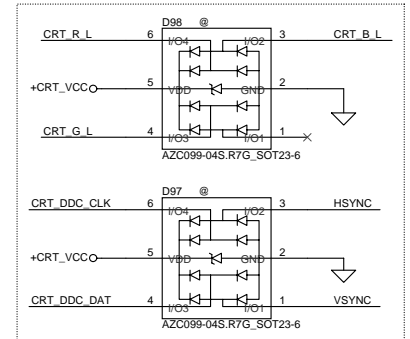
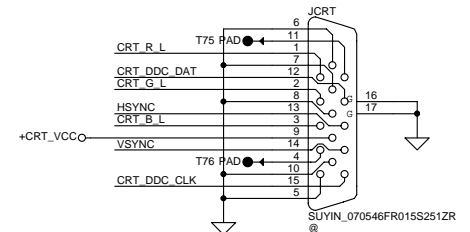
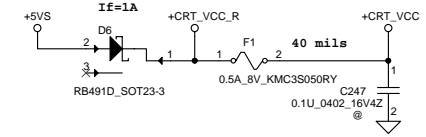


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				4019K4	B
				Date: Saturday, September 07, 2013	Sheet 19 of 47

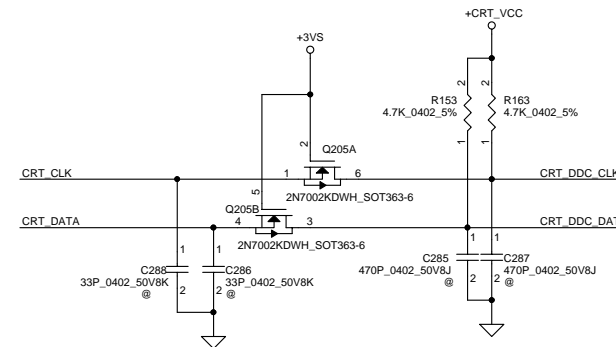
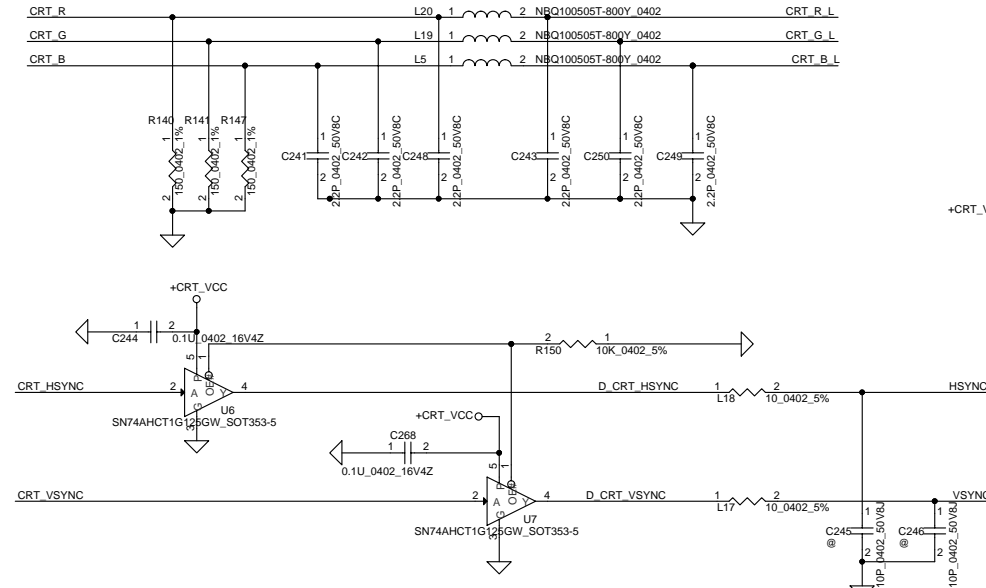
**SCHEMATIC, MB A8868**

# CRT CONNECTOR

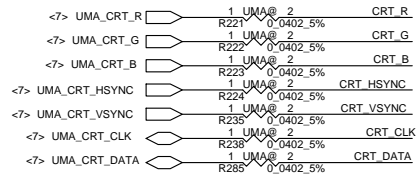
Remove D3-D5 on DVT



Reserve ESD for CRT connector on DVT

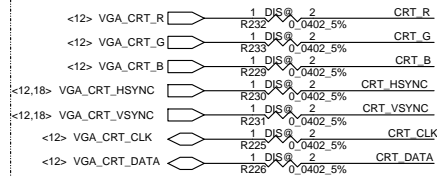


## UMA



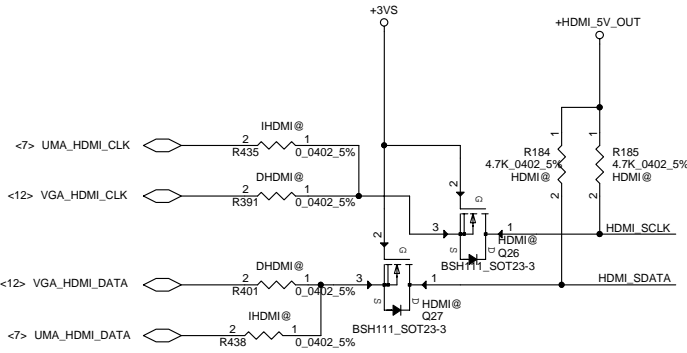
Close to CRT Connector

## DISCRETE



Close to CRT Connector

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				Date:	Saturday, September 07, 2013
				Sheet	20 of 47

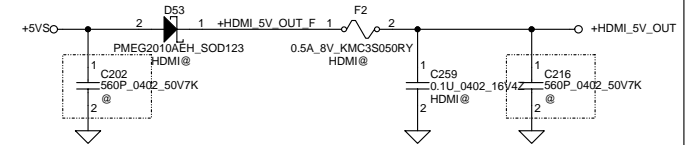
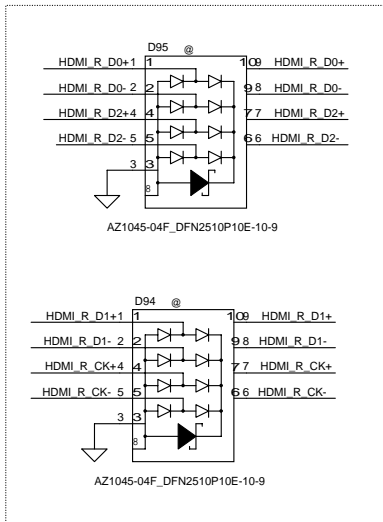
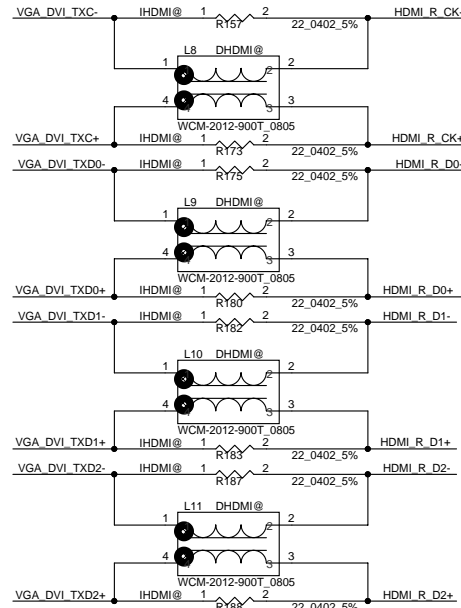
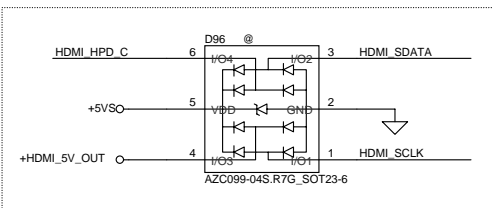


**DISCRETE**

<12> VGA_HDMI_CLK+	CV296	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXC+
<12> VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXC-
<12> VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0+
<12> VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0-
<12> VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1+
<12> VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1-
<12> VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2+
<12> VGA_HDMI_TX2-	CV300	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2-

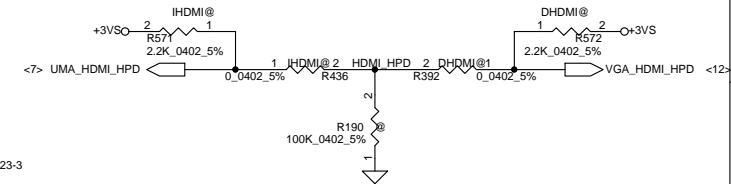
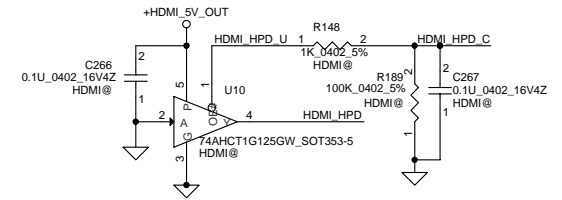
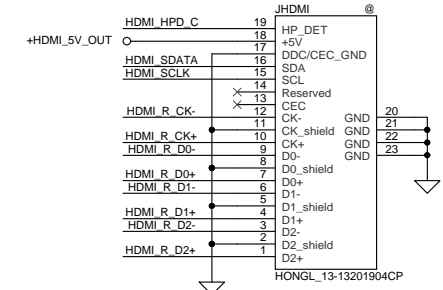
**UMA**

<7> UMA_HDMI_TXC+	C838	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXC+
<7> UMA_HDMI_TXC-	C837	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXC-
<7> UMA_HDMI_TX0+	C843	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD0+
<7> UMA_HDMI_TX0-	C844	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD0-
<7> UMA_HDMI_TX1+	C841	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD1+
<7> UMA_HDMI_TX1-	C842	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD1-
<7> UMA_HDMI_TX2+	C839	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD2+
<7> UMA_HDMI_TX2-	C840	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD2-



4/23 Add C202 and C216 for EMI request

**HDMI Connector**



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Size	Custom	Document Number	4019K4		Rev B
Date:	Saturday, September 07, 2013	Sheet	21	of	47

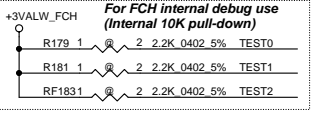
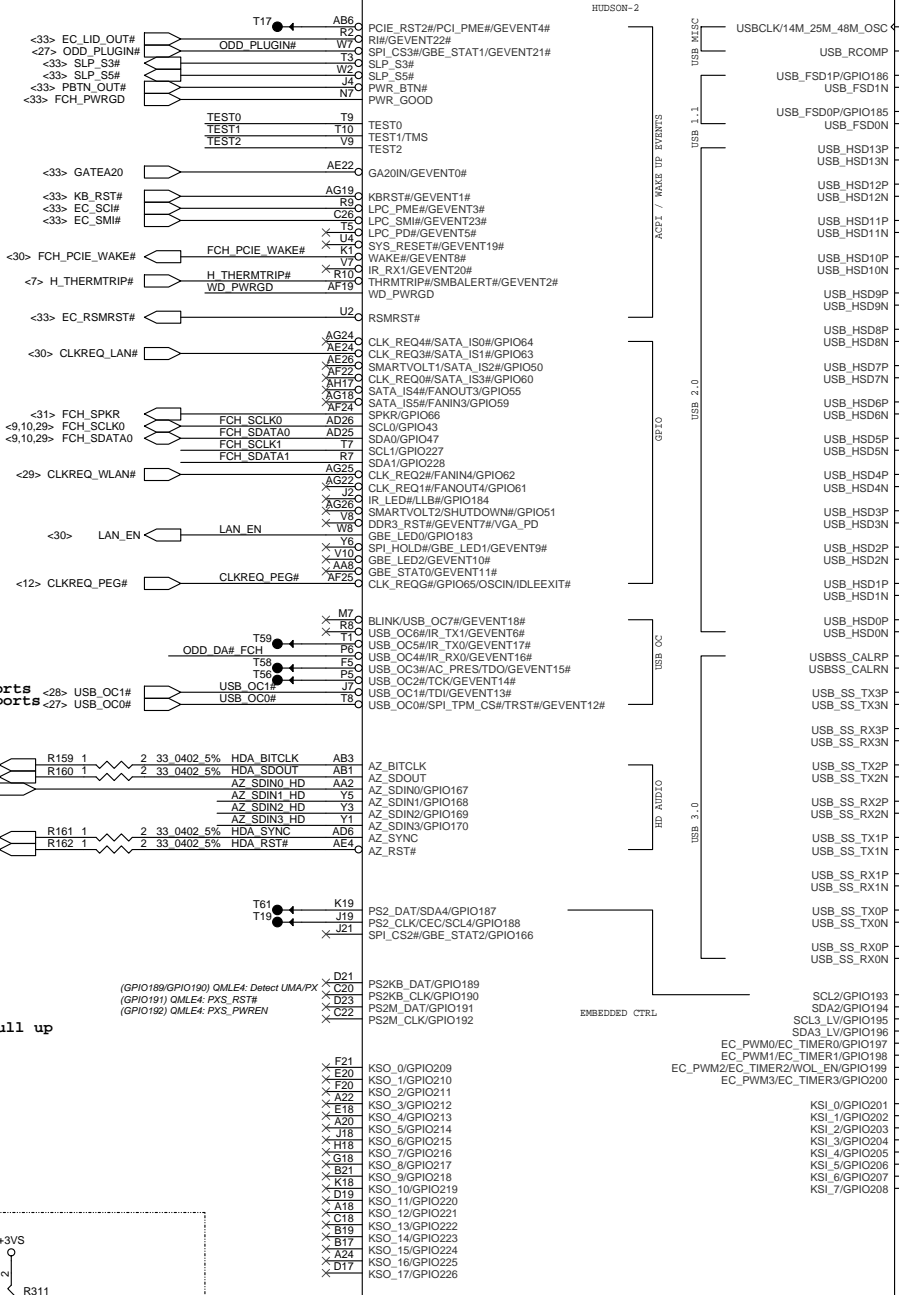
Reserve ESD for HDMI conn. on DVT



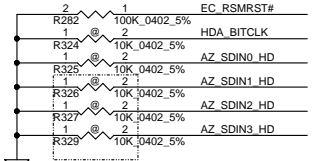


PCIE\_RST2 : Reset PCIE device on Hudson 3

U2D

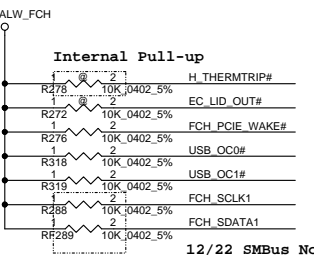


SM Bus 0 -> S0 PWR domain => SO-DIMM, WLAN  
SM Bus 1 -> S5 PWR domain => no use

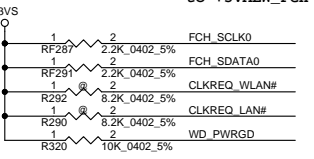


12/22 Reserve R326, R327, R329 but AMD have internal pull down

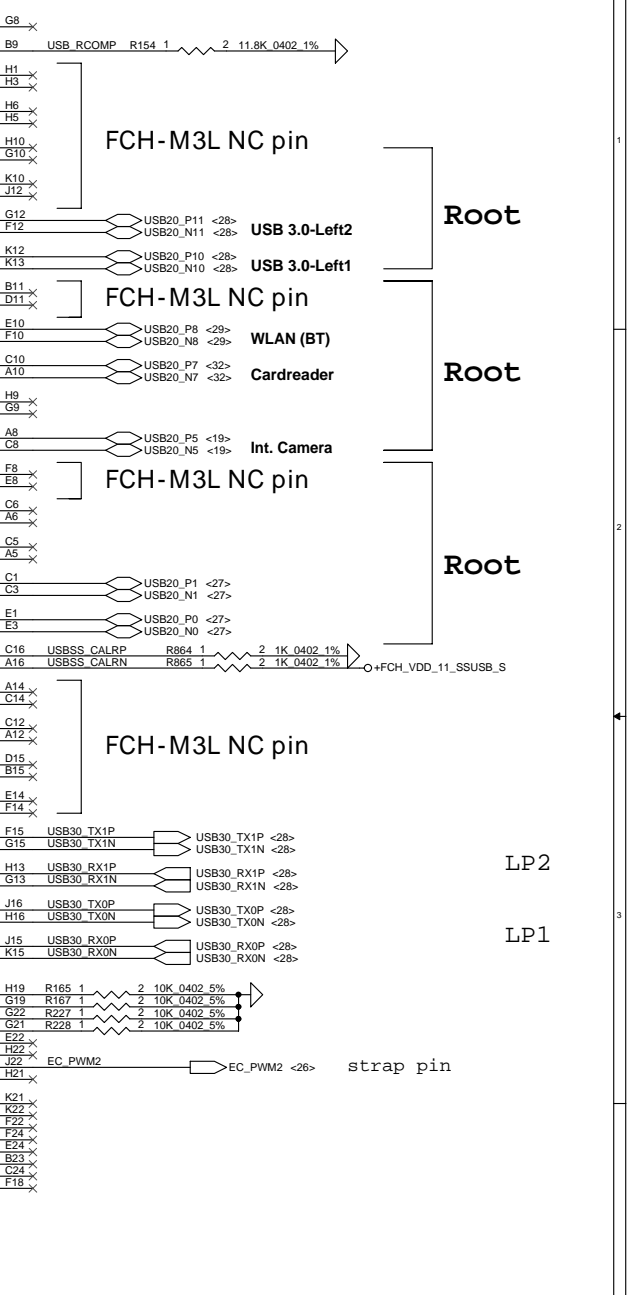
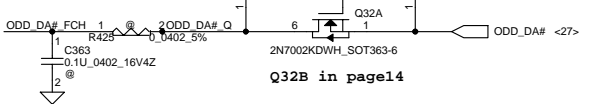
USB\_OC1# is for left USB3.0 ports <28>: USB\_OC1#  
USB\_OC0# is for right USB2.0 ports <27>: USB\_OC0#



12/22 SMBus Not Implemented use 10k pull up to +3VALW\_PCH



Place R425 and C363 close to FCH for ESD

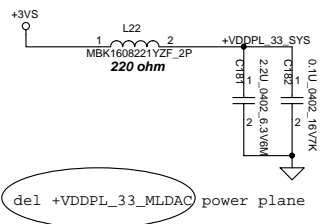


218-0755091 A13 HUDSON-M3L FCBCGA 656P C38

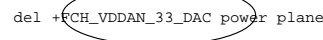
M3LR1@

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Rev	Document Number	Date	Sheet	47
B	4019K4	Saturday, September 07, 2013	24	47

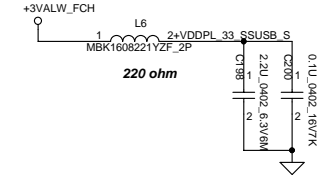




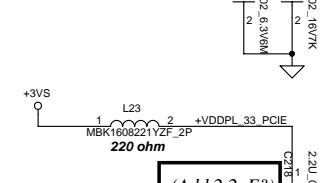
del +VDDPL\_33\_ML DAC power plane



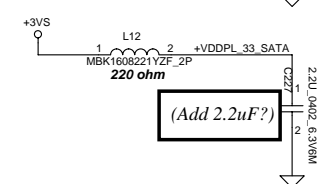
del +FCH\_VDDAN\_33\_DAC power plane



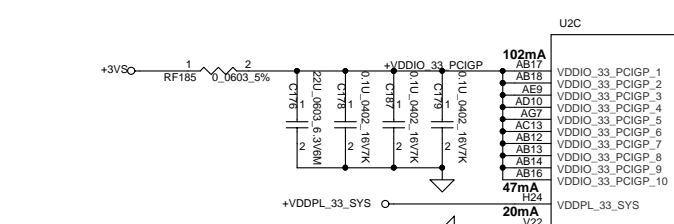
Check Caps



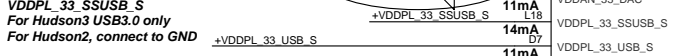
(Add 2.2uF?)



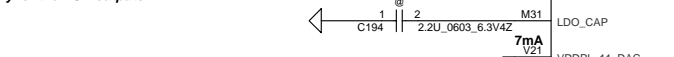
(Add 2.2uF?)



demo board connect to GND



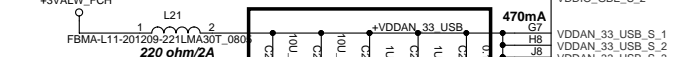
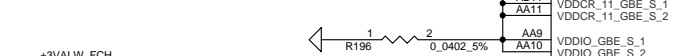
VDDPL\_33\_SSUSB\_S For Hudson3 USB3.0 only For Hudson2, connect to GND



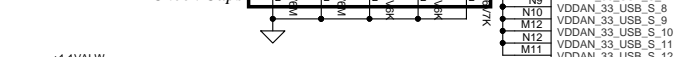
LDO\_CAP: Internally generated 1.8V supply for the RGB outputs



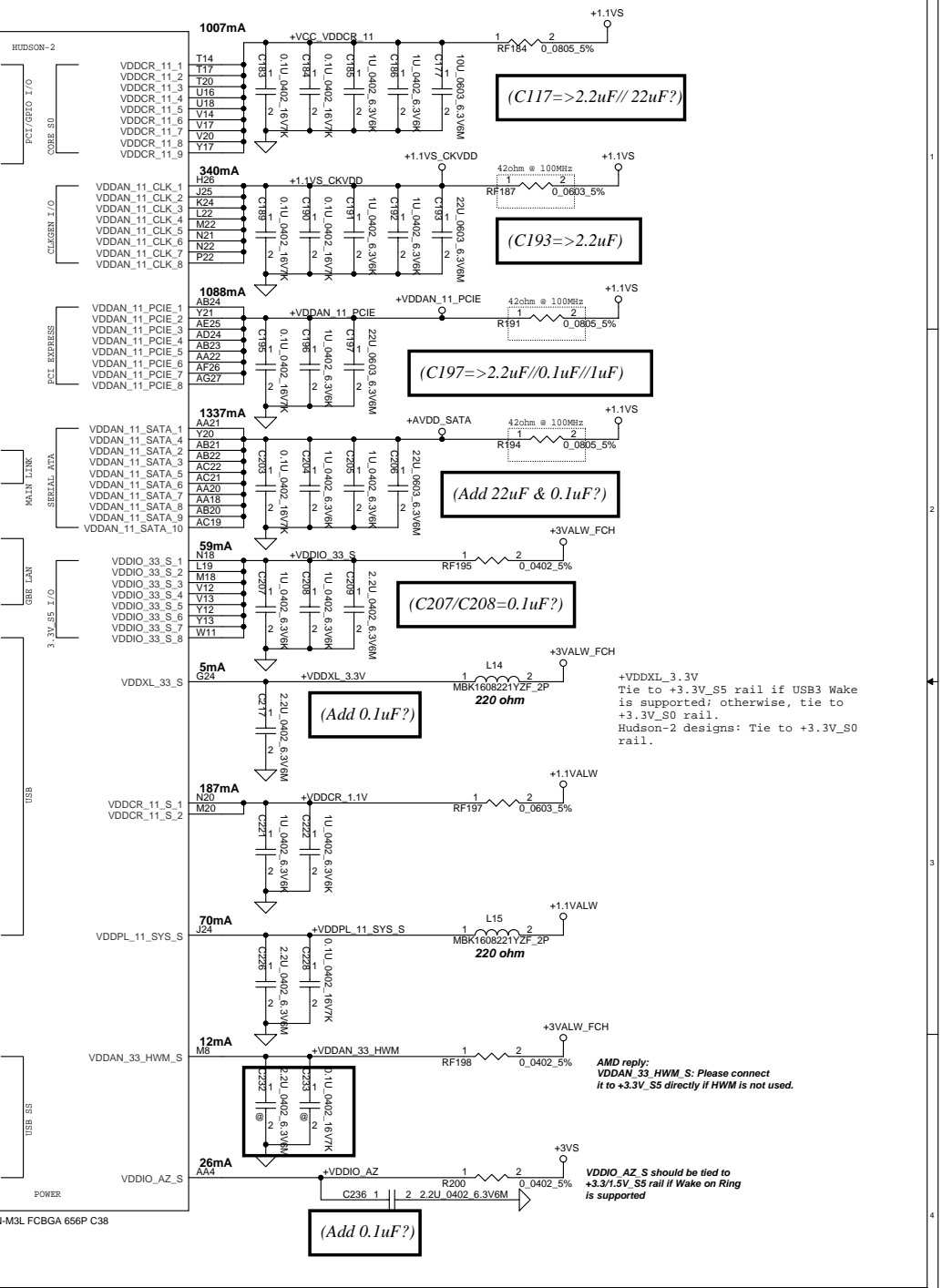
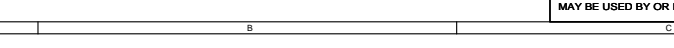
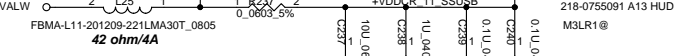
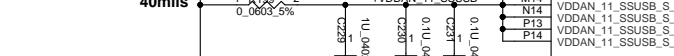
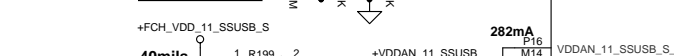
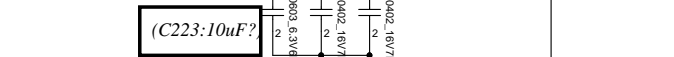
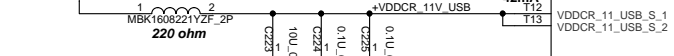
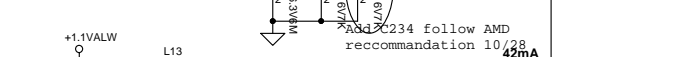
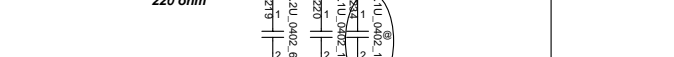
demo board connect to GND



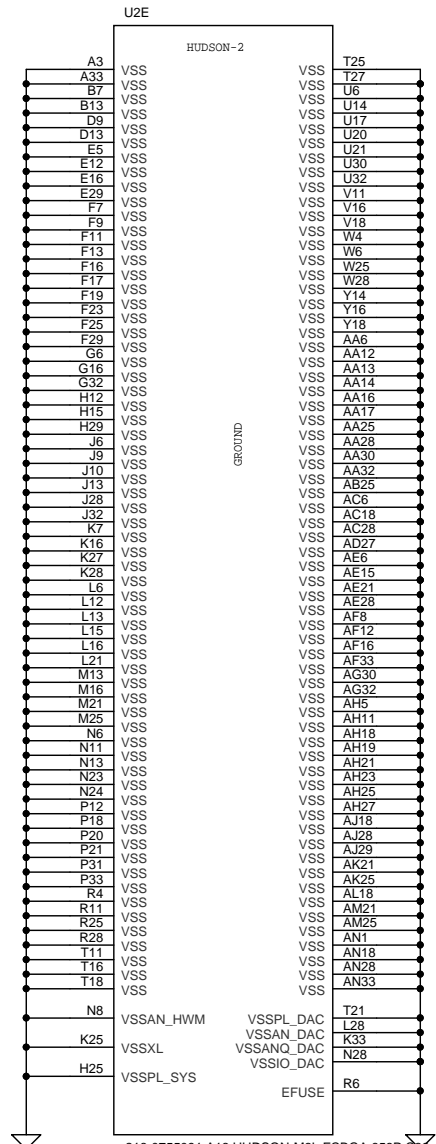
reccomendation 10/28



(C223: 10uF?)



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Document Number	4019K4		Date	Saturday, September 07, 2013
Rev	B		Sheet	25 of 47



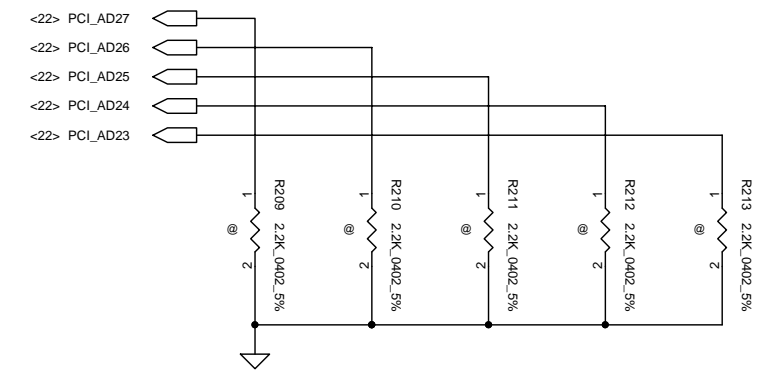
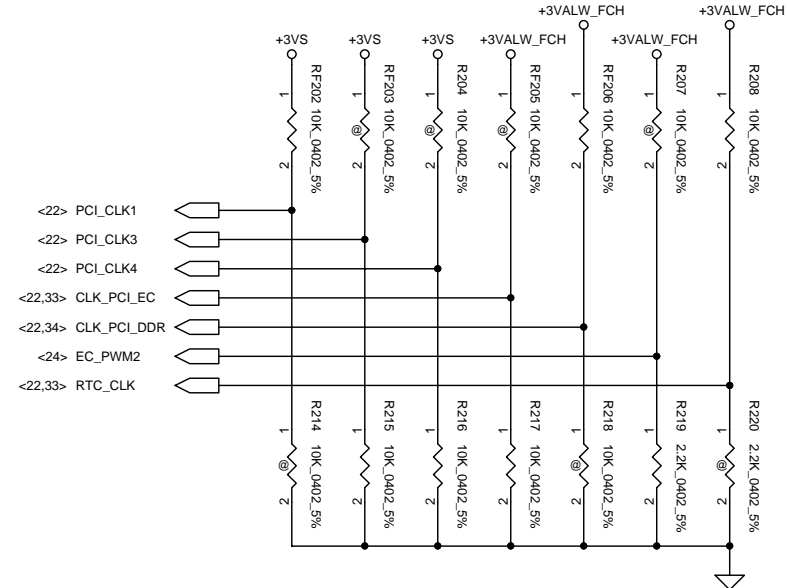
## STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

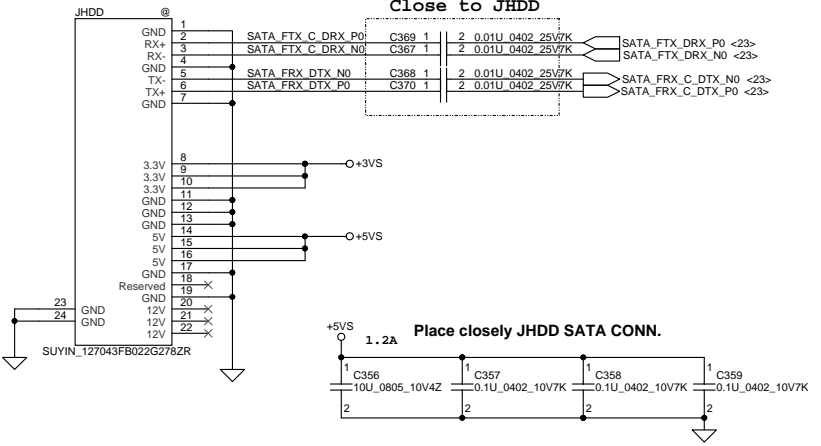


218-0755091 A13 HUDSON-M3L FCBGA 656P C36

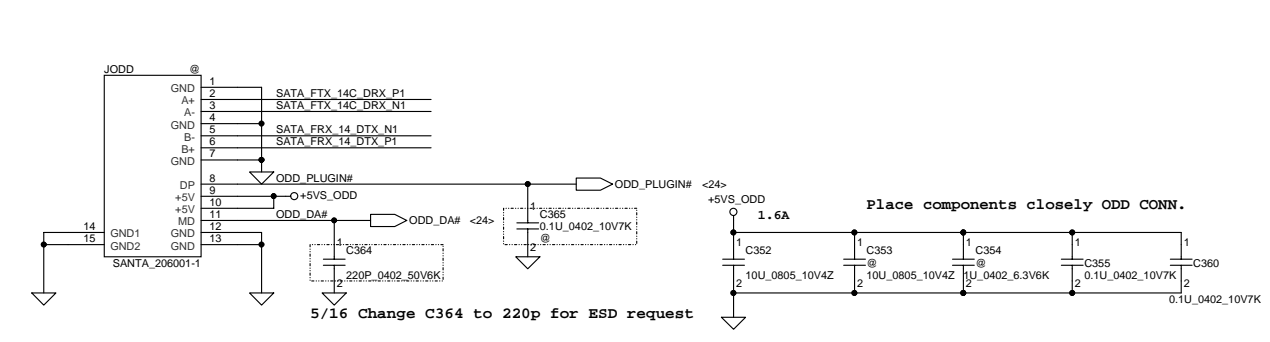
M3LR1@

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Document Number	4019K4			Rev	B
Date:	Saturday, September 07, 2013	Sheet	26	of	47

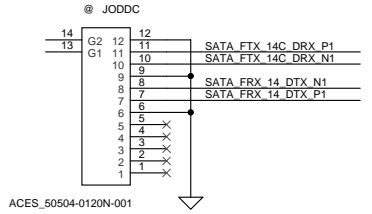
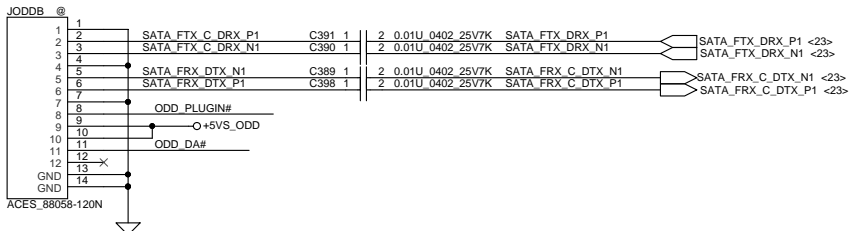
### SATA HDD Conn.



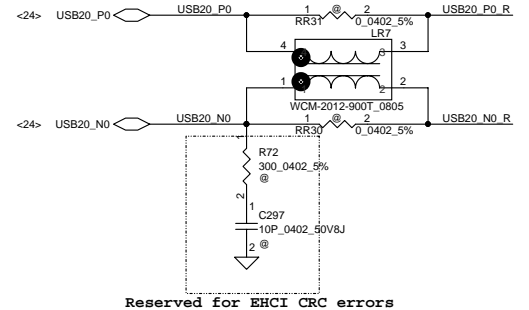
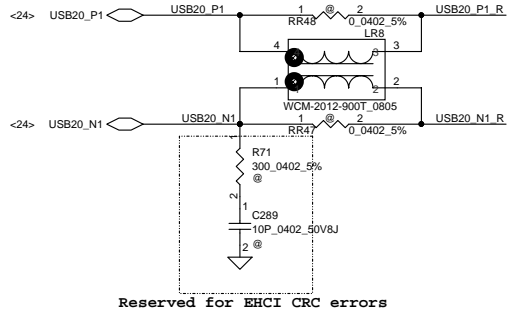
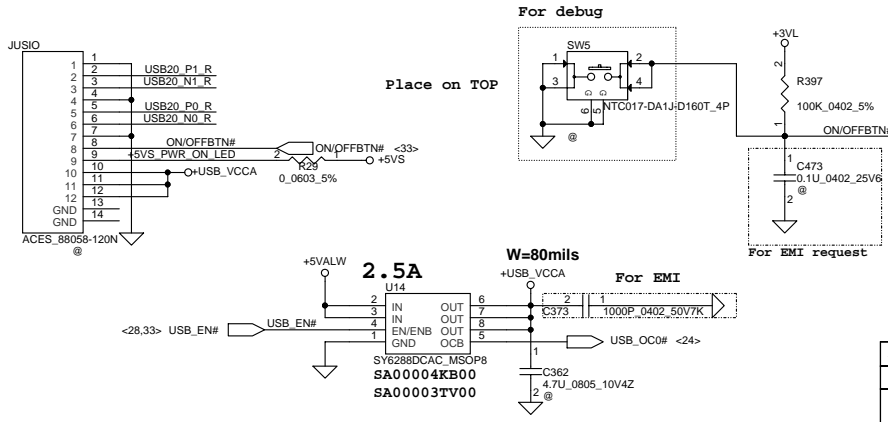
### SATA ODD Conn (for 14")



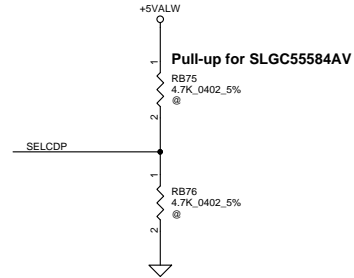
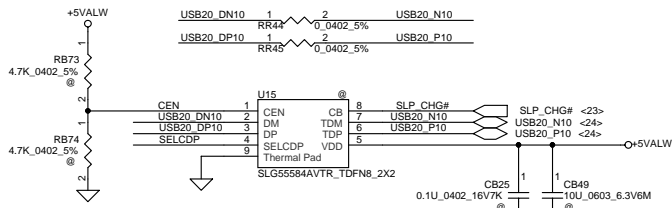
### SATA ODD Conn (for 15")



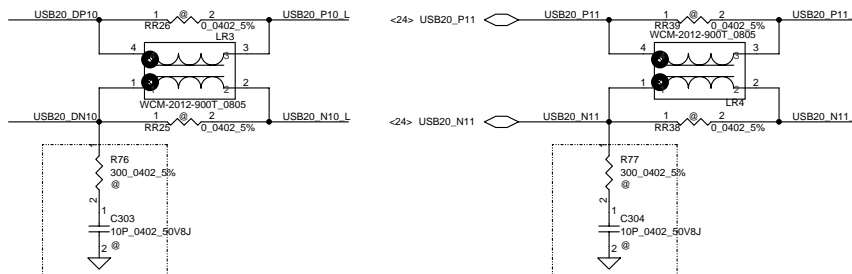
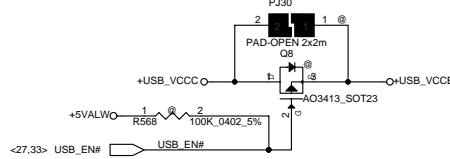
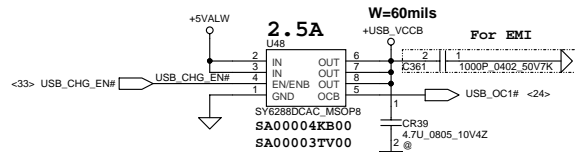
### Power Button & RUSB connector



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Date			Saturday, September 07, 2013		Sheet 27 of 47

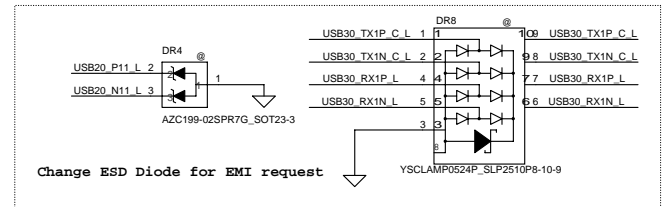
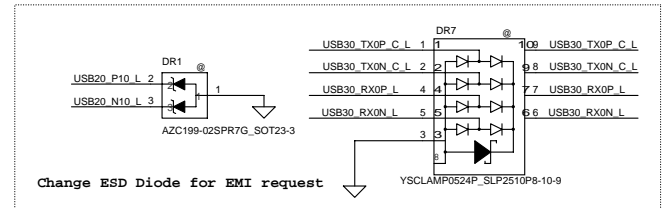
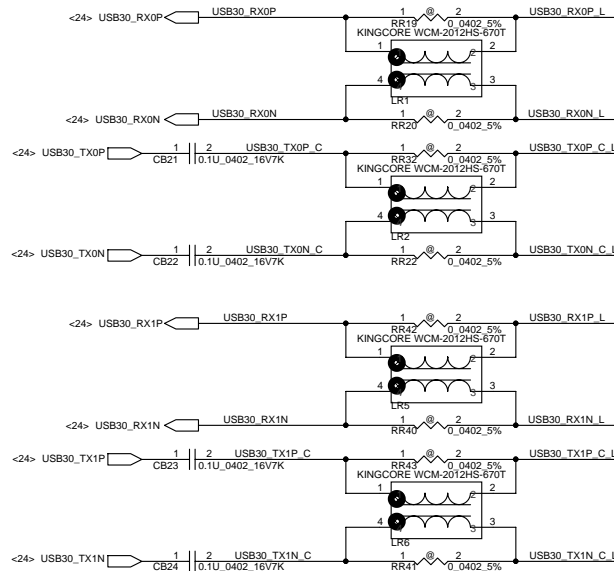
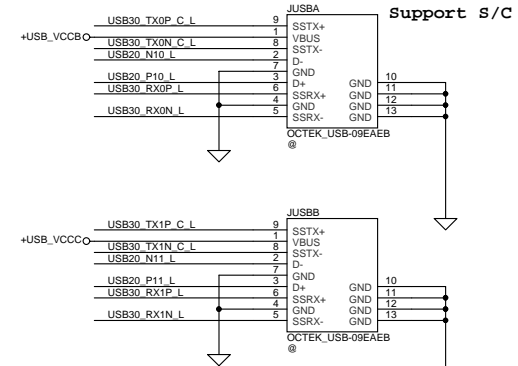
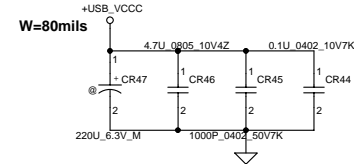
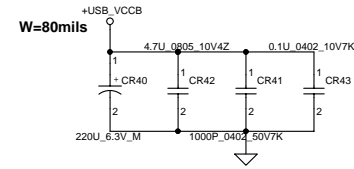


SLP_CHG#	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only

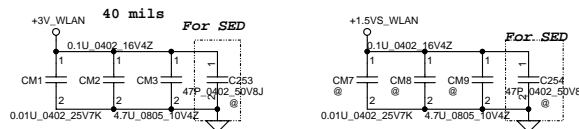


Reserved for EHCI CRC errors

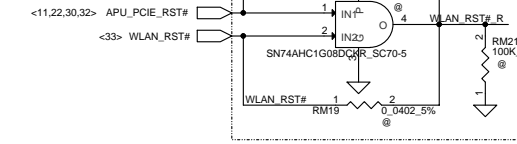
Reserved for EHCI CRC errors



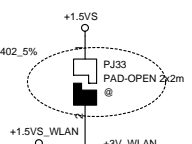
# Slot 1 Half PCIe Mini Card-WLAN



Add WLAN\_RST# on DVT



4/23 Add RM20 and change UM5, RM21 to @



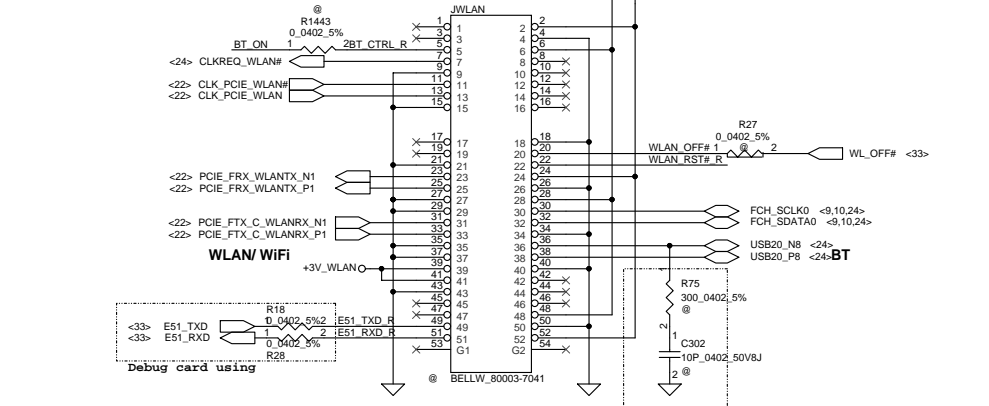
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L

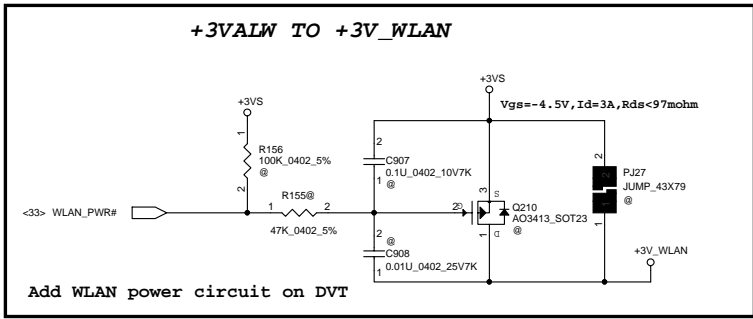
  

<33> BT\_ON 1 R328 2 E51\_RXD R  
1K\_0402\_5%

For isolate BT\_CTRL and Compal Debug Card.

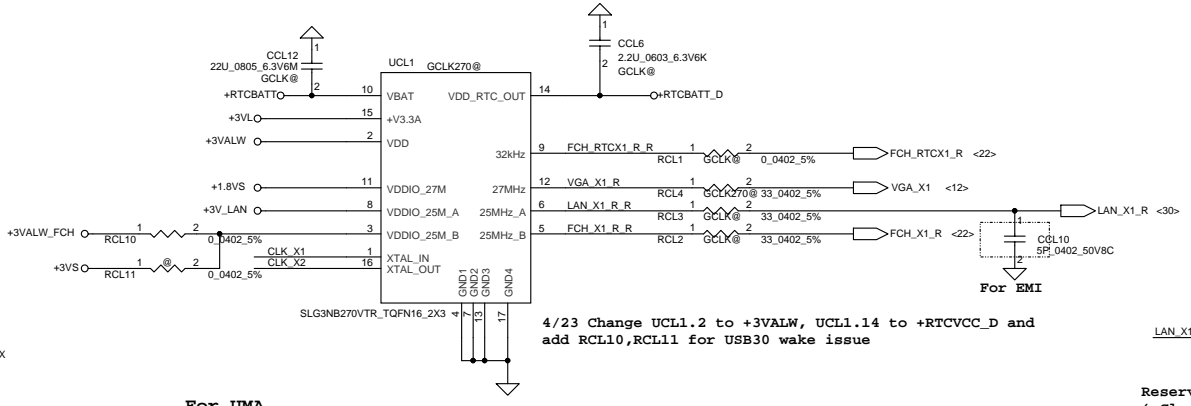
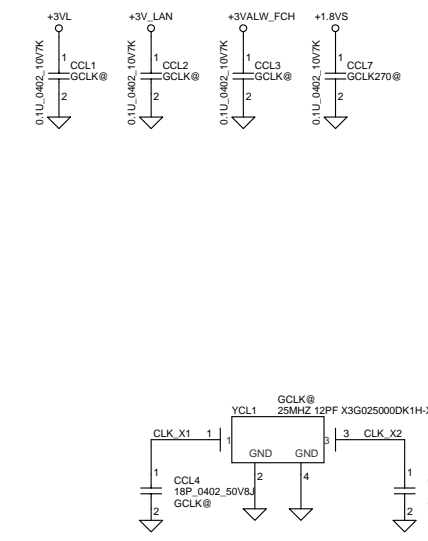


Change JWLAN symbol to SP07000TB00 on DVT  
Reserved for EHCI CRC errors



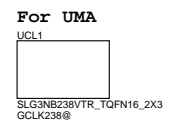
4/23 Change R156, R155, C907, C908, Q210 to @

## Green Clock Generator



4/23 Change UCL1.2 to +3VALW, UCL1.14 to +RTC\_VCC\_D and add RCL10, RCL11 for USB30 wake issue

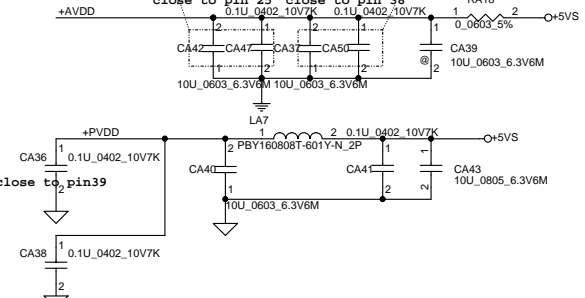
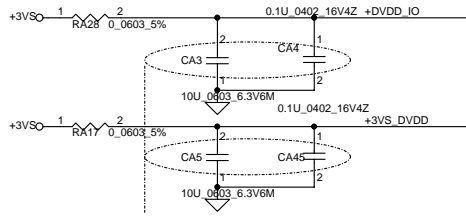
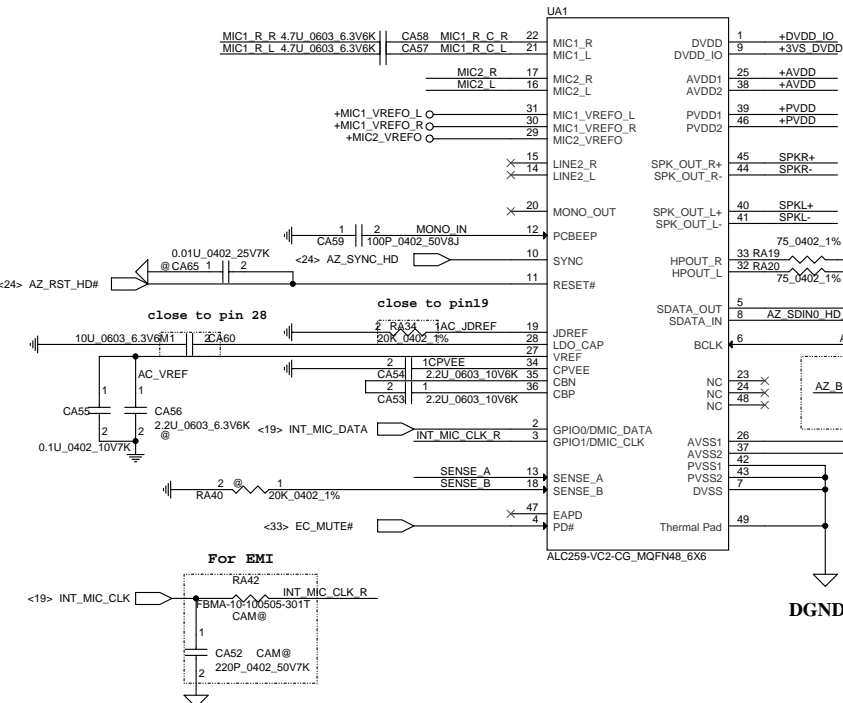
LAN\_X1\_R R R 1 @ 2 0.0402\_5%  
Reserved for Swing Level adjustment (Close GCLK side)



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Date	Saturday, September 07, 2013	Sheet	29	of	47	



**35mA for 3.3V level**

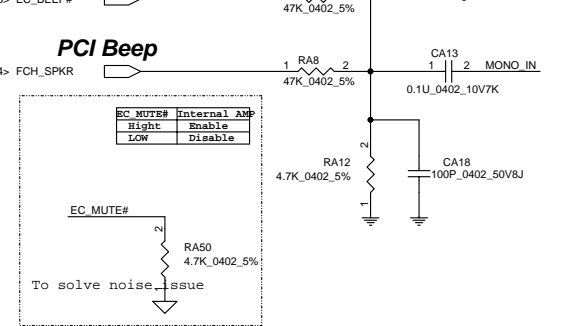


place close to chip

For EMI please place near codec

**EC BEEP**

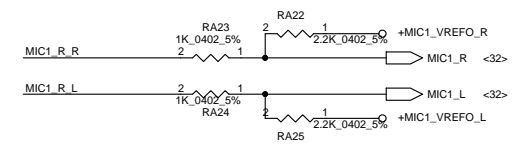
**Beep sound**



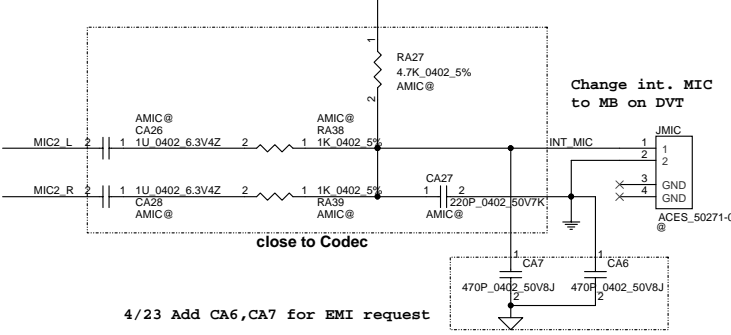
EC MUTE#	Internal Amp
High	Enable
LOW	Disable

To solve noise issue

**Ext.MIC/LINE IN JACK**



**Analog MIC**

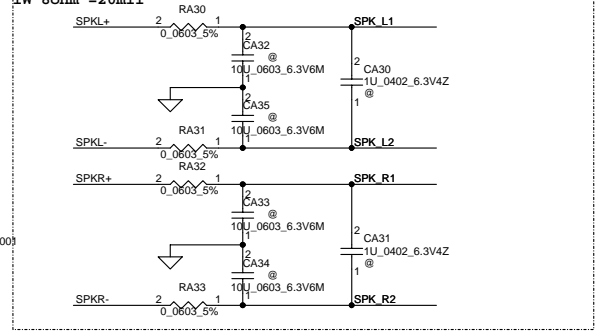


Change int. MIC to MB on DVT

close to Codec

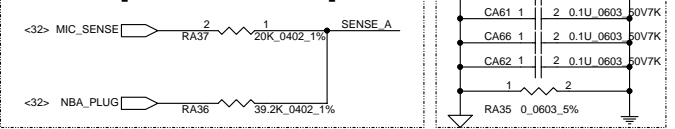
4/23 Add CA6,CA7 for EMI request

**placement near Audio Codec**

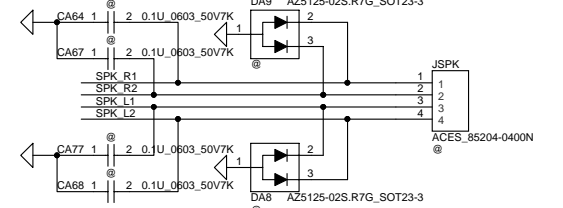


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	

place close to chip

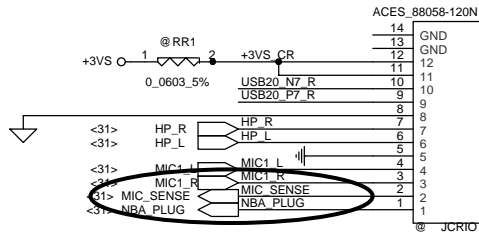


**SPK Conn. 4/23 Add CA64,CA67,CA68,CA77 for EMI request**

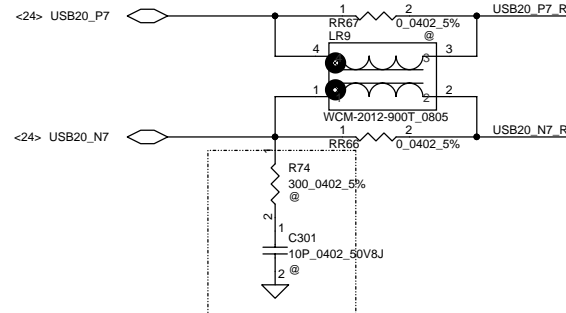


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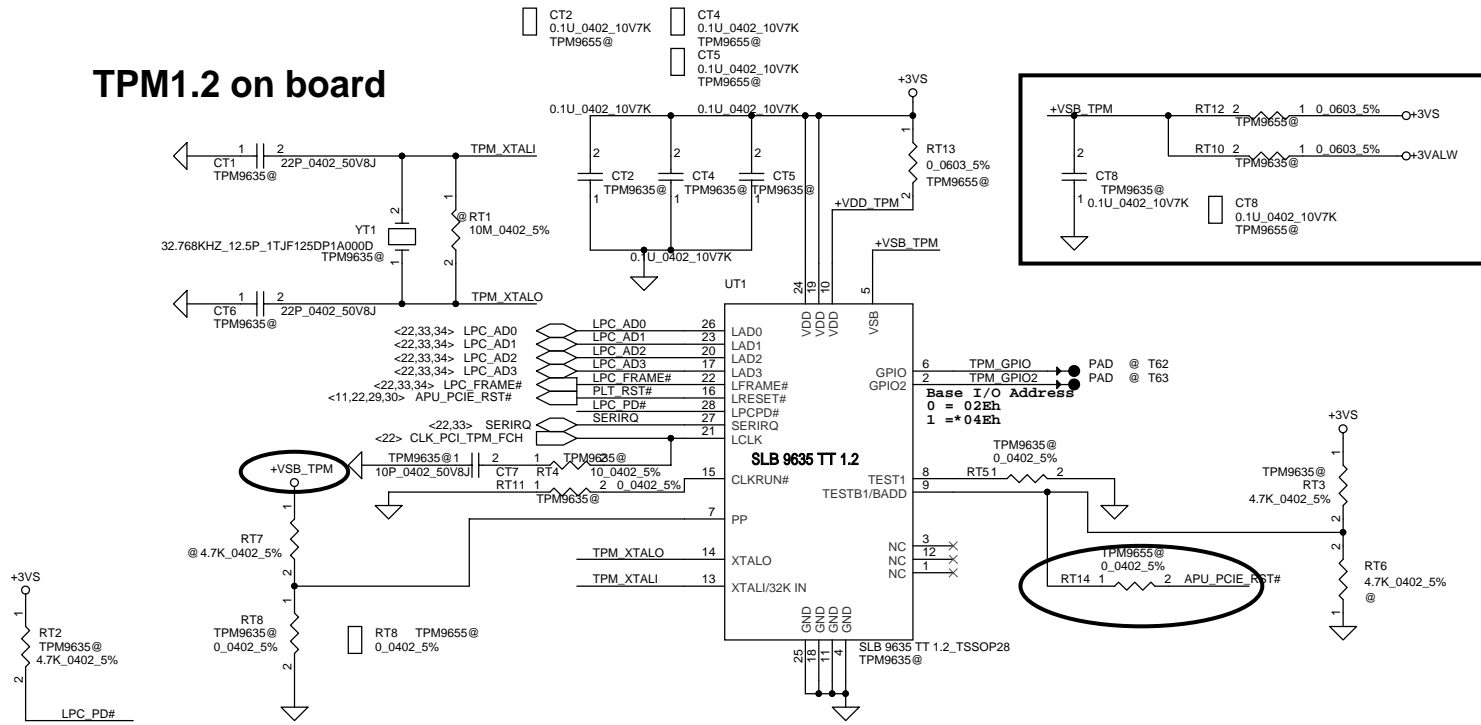
# CardReader Conn.



Update JCRIO pin definition on DVT

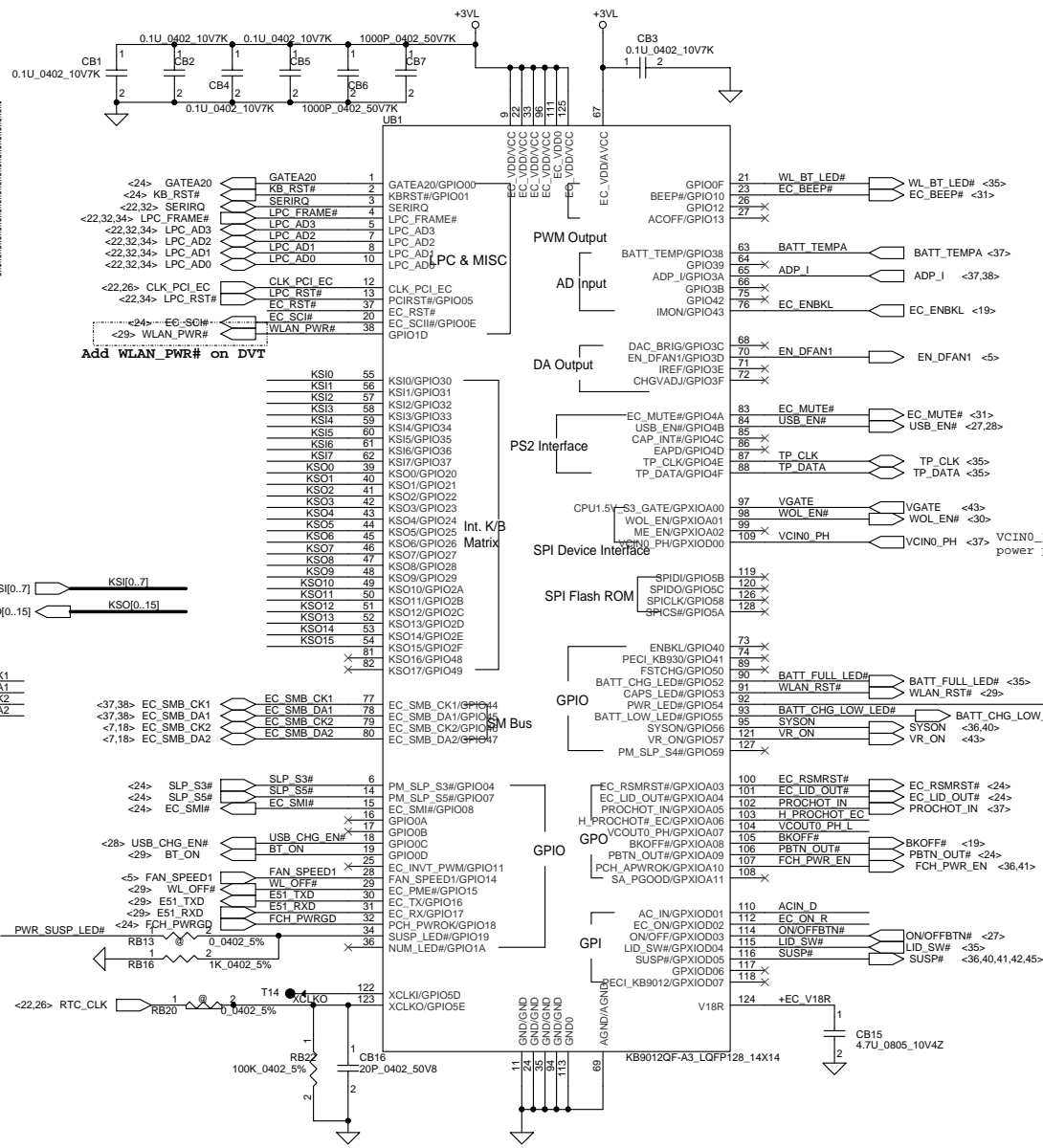
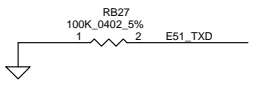
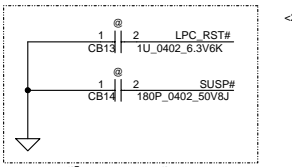
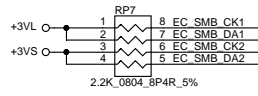
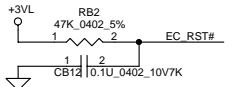
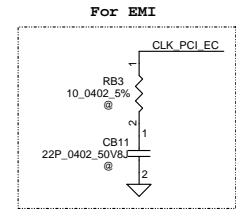


# TPM1.2 on board



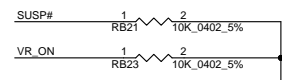
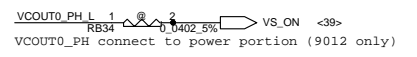
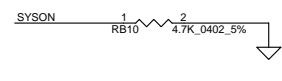
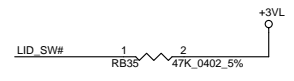
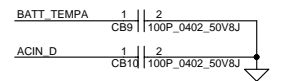
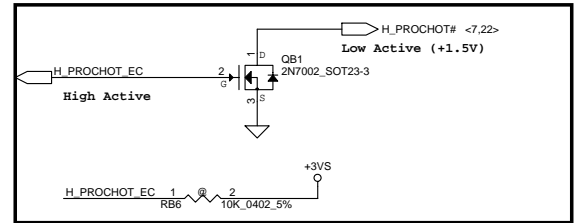
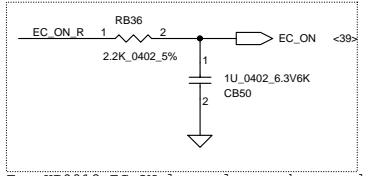
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				4019K4	
Date:				Saturday, September 07, 2013	Sheet 32 of 47





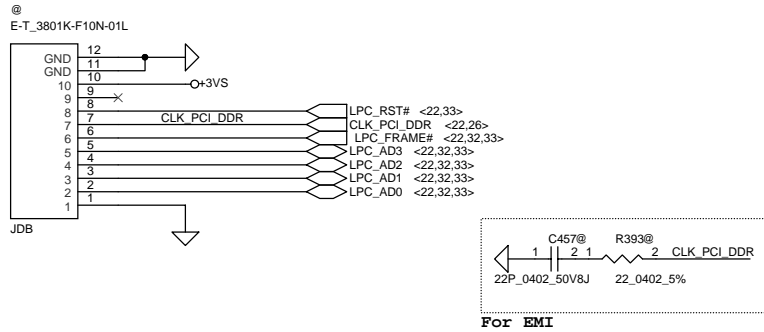
**Voltage Comparator Pins FOR 9012 A3**

VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102	HIGH	LOW
VCCOUT0 pin104	HIGH	LOW
VCCOUT1 pin103	LOW	HIGH



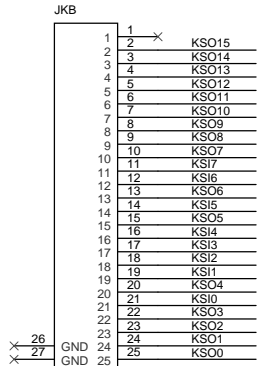
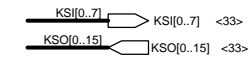
# LPC Debug Port

Place the PAD under DDR DIMM.



For EMI

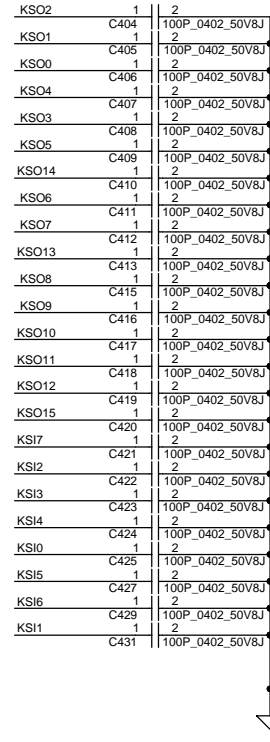
# KEYBOARD CONN.



ACES\_50524-02501-001  
@

For EMI

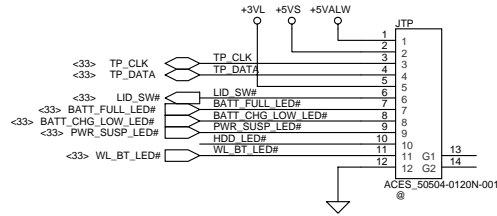
Close to JKB



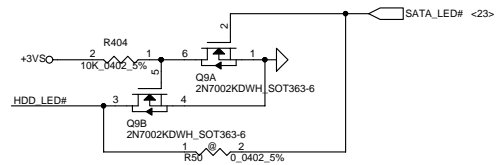
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				4019K4	
Date:		Saturday, September 07, 2013		Sheet	34 of 47

# Touchpad Connector

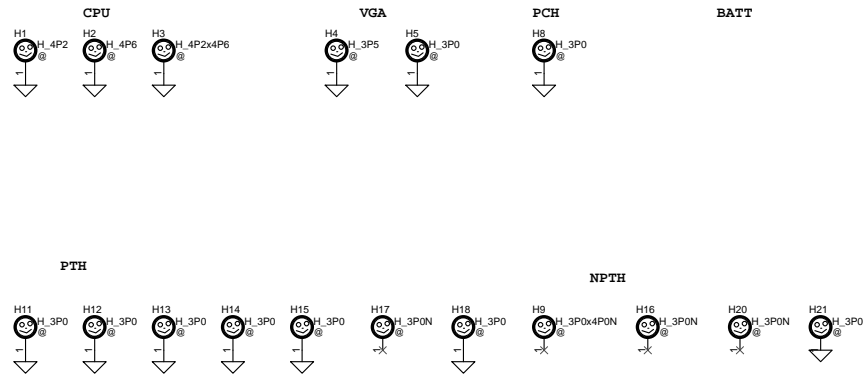
(Reserve 7 pins for LED & Win8 TP)



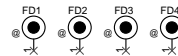
## HDD LED



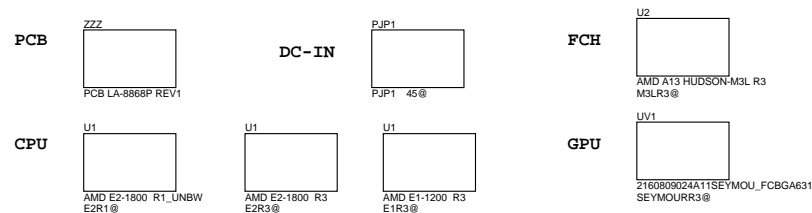
## Screw Hole



## PCB Federal Mark PAD

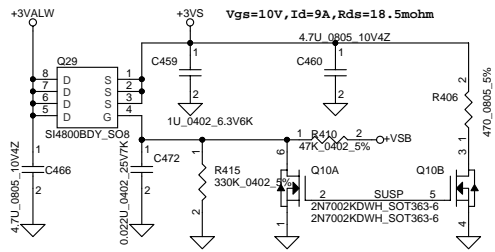


## ISPD

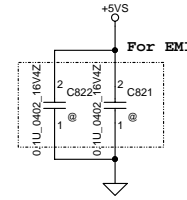
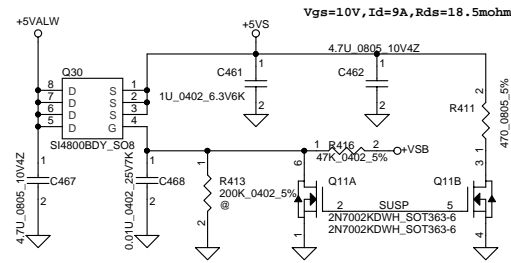


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Size	Document Number	Rev		
	4019K4	B		
Date:	Saturday, September 07, 2013	Sheet	35	of 47

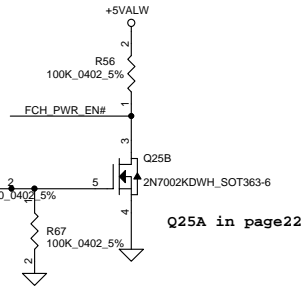
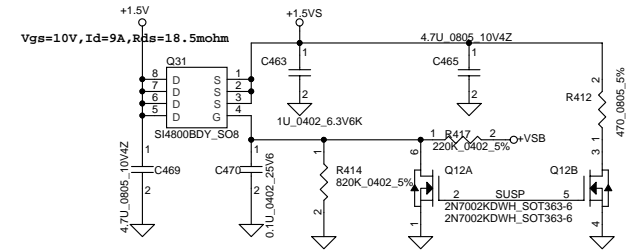
**+3VALW TO +3VS**



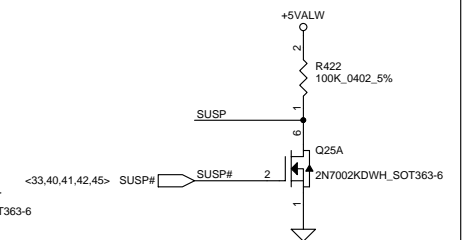
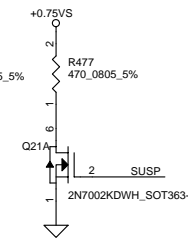
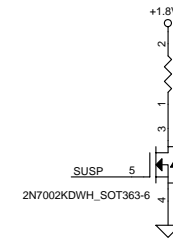
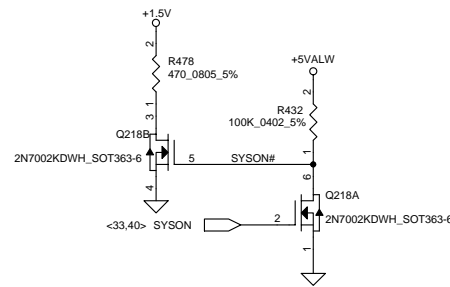
**+5VALW TO +5VS**



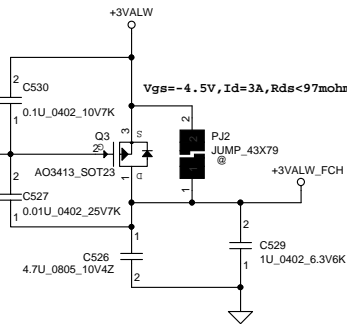
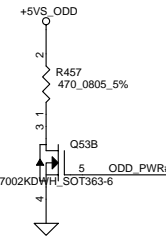
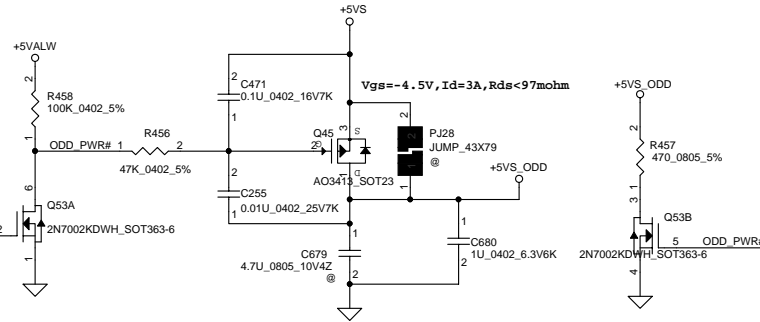
**+1.5V to +1.5VS**



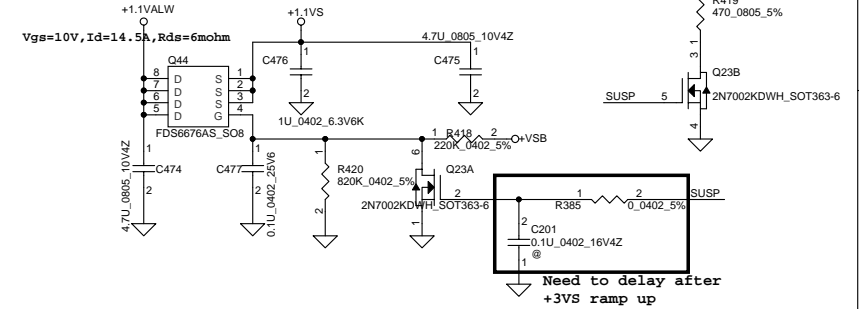
Q25A in page22



**+5VS TO +5VS\_ODD**

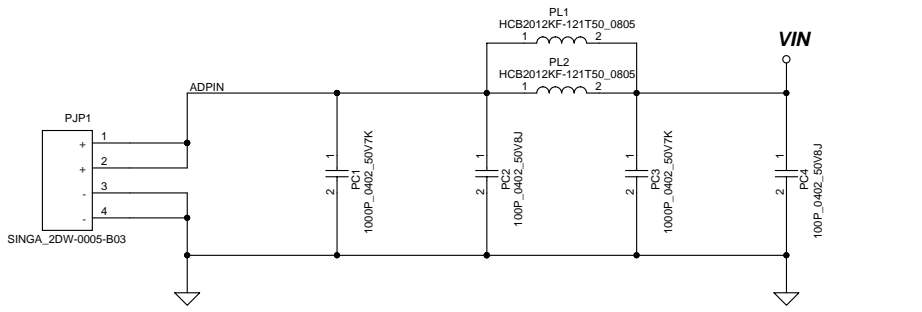


**+1.1VALW to +1.1VS**



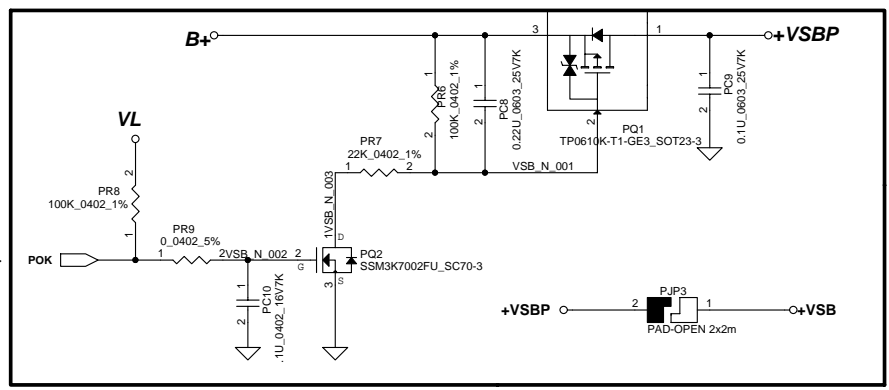
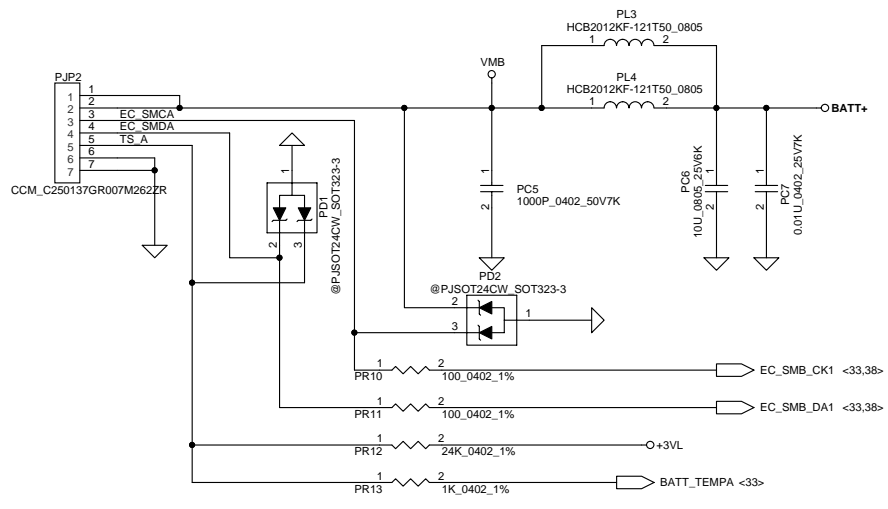
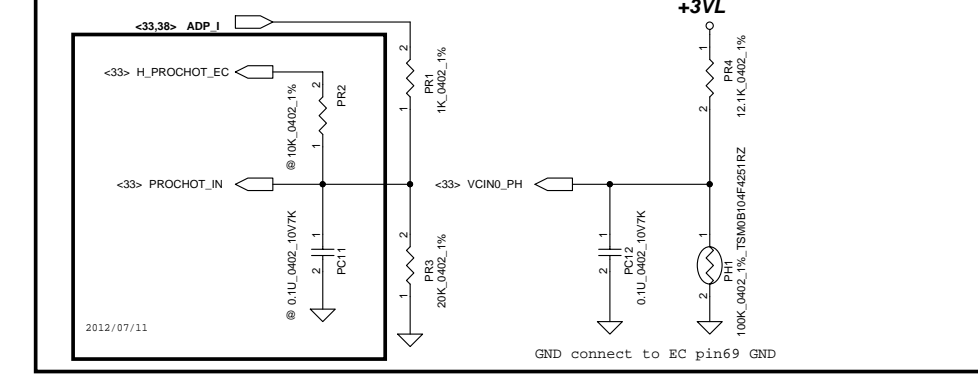
Need to delay after +3VS ramp up

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				4019K4	B
Date: Saturday, September 07, 2013				Sheet	36 of 47

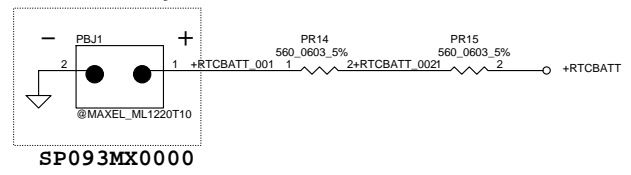


**PH1 under CPU bottom side :**  
**CPU thermal protection at 93 +3 degree C**  
**Recovery at 56 +3 degree C**

Please locate these parts  
 Near EC chip

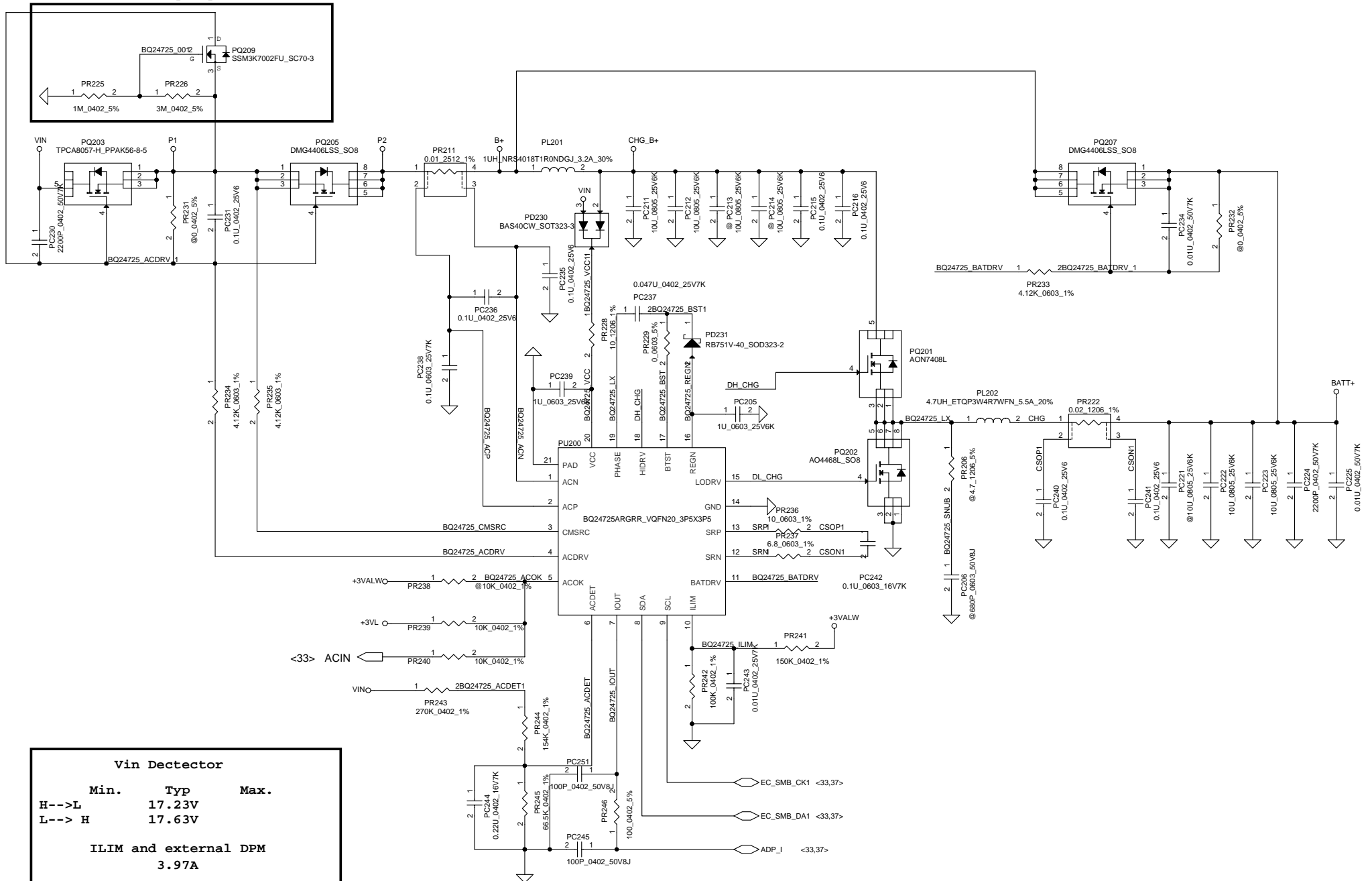


**RTC Battery**

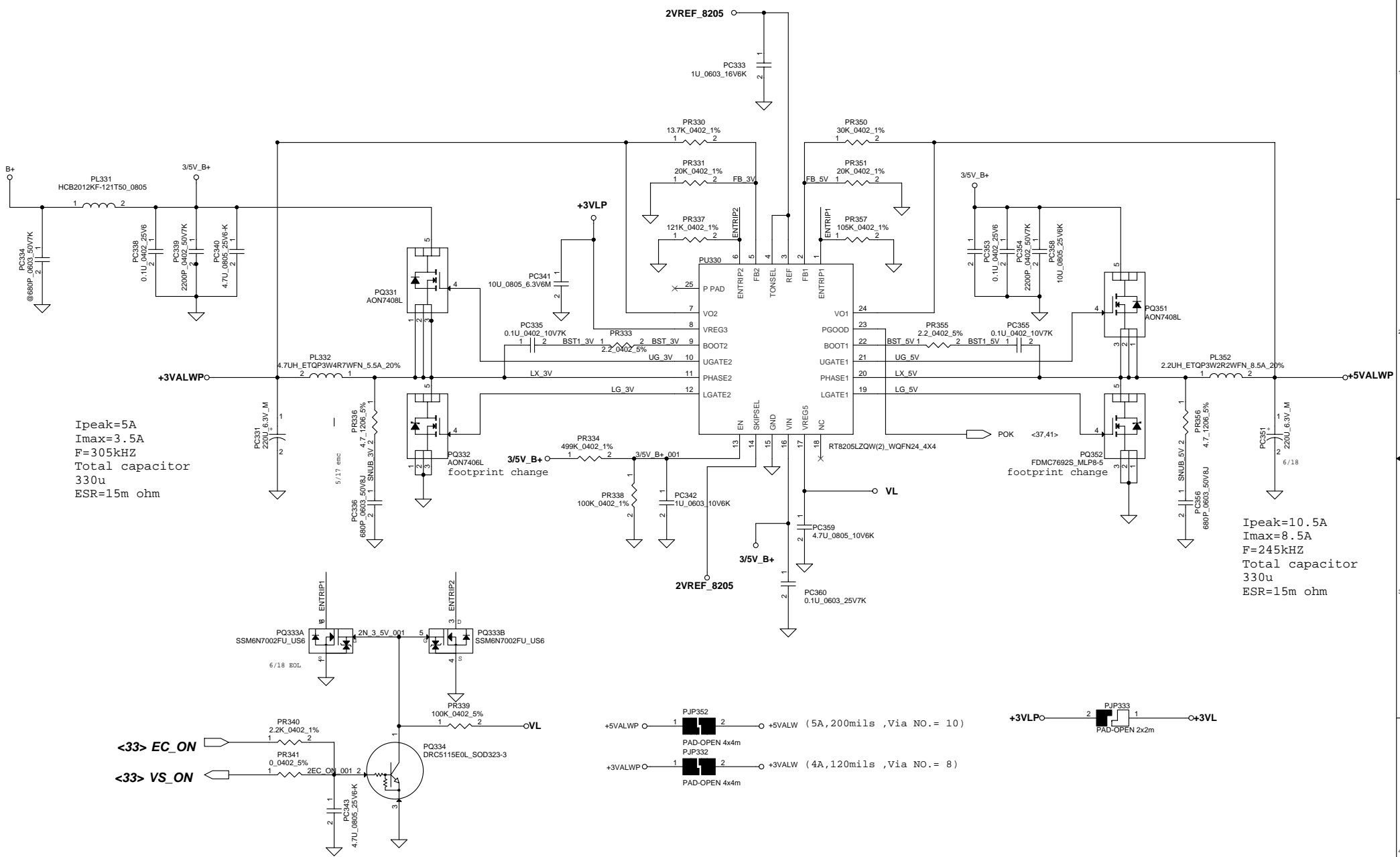


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Date: Saturday, September 07, 2013				Sheet	37 of 47

for reverse input protection

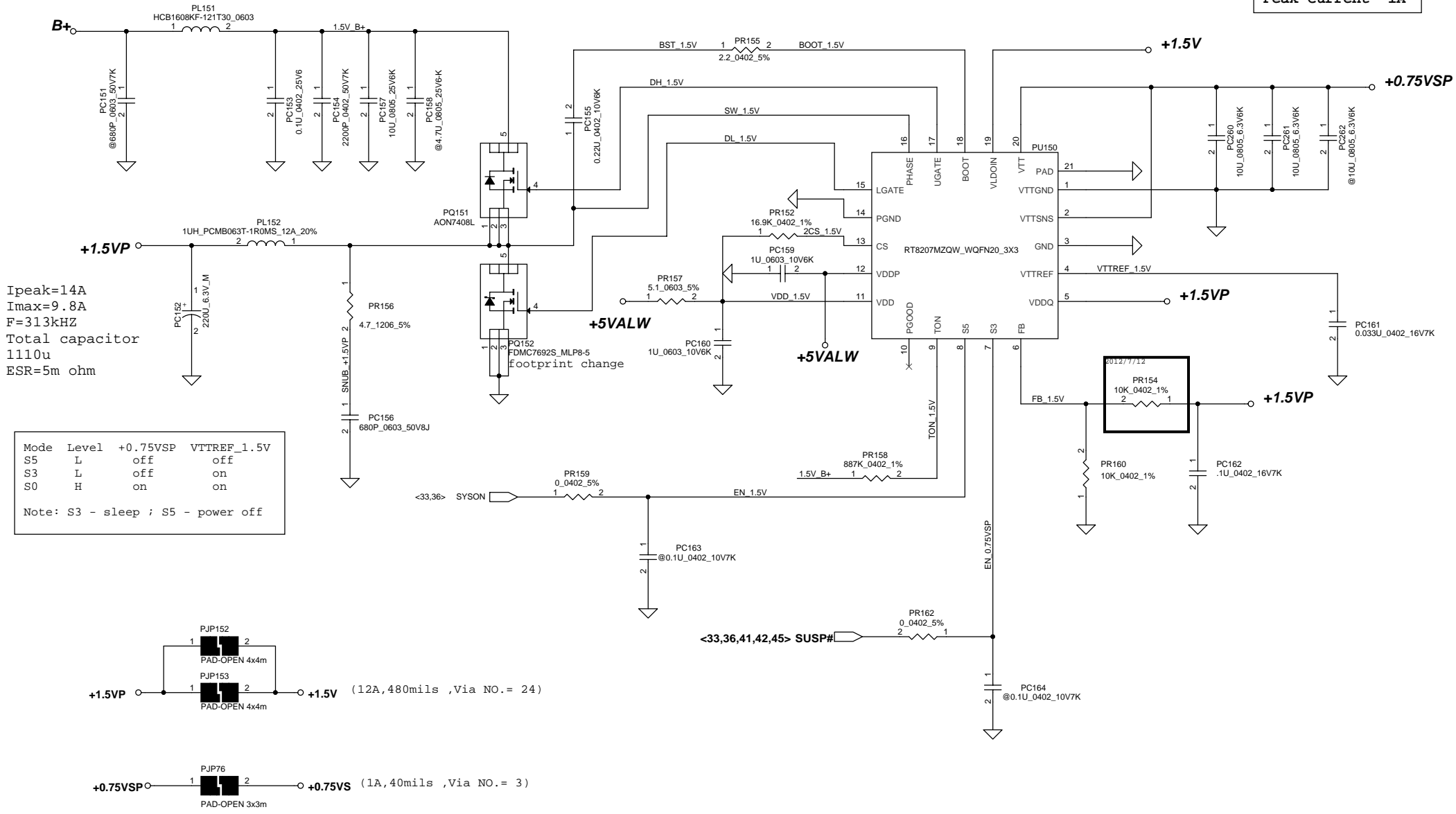


Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
3.97A			



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				4019K4	B
				Date:	Saturday, September 07, 2013 [Sheet 39 of 47

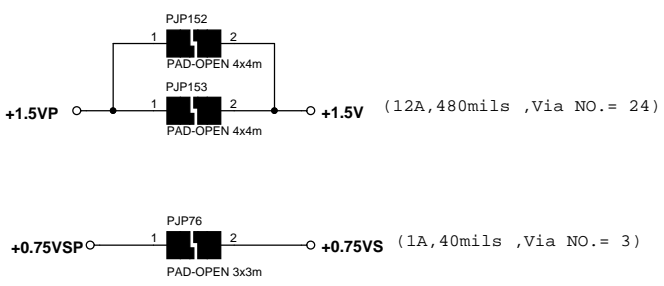
0.75Volt +/- 5%  
TDC 0.7A  
Peak Current 1A



Ipeak=14A  
Imax=9.8A  
F=313kHz  
Total capacitor  
1110u  
ESR=5m ohm

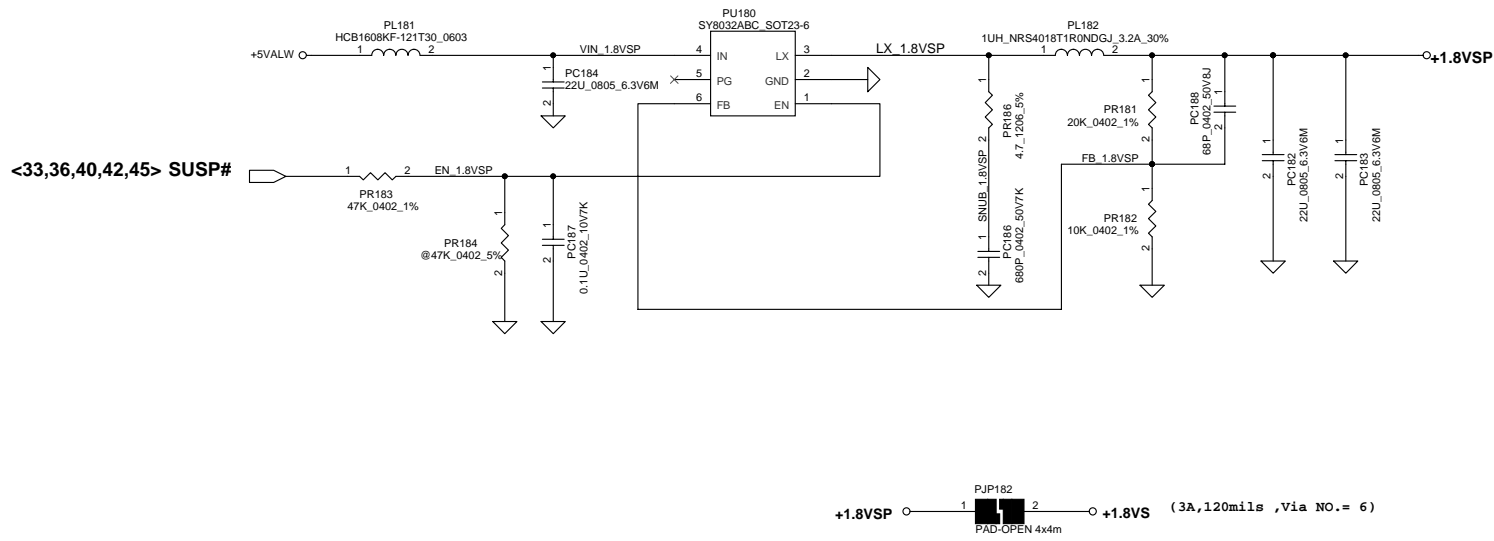
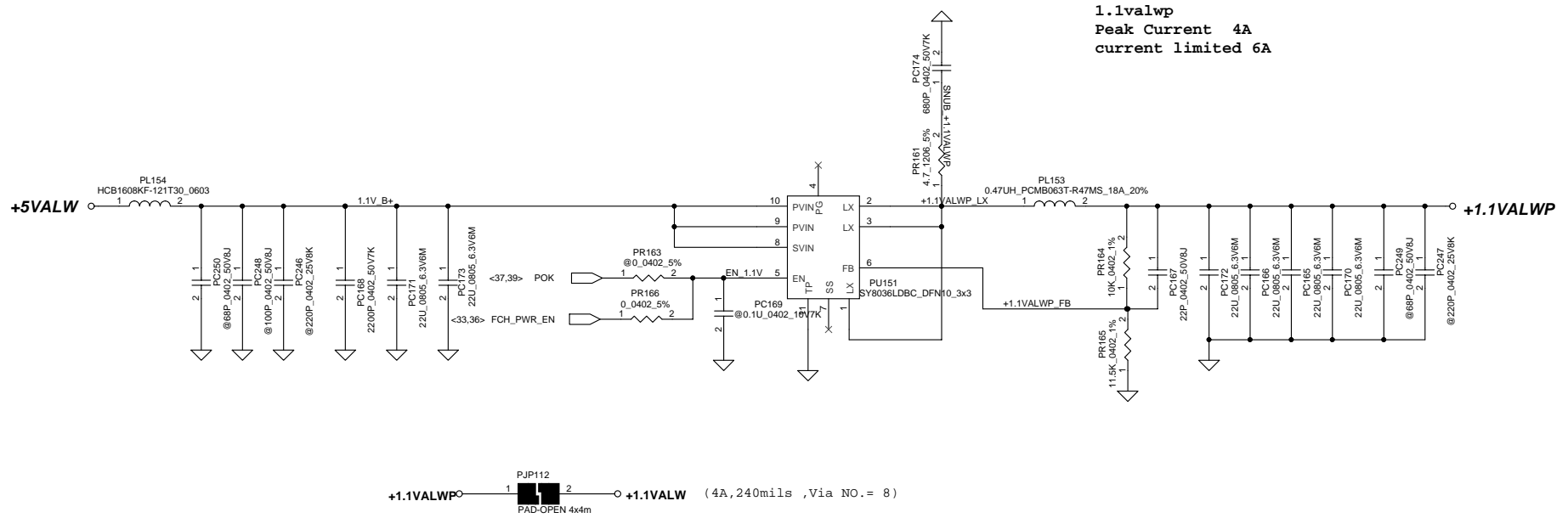
Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

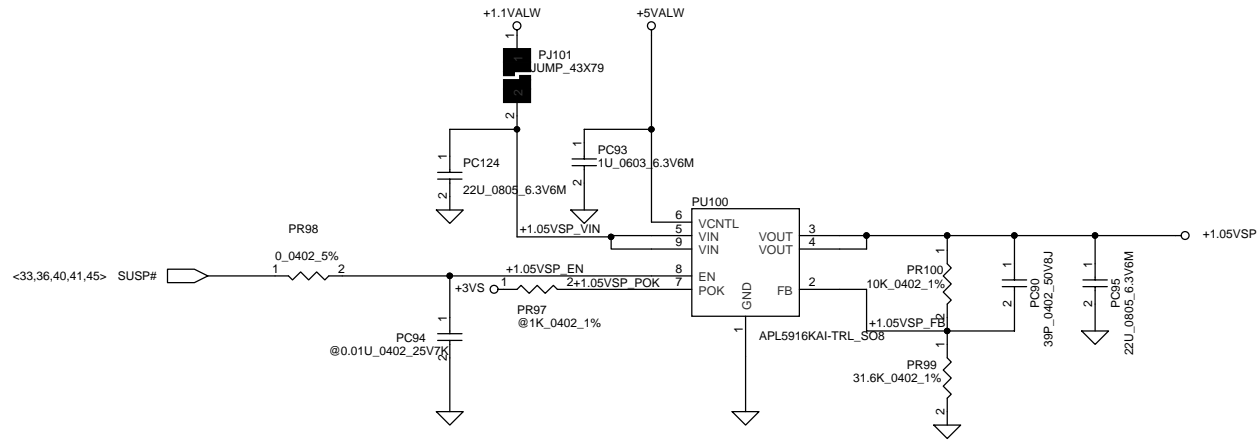


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Date:	Saturday, September 07, 2013	Sheet	40	of	47

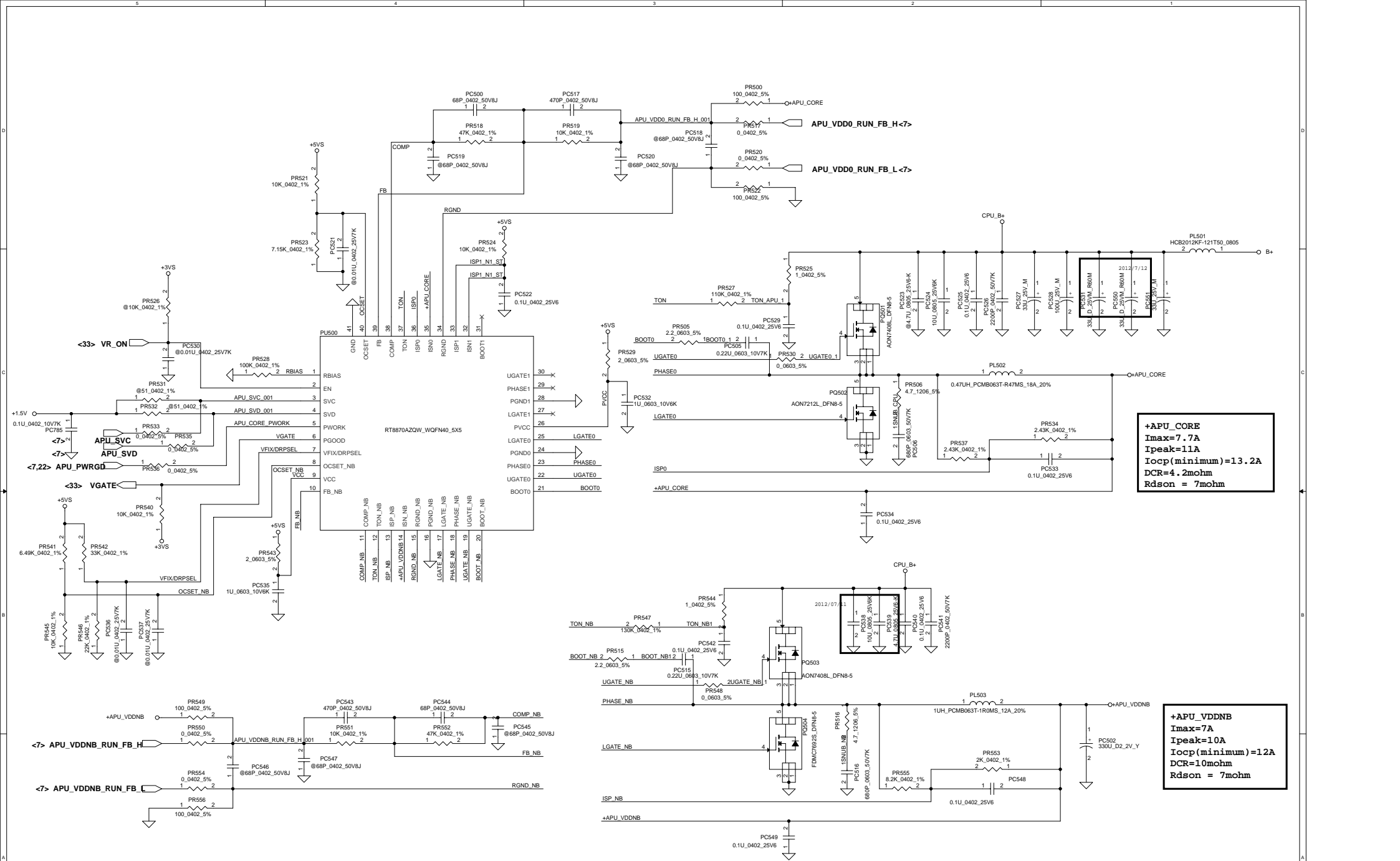




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			LA-8712P	B
Date:			Saturday, September 07, 2013	Sheet 41 of 47



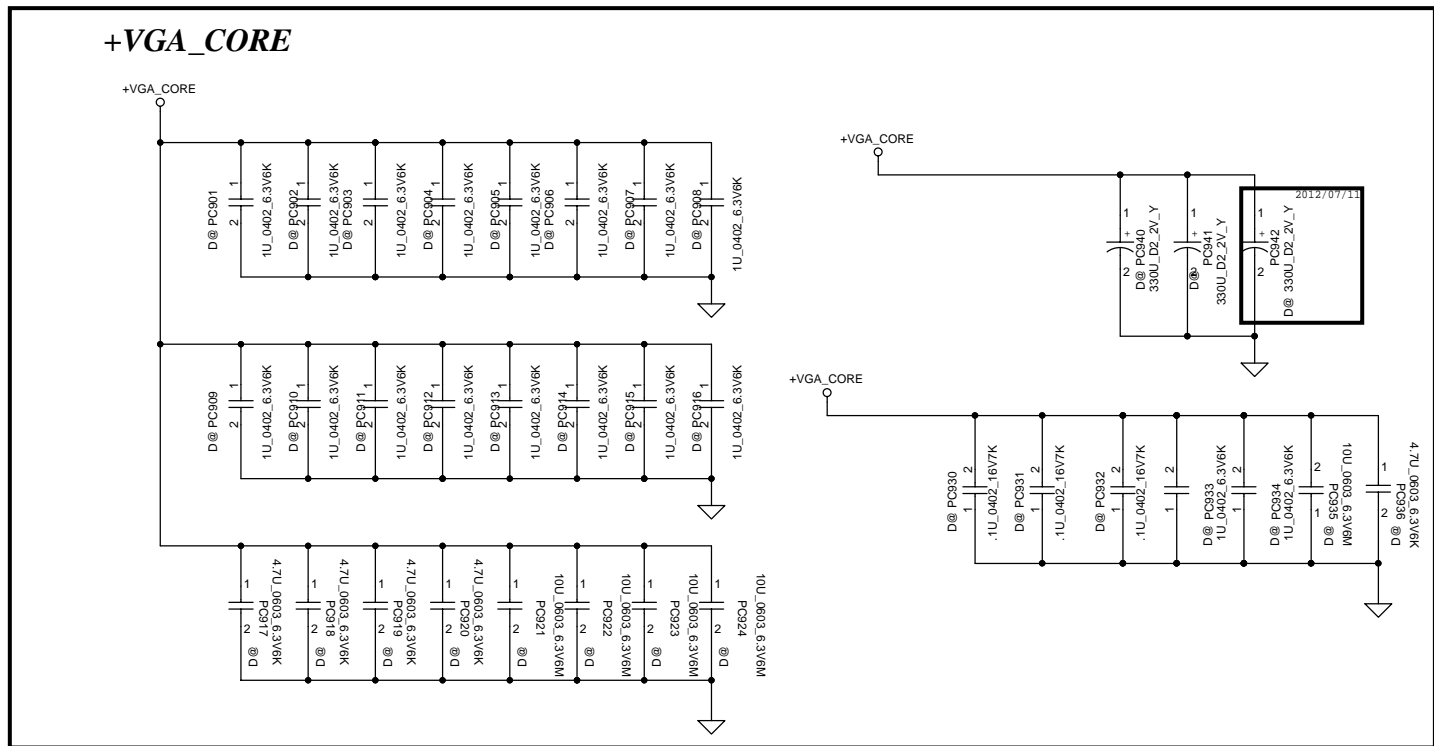
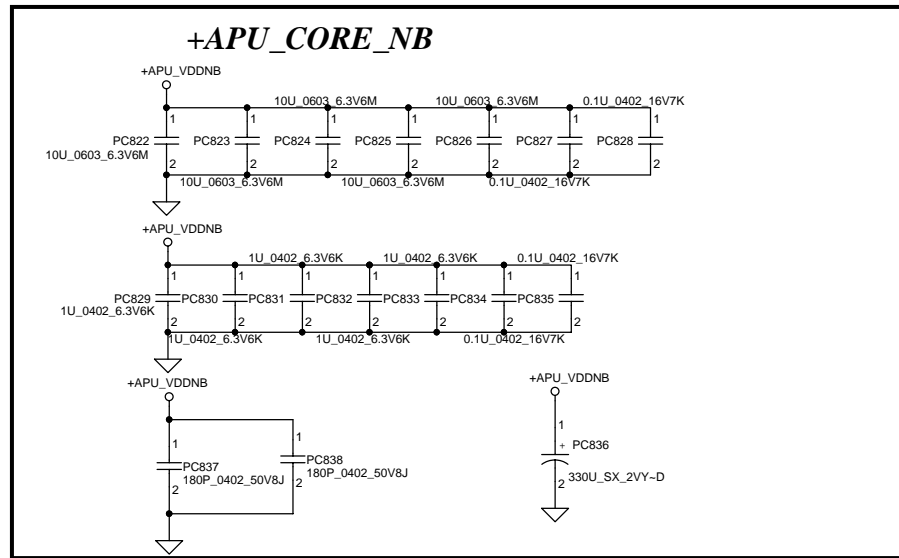
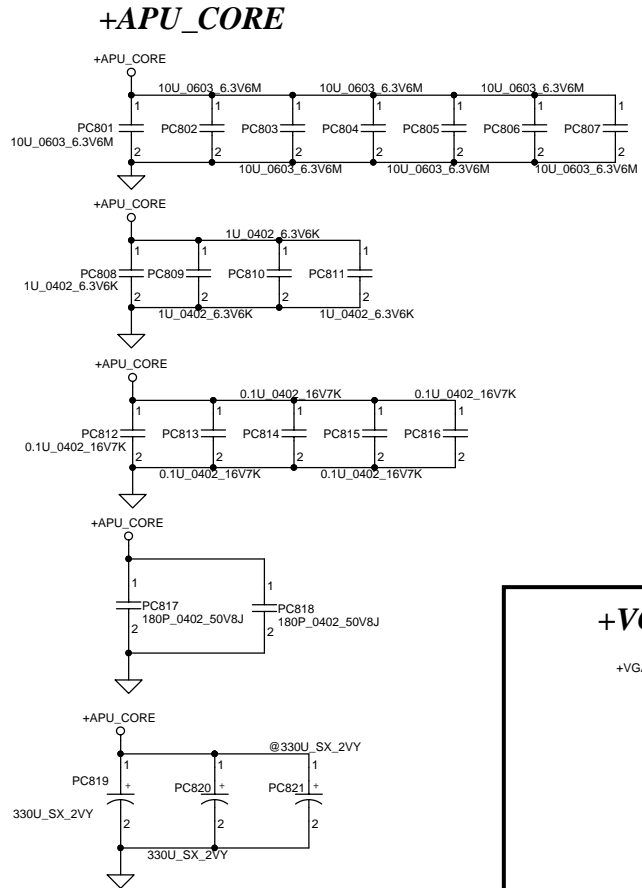
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Size	Document Number	LA-8712P	Rev	B
Date:	Saturday, September 07, 2013	Sheet	42	of 47



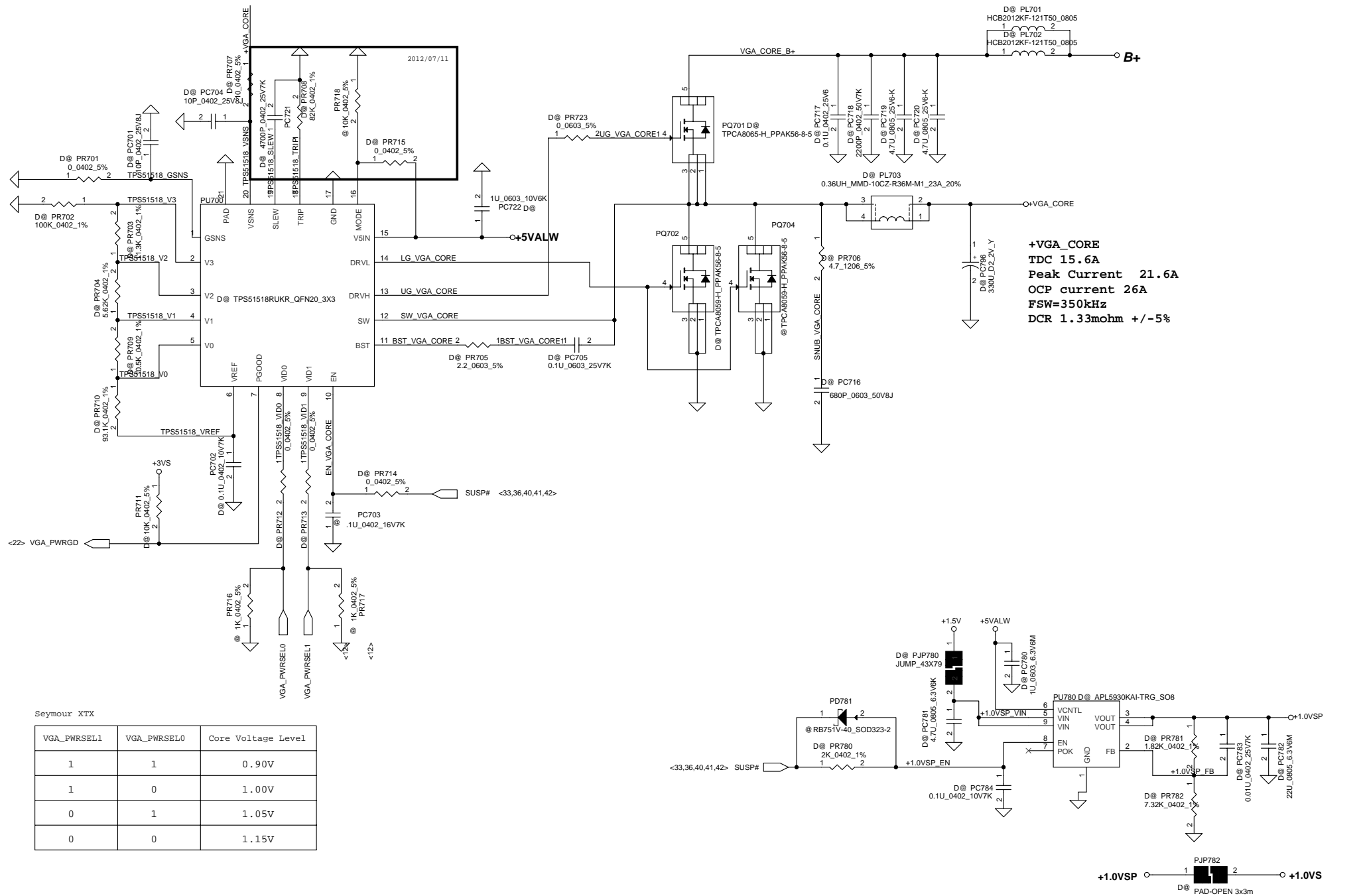
**+APU\_CORE**  
 I<sub>max</sub>=7.7A  
 I<sub>peak</sub>=11A  
 I<sub>opp(minimum)</sub>=13.2A  
 DCR=4.2mohm  
 R<sub>dson</sub> = 7mohm

**+APU\_VDDNB**  
 I<sub>max</sub>=7A  
 I<sub>peak</sub>=10A  
 I<sub>opp(minimum)</sub>=12A  
 DCR=10mohm  
 R<sub>dson</sub> = 7mohm

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Size	Document Number <b>4019K4</b>	Rev	B
Date:	Saturday, September 07, 2013	ISheet	43 of 47



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				LA-8712P
				Rev B
				Date: Saturday, September 07, 2013
				Sheet 44 of 47



**+VGA\_CORE**  
 TDC 15.6A  
 Peak Current 21.6A  
 OCP current 26A  
 FSW=350kHz  
 DCR 1.33mohm +/-5%

Seymour XT

VGA_PWRSEL1	VGA_PWRSEL0	Core Voltage Level
1	1	0.90V
1	0	1.00V
0	1	1.05V
0	0	1.15V

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2012/04/24	P37-PWR-DCIN/BATT CONN/OTP	Change PR12 from 6.49k to 24k	Change source
2.	2012/04/24	P37-PWR-DCIN/BATT CONN/OTP	Add PR13 1k	Change source
3.	2012/04/24	P38-PWR_PWR-CHARGER	Change PQ209 from SI1304BDL-T1-GE3_SC70-3 to SSM3K7002FU_SC70-3	Change source
4.	2012/04/24	P38-PWR_PWR-CHARGER	Change PC244 from 0.1u to 0.22u	Change source
5.	2012/04/24	P38-PWR_PWR-CHARGER	Change PR241 from 100k to 150k	Adjust current limit point
6.	2012/04/24	P41-PWR-3.3VALWP/5VALWP	Change PR330 from 13k to 13.7k	Adjust 3v voltage for HW request
7.	2012/04/24	P41-PWR-3.3VALWP/5VALWP	Change PR351 from 19.1K to 20k	Adjust 5v voltage for HW request
8.	2012/04/24	P41-PWR+1.1VALWP/+1.8VSP	Change PU180 from SY8032ABC_SOT23-6 to SY8033BDBC_DFN10_3X3	Change IC solution for cost down
9.	2012/04/24	P43-PWR-CPU_CORE	Add PC531 33u	For acoustic noise
10.	2012/04/24	P43-PWR-CPU_CORE	Add PC550 33u	For acoustic noise
11.	2012/04/24	P43-PWR-CPU_CORE	Add PC551 33u	For acoustic noise
12.	2012/05/17	P38-PWR_PWR-CHARGER	Un-mount PC123 10U and PC124 10U	For acoustic noise
13.	2012/05/17	P39-PWR-3.3VALWP/5VALWP	Add PR336 4.7 and PC336 680P	EMI demand
14.	2012/05/17	P39-PWR-3.3VALWP/5VALWP	Add PR356 4.7 and PC356 680P	EMI demand
15.	2012/05/17	P40-PWR_1.5VP/0.75VSP	Add PR156 4.7 and PC156 680P	EMI demand
16.	2012/05/17	P40-PWR_1.5VP/0.75VSP	PL152 Change partnumber SH00000PJ00 to SH00000QD00	lake of material
17.	2012/05/17	P43-PWR-CPU_CORE	Change PC538 from 10U to 4.7U	For acoustic noise
18.	2012/05/17	P43-PWR-CPU_CORE	Add PC539 4.7U	For acoustic noise
19.	2012/05/17	P43-PWR-CPU_CORE	Add PC785 0.1U	For acoustic noise
20.	2012/05/18	P44-PWR-PROCESSOR-DECOUPLING	Un-mount 1U:PC901,PC902,PC903,PC904,PC905,PC906,PC907,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC916,PC933,PC934	EVT:uma load bom時把vga_core mlcc多Load的部分 DVT:設變數把多餘mlcc拿掉
21.	2012/05/18	P44-PWR-PROCESSOR-DECOUPLING	Un-mount 10U:PC921,PC922,PC923,PC924,PC935	
22.	2012/05/18	P44-PWR-PROCESSOR-DECOUPLING	Un-mount 0.1U:PC930,PC931,PC932	
23.	2012/05/18	P44-PWR-PROCESSOR-DECOUPLING	Un-mount 330U:PC940,PC941	
24.	2012/05/18	P44-PWR-PROCESSOR-DECOUPLING	Un-mount 4.7U:PC917,PC918,PC919,PC920,PC936	
25.	2012/06/18	P41-PWR-3.3VALWP/5VALWP	Change part number PC331 and PC351 from MATSUKI to S.Elcon	forbid:MATSUKI
26.	2012/06/18	P41-PWR-3.3VALWP/5VALWP	Change part number PQ333 from TOSHIBA to TOSHIBA	EOL
27.	2012/06/18	P43-PWR-CPU_CORE	Change part number PC531 and PC550 from Panasonic to KEMET	shortage
28.	2012/07/16	P37-PWR-DCIN/BATT CONN/OTP	Add PR2 10K and PC11 Change to unmount	For support 60w adapter
29.	2012/07/16	P38-PWR_PWR-CHARGER	Change vendor PQ205 and PQ207 from DII to NIKO-SEM	Customoer forbid DII
30.	2012/07/16	P40-P40-PWR_1.5VP / 0.75VSP	Change PR154 from 10.2k to 10k	For HW request
31.	2012/07/16	P43-PWR-CPU_CORE	Change vendor PC531 and PC550 from Kemet to Sayno	For acoustic noise
32.	2012/07/16	P43-PWR-CPU_CORE	Change PC538 and Pc539 from 4.7u to 10u	For acoustic noise
33.	2012/07/16	P45-PWR-VGA_CORE/1.0VSP	Change PR708 from 130K to 82k	Adjust over current protection point
34.	2012/07/16	P45-PWR-VGA_CORE/1.0VSP	Add PR718 and PR715	For vga transient test
35.	2012/07/16	P37-PWR-DCIN/BATT CONN/OTP P38-PWR_CHARGER P39-PWR-3.3VALWP/5VALWP P40-PWR_1.5VP / 0.75VSP P43-PWR-APU_CORE	Change PC6,PC157,PC211,PC212,PC222,PC223,PC358,PC524,PC539,PC538 from TAIYO(10U_25V_0805_H1.25) to Murata	For acoustic noise
36.	2012/08/07	P41-PWR-3.3VALWP/5VALWP	Change PR351 from 20k to 19.1k	Adjust 5v voltage for HW request

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# HW PIR (Product Improve Record)

VBLE4/5 LA-8866P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2012/02/14

Item	Date	Page	Solution	Request
1.	2/1	P28	Change JUSB.1 from +USB_VCCB to +USB_VCCC	For USB power
2.	2/1	P18	Change RV141,RV138,RV138,RV137 to DIS@	For VGA int. sensor
3.	2/1	P12	Remove RV29, change RV28 to 0 ohm	For VGA 2MHz
4.	2/1	P22	Change R339 to UMA@ , Change R340 to DIS@	For board ID
5.	2/1	P29	Change +1.8VGS to +1.8VS	For Green CLK
6.	2/2	P30	Change CL36 from SEL20102K80 to SEL20102K90	For shortage
7.	2/6	P32	Update JCRIO pin definition	Change int. MIC to MB
8.	2/6	P31	Add RA36,RA37 and delete CA64	Move sense resistors to MB
9.	2/6	P35	Change JTP from SP010015H00 to SP01001BF10	For ME request
10.	2/6	P31	Add JM1C connector SP02000R000	For customer request
11.	2/6	P29	Change JWLAN from SP07000JP00 to SP07000TB00	For ME request
12.	2/8	P30	Add PU31	For saving power consumption
13.	2/8	P29	Add PU33, WLAN power circuit and reset pin	For customer request
14.	2/8	P29	Change CM7,CM8,CM9 to @	For cost down
15.	2/8	P29	Add WLAN_PWR# and WLAN_RST#	For customer request
16.	2/8	P30	Add test point TLI for pin37	For vendor request
17.	2/8	P27	Delete SW4	For layout request
18.	2/8	P11	Change UV1 from SA000047G70 to SA000047G60	For PJE request
19.	2/8	P18	Change RV118, RV119 to DIS@	For HDMI issue
20.	2/8	P35	Add screw H17, H20 and H21	For ME request
21.	2/9	P21	Reserve ESD D94-D96 for HDMI	For ESD request
22.	2/9	P9	Change C218 from 390U to 330U (SF000002080)	For cost down
23.	2/9	P20	Remove D3-D5 and add D97 and D98	For ESD request
24.	2/9	P30	Reserve ESD D99 and D100 for LAN	For ESD request
25.	2/9	P27	Add resistors R87,R89,R164,R158	Improve SATA signal quality
26.	2/10	P27	Add JDDC	For HW experiment on DVT
27.	2/10	P8	Add C95,C102,C105	For EMI request
28.	2/10	P34	Change C457,R393 to mount	For EMI request
29.	2/10	P29	Change CCL10 to mount	For EMI request
30.	2/10	P24	Change ODD_DA#_FCH connect to U2.P6	For Module Design
31.	2/10	P24	Change ODD_PLUGIN# connect to P2.W7	For Module Design
32.	2/10	P21	Change Q6 from SB00000M700 to SB570020020	For BOM reduce
33.	4/23	P19	Change R117 +3VS to +3VALW	For LVDS power down sequence
34.	4/23	P19	Change R110,R133,C265,C261	For LVDS power down sequence
35.	4/23	P19	Change R388 +3VS to +5VS,R388 +3VS_LVDS_CAM to +5VS_LVDS_CAM	
36.	4/23	P21	Add C202 and C216	For EMI request
37.	4/23	P22	Change R241 from GCLK6 to @	For USB30 wake issue
38.	4/23	P22	Change C294,C293,Y1,R242 to mount	For USB30 wake issue
39.	4/23	P22	Change R271 and add R277,R268,C305,+RTCBATT_D	
40.	4/23	P29	Change R156,R155,C907,C908,Q210 to @	
41.	4/23	P29	Add RM20 and change UM5,RM21 to @	
42.	4/23	P29	Change UCLL.2 to +3VALW, UCLL.14 to +RTCVCC_D and add RCL10 ,RCLL1	For USB30 wake issue
43.	4/23	P30	Mount QL53 and RL24 and change RL28,RL26 to @	For LAN disable
44.	4/23	P31	Add CA6,CA7	For EMI request
45.	4/23	P31	Add CA64,CA67,CA68,CA77	For EMI request
46.	5/16	P27	Delete R90-R93,R166,R168-R170,C379-C382,R87,R89,R96,R97,R158 R164,R171,R172	For ODD 14" and 15" common PCBA issue
47.	5/16	P27	Add U4	For ODD 14" and 15" common PCBA issue
48.	5/16	P23	Reserve R174	For ODD 14" and 15" common PCBA issue
49.	5/16	P27	Change C364 to 220p	For ESD request

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2012/06/18

Item	Date	Page	Solution	Request
1.	6/11	P27	Add JDDC circuit and remove U4 circuit	SATA ODD
2.	6/11	P33	Reserve RB8,RE9	Due to TP module for win8 feature
3.	6/15	P7	Change R846,R847,R848,R849,R851,R852 to Reserve	For Debug only

REVISION CHANGE: 0.3 TO 1.0

GERBER-OUT DATE: 2012/07/18

Item	Date	Page	Solution	Request
1.	7/12	P19	Add D85	For avoid LVDS_CLK damage issue
2.	7/17	P6	Add C78	For EMI request
3.	7/18	P27	Un-stuff SW5	For debug only
4.	7/25	P30	Stuff D92	For ESD request
5.	8/27	P32	Stuff CT7 and RT4 on TFM SKU	For EMI request

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Date:	Saturday, September 07, 2013	Sheet	47	of	47
					Rev B