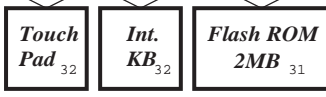
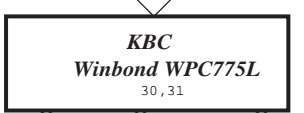
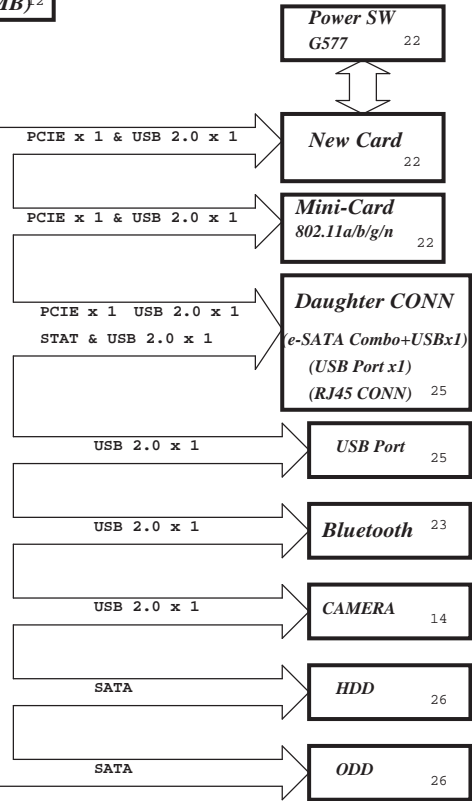
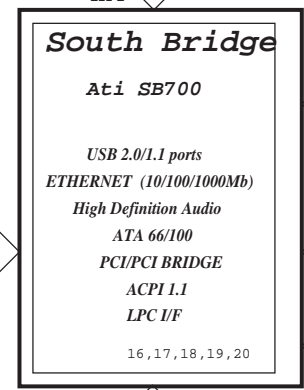
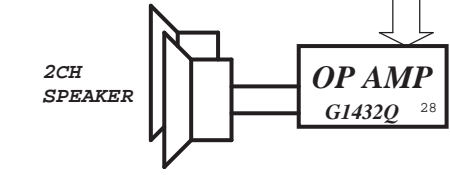
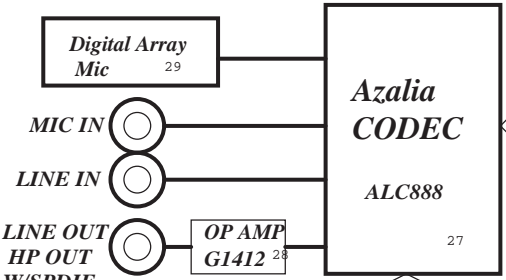
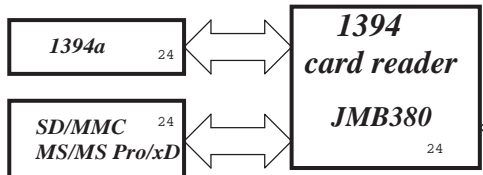
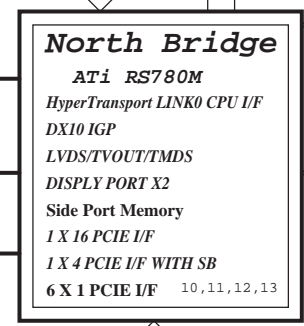
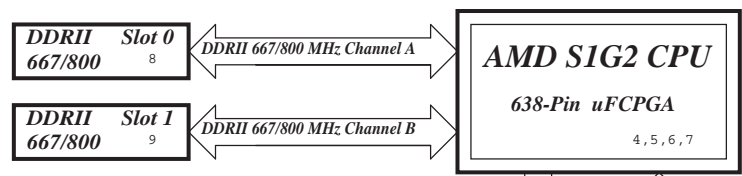


S13 Block Diagram

<http://hobielektronika.net>

Project code : 91.4H801.001
 PCB Number : 48.4H801.0SC
 Revision : SC



CPU V_CORE	
ISL6265 34, 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51124 37	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0

SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC LDO 39	
INPUTS	OUTPUTS
5V_S5 3D3V_S0	0D9V_S3 1D5V_S0

SYSTEM DC/DC LDO 39	
INPUTS	OUTPUTS
3D3V_S5 3D3V_S0	1D2V_S5 2D5V_S0

SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

MAXIM CHARGER BQ24745 41	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

<Core Design>

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Title: **System Block Diagram**

Size A3 Document Number **S13** Rev **SC**

Date: Friday, May 16, 2008 Sheet 1 of 44

RS780M Functional Strap Definitions

STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO. (PIN: RS780M--> VSYNC)
 0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)

* 0 : Enable 1 : Disable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 * 0 : I2C Master can load strap values from EEPROM if connected,
 or use default values if not connected

SB700 Functional Strap Definitions

		PULL HIGH	PULL LOW
CLK_PCI_2	WatchDOG (NB_PWRGD)	ENABLED	DISABLED DEFAULT
CLK_PCI_3	DEBUG STRAPS	USB	IGNORE DEFAULT
CLK_PCI_1 CLK_PCI_4	RESERVED		
LPCCLK0	PCI MEM BOOT	ENABLED	DISABLED DEFAULT
LPCCLK1	INTERNAL CLK GEN	ENABLED	DISABLED DEFAULT
RTCCLK	INTERNAL RTC	ENABLED DEFAULT	DISABLED
AZ_RST#	IMC	ENABLED	DISABLED DEFAULT
SB_GPO17 SB_GPO16	ROM TYPE	H, H = Reserved H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM DEFAULT	

		USB PORT#	DESTINATION
SB700	2.0	0	USB1
		1	CAMERA
		2	Combo (ESATA/USB)
		3	NEW CARD
		4	USB2
		5	Bluetooth
		6	NC
		7	WLAN
		8	NC
		9	NC
		10	NC
	11	NC	
	1.1	12	NC
	13	NC	

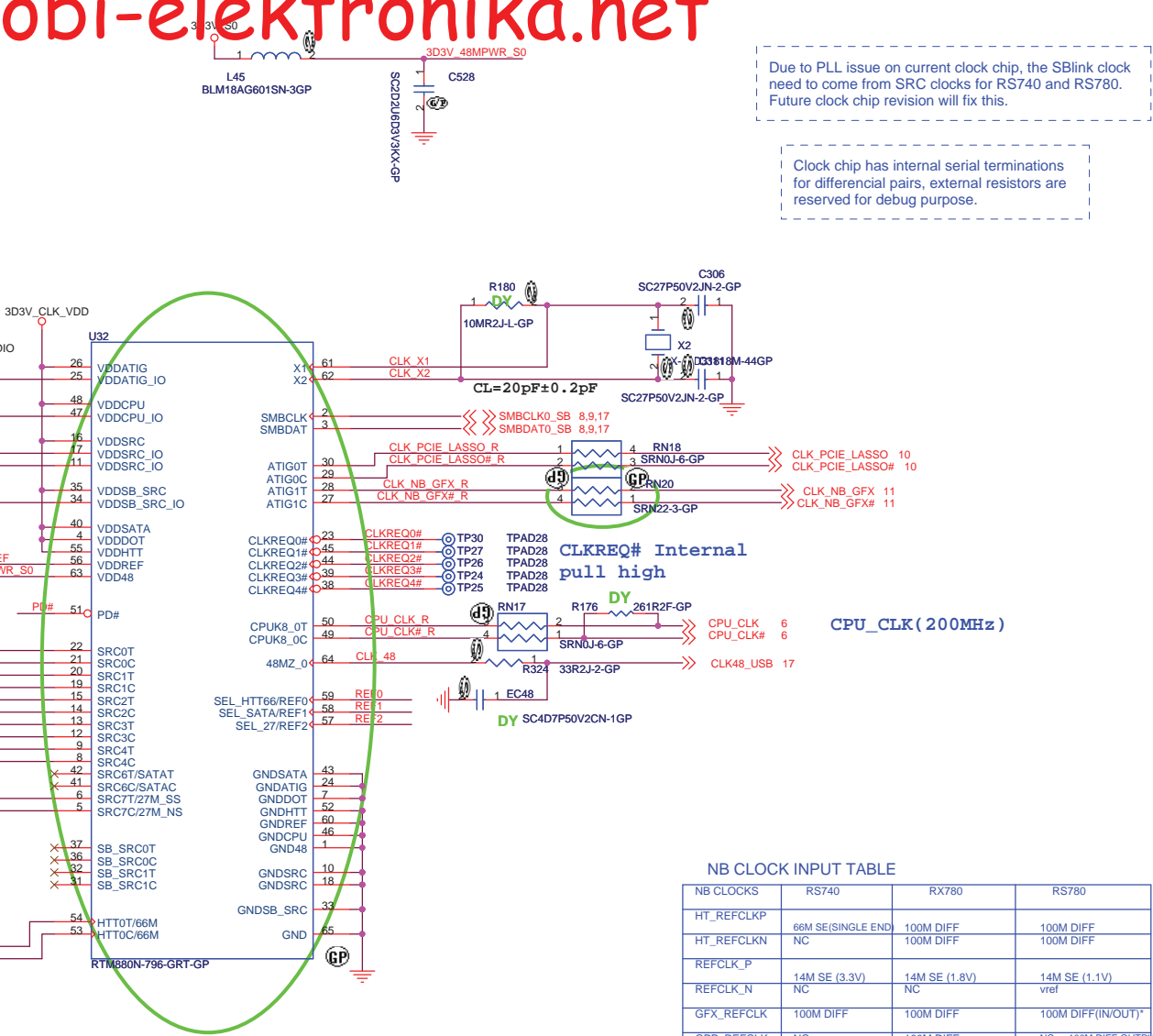
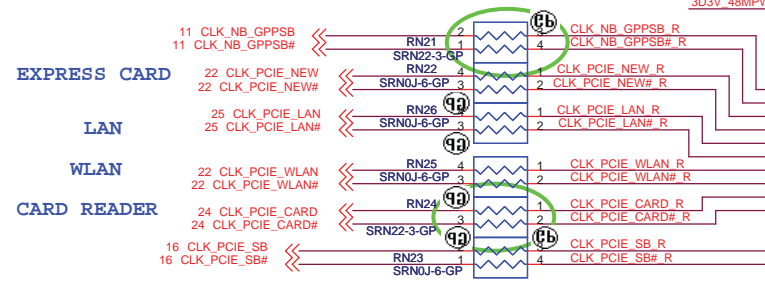
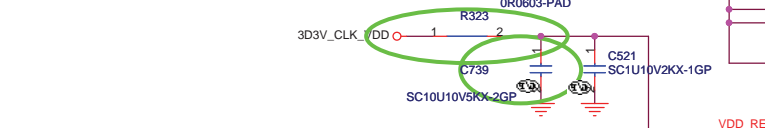
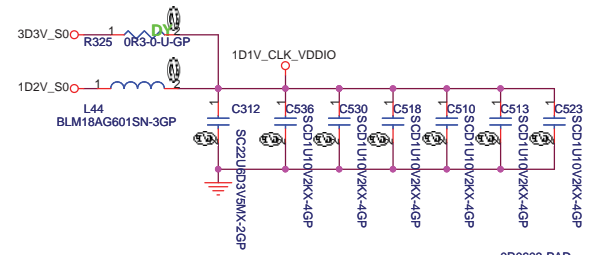
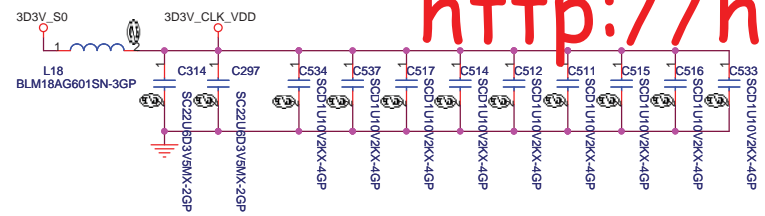
PCI EXPRESS	DESTINATION
Lane 0	NEW CARD
Lane 1	WLAN
Lane 2	LAN
Lane 3	CARD READER&1394
Lane 4	NC
Lane 5	NC

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Table of Content		
Size A3	Document Number S13	Rev SC
Date: Friday, May 16, 2008	Sheet 2	of 44

Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



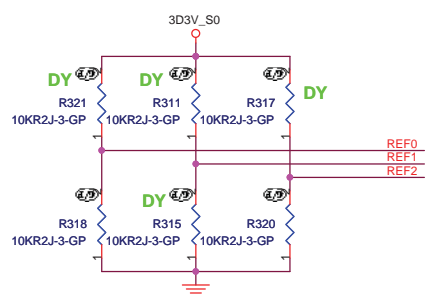
CLKREQ# Internal pull high

CPU_CLK (200MHz)

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.



* default

SEL_HTT66	FS0	1	66 MHz 3.3V single ended HTT clock
SEL_SATA	FS1	1	100 MHz non-spreading differential SATA clock
SEL_27	FS2	1	100 MHz spreading differential SRC clock
		0	27MHz non-spreading singled clock on pin 13 and 27MHz spread clock on pin 14
		0	100MHz differential spreading SRC clock

OSC 14M NB
RS780M 1.1V 158R/90.9P

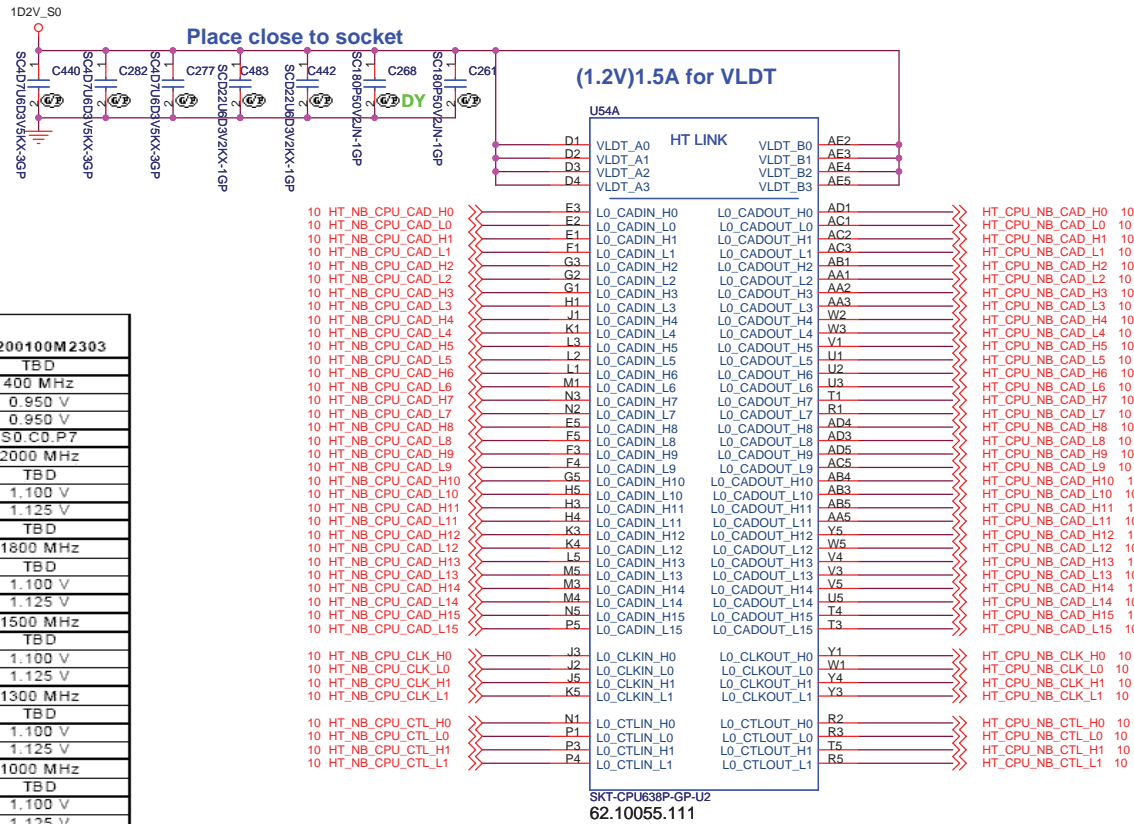
<Core Design>

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Title: **Clock Gen-ICS 9LPR473**

Size A3: Document Number **S13** Rev **SC**

Date: Friday, May 16, 2008 Sheet 3 of 44

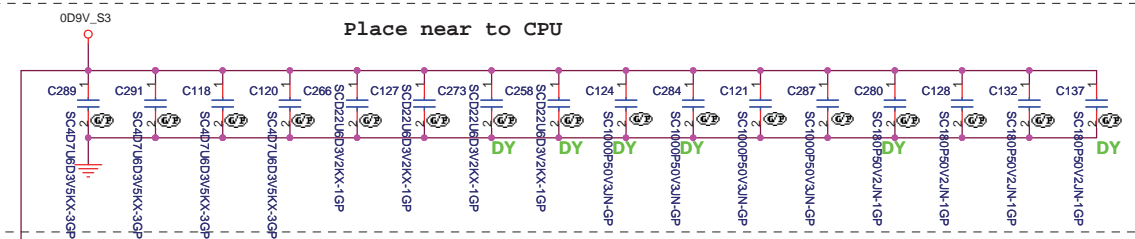


State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

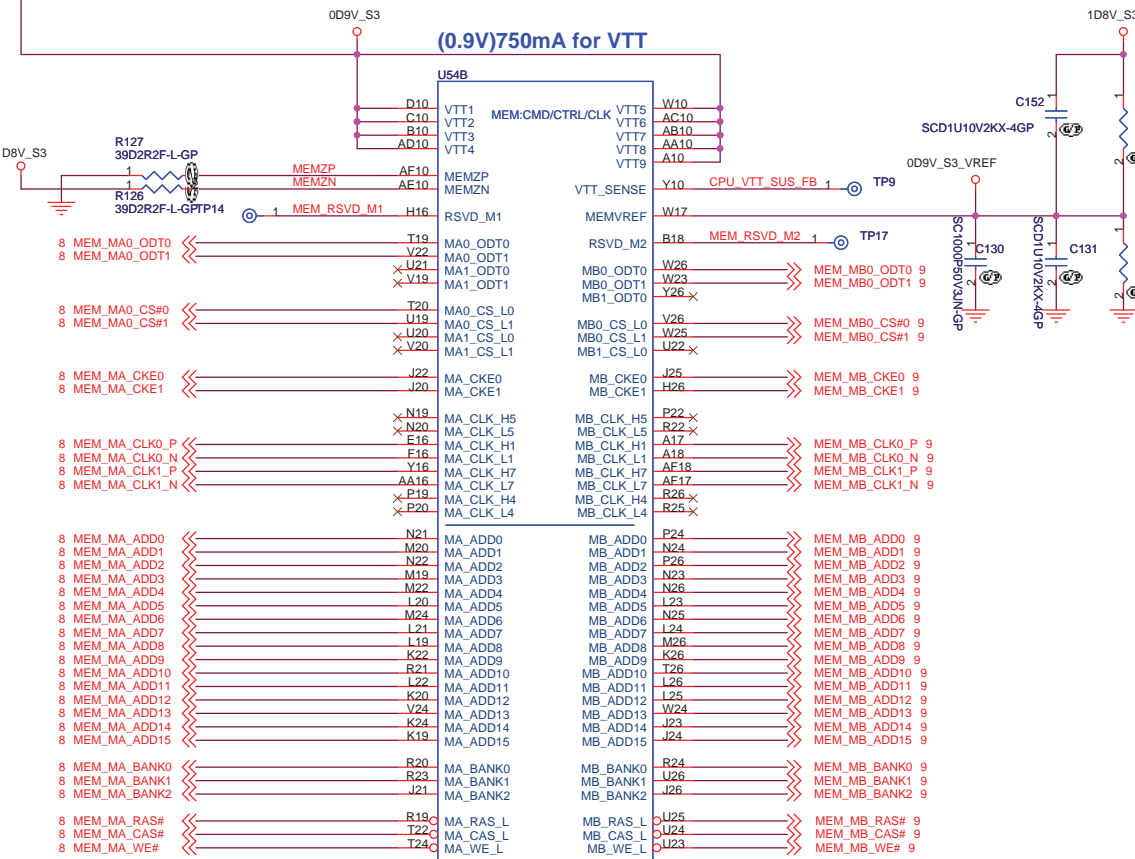
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|----------------------|----|--------------|---------------|-----|-------------------|----|
| 10 HT_NB_CPU_CAD_H0 | E3 | L0_CADIN_H0 | L0_CADOUT_H0 | AD1 | HT_CPU_NB_CAD_H0 | 10 |
| 10 HT_NB_CPU_CAD_H1 | E2 | L0_CADIN_L0 | L0_CADOUT_L0 | AC1 | HT_CPU_NB_CAD_H1 | 10 |
| 10 HT_NB_CPU_CAD_H1 | E1 | L0_CADIN_H1 | L0_CADOUT_H1 | AC2 | HT_CPU_NB_CAD_H1 | 10 |
| 10 HT_NB_CPU_CAD_L1 | F1 | L0_CADIN_L1 | L0_CADOUT_L1 | AC3 | HT_CPU_NB_CAD_L1 | 10 |
| 10 HT_NB_CPU_CAD_H2 | G3 | L0_CADIN_H2 | L0_CADOUT_H2 | AB1 | HT_CPU_NB_CAD_H2 | 10 |
| 10 HT_NB_CPU_CAD_L2 | G2 | L0_CADIN_L2 | L0_CADOUT_L2 | AA1 | HT_CPU_NB_CAD_L2 | 10 |
| 10 HT_NB_CPU_CAD_H3 | H1 | L0_CADIN_H3 | L0_CADOUT_H3 | AA2 | HT_CPU_NB_CAD_H3 | 10 |
| 10 HT_NB_CPU_CAD_L3 | J1 | L0_CADIN_L3 | L0_CADOUT_L3 | W2 | HT_CPU_NB_CAD_L3 | 10 |
| 10 HT_NB_CPU_CAD_H4 | K1 | L0_CADIN_H4 | L0_CADOUT_H4 | AA3 | HT_CPU_NB_CAD_H4 | 10 |
| 10 HT_NB_CPU_CAD_L4 | L3 | L0_CADIN_L4 | L0_CADOUT_L4 | W3 | HT_CPU_NB_CAD_L4 | 10 |
| 10 HT_NB_CPU_CAD_H5 | L1 | L0_CADIN_H5 | L0_CADOUT_H5 | V1 | HT_CPU_NB_CAD_H5 | 10 |
| 10 HT_NB_CPU_CAD_L5 | L4 | L0_CADIN_L5 | L0_CADOUT_L5 | U1 | HT_CPU_NB_CAD_L5 | 10 |
| 10 HT_NB_CPU_CAD_H6 | M1 | L0_CADIN_H6 | L0_CADOUT_H6 | U2 | HT_CPU_NB_CAD_H6 | 10 |
| 10 HT_NB_CPU_CAD_L6 | N3 | L0_CADIN_L6 | L0_CADOUT_L6 | U3 | HT_CPU_NB_CAD_L6 | 10 |
| 10 HT_NB_CPU_CAD_H7 | N2 | L0_CADIN_H7 | L0_CADOUT_H7 | T1 | HT_CPU_NB_CAD_H7 | 10 |
| 10 HT_NB_CPU_CAD_L7 | E5 | L0_CADIN_L7 | L0_CADOUT_L7 | R1 | HT_CPU_NB_CAD_L7 | 10 |
| 10 HT_NB_CPU_CAD_H8 | F5 | L0_CADIN_H8 | L0_CADOUT_H8 | AD4 | HT_CPU_NB_CAD_H8 | 10 |
| 10 HT_NB_CPU_CAD_L8 | F4 | L0_CADIN_L8 | L0_CADOUT_L8 | AD3 | HT_CPU_NB_CAD_L8 | 10 |
| 10 HT_NB_CPU_CAD_H9 | G5 | L0_CADIN_H9 | L0_CADOUT_H9 | AD5 | HT_CPU_NB_CAD_H9 | 10 |
| 10 HT_NB_CPU_CAD_L9 | H5 | L0_CADIN_L9 | L0_CADOUT_L9 | AB4 | HT_CPU_NB_CAD_L9 | 10 |
| 10 HT_NB_CPU_CAD_H10 | H4 | L0_CADIN_H10 | L0_CADOUT_H10 | AB3 | HT_CPU_NB_CAD_H10 | 10 |
| 10 HT_NB_CPU_CAD_L10 | H3 | L0_CADIN_L10 | L0_CADOUT_L10 | AB5 | HT_CPU_NB_CAD_L10 | 10 |
| 10 HT_NB_CPU_CAD_H11 | H4 | L0_CADIN_H11 | L0_CADOUT_H11 | AA6 | HT_CPU_NB_CAD_H11 | 10 |
| 10 HT_NB_CPU_CAD_L11 | K3 | L0_CADIN_L11 | L0_CADOUT_L11 | V5 | HT_CPU_NB_CAD_L11 | 10 |
| 10 HT_NB_CPU_CAD_H12 | L5 | L0_CADIN_H12 | L0_CADOUT_H12 | W5 | HT_CPU_NB_CAD_H12 | 10 |
| 10 HT_NB_CPU_CAD_L12 | K4 | L0_CADIN_L12 | L0_CADOUT_L12 | V4 | HT_CPU_NB_CAD_L12 | 10 |
| 10 HT_NB_CPU_CAD_H13 | M5 | L0_CADIN_H13 | L0_CADOUT_H13 | V3 | HT_CPU_NB_CAD_H13 | 10 |
| 10 HT_NB_CPU_CAD_L13 | M3 | L0_CADIN_L13 | L0_CADOUT_L13 | V5 | HT_CPU_NB_CAD_L13 | 10 |
| 10 HT_NB_CPU_CAD_H14 | M4 | L0_CADIN_H14 | L0_CADOUT_H14 | V6 | HT_CPU_NB_CAD_H14 | 10 |
| 10 HT_NB_CPU_CAD_L14 | N5 | L0_CADIN_L14 | L0_CADOUT_L14 | U5 | HT_CPU_NB_CAD_L14 | 10 |
| 10 HT_NB_CPU_CAD_H15 | P5 | L0_CADIN_H15 | L0_CADOUT_H15 | T4 | HT_CPU_NB_CAD_H15 | 10 |
| 10 HT_NB_CPU_CAD_L15 | P4 | L0_CADIN_L15 | L0_CADOUT_L15 | T3 | HT_CPU_NB_CAD_L15 | 10 |
| 10 HT_NB_CPU_CLK_H0 | J3 | L0_CLKIN_H0 | L0_CLKOUT_H0 | Y1 | HT_CPU_NB_CLK_H0 | 10 |
| 10 HT_NB_CPU_CLK_L0 | J2 | L0_CLKIN_L0 | L0_CLKOUT_L0 | W1 | HT_CPU_NB_CLK_L0 | 10 |
| 10 HT_NB_CPU_CLK_H1 | J5 | L0_CLKIN_H1 | L0_CLKOUT_H1 | Y4 | HT_CPU_NB_CLK_H1 | 10 |
| 10 HT_NB_CPU_CLK_L1 | K5 | L0_CLKIN_L1 | L0_CLKOUT_L1 | Y3 | HT_CPU_NB_CLK_L1 | 10 |
| 10 HT_NB_CPU_CTL_H0 | N1 | L0_CTLIN_H0 | L0_CTLOUT_H0 | R2 | HT_CPU_NB_CTL_H0 | 10 |
| 10 HT_NB_CPU_CTL_L0 | P1 | L0_CTLIN_L0 | L0_CTLOUT_L0 | R3 | HT_CPU_NB_CTL_L0 | 10 |
| 10 HT_NB_CPU_CTL_H1 | P3 | L0_CTLIN_H1 | L0_CTLOUT_H1 | T5 | HT_CPU_NB_CTL_H1 | 10 |
| 10 HT_NB_CPU_CTL_L1 | P4 | L0_CTLIN_L1 | L0_CTLOUT_L1 | R5 | HT_CPU_NB_CTL_L1 | 10 |

SKT-CPU638P-GP-U2
62.10055.111

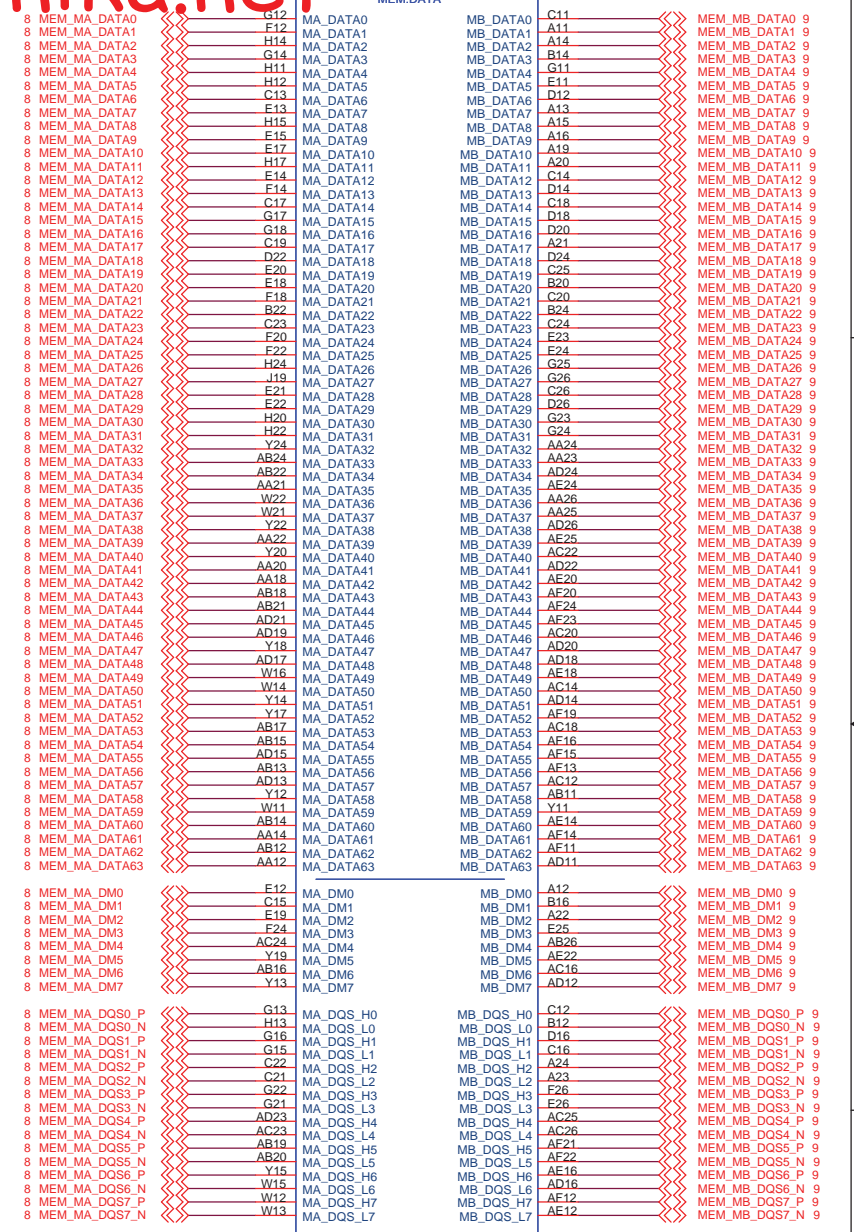
Place near to CPU



(0.9V)750mA for VTT



SKT-CPU638P-GP-U2



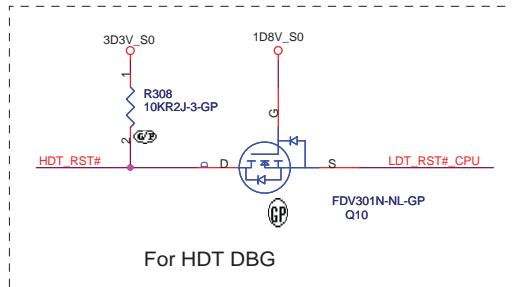
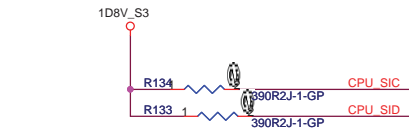
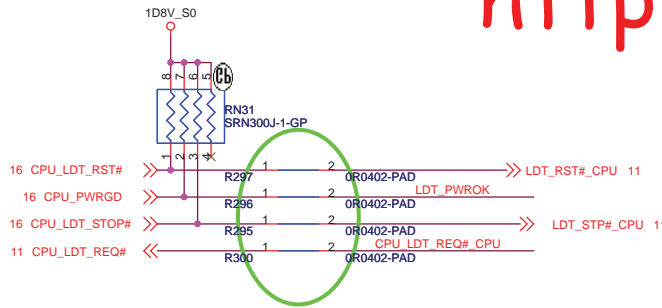
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<Core Design>

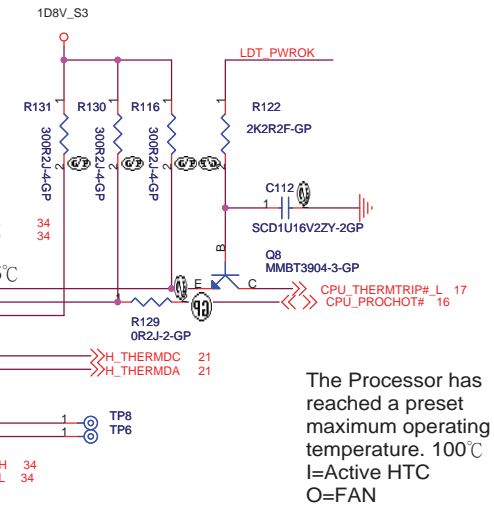
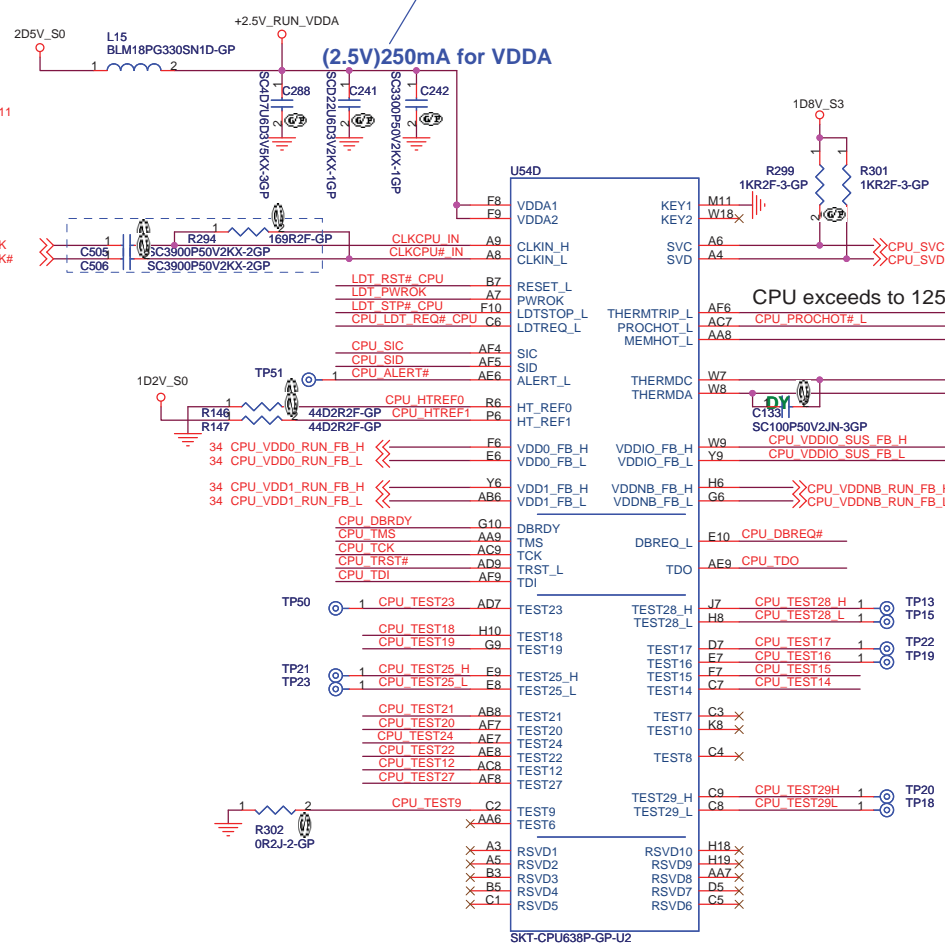
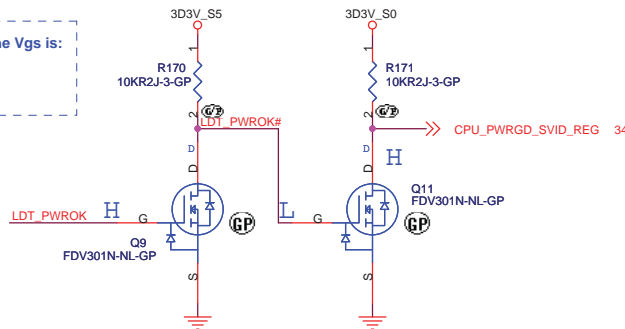
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Table with 4 columns: Title, Size, Date, Rev. Title: CPU DDR (2/4), Size: A3, Date: Friday, May 16, 2008, Rev: SC

LYAOU CPU PCB VDDX TRAC APPROX
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

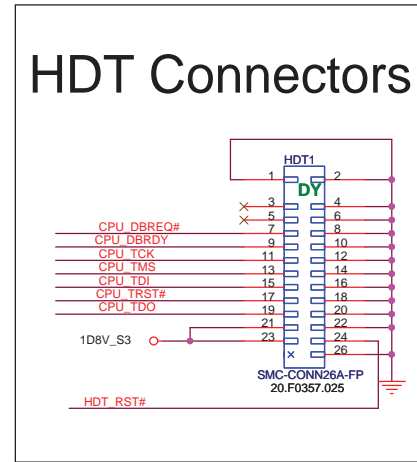
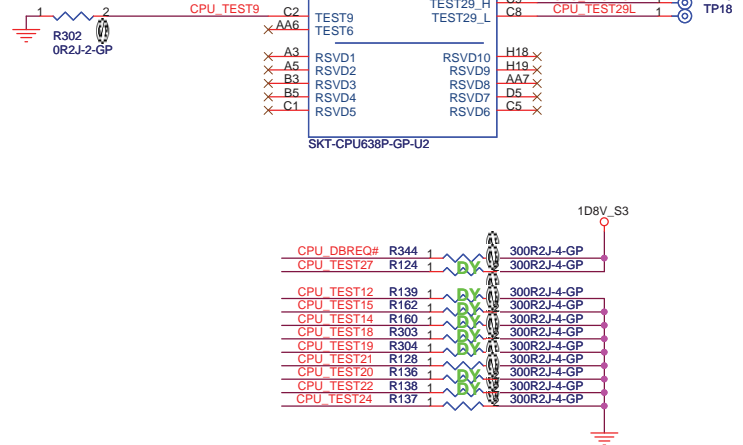


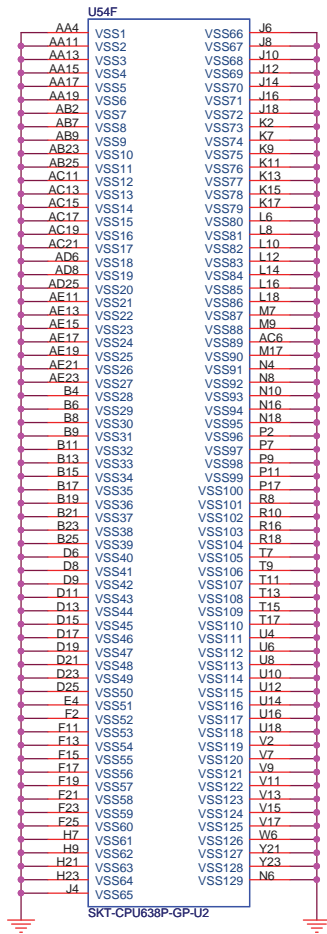
FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V



The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

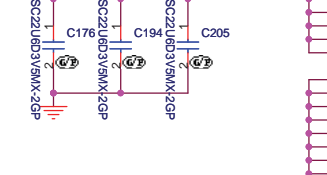




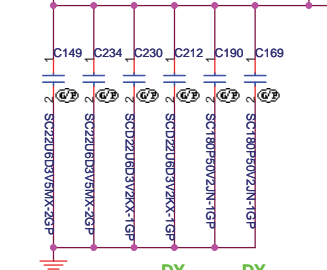
36A for VDD0&VDD1
Bottom Side Decoupling



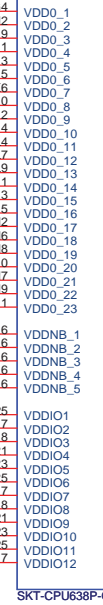
(0.8~1.1V)3A for VDDNB
Bottom Side Decoupling



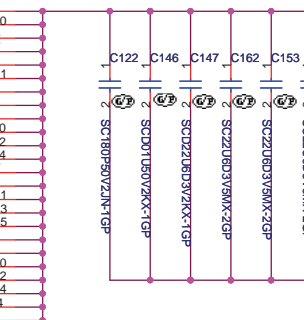
(1.8V)2A for VDDIO
Bottom Side Decoupling



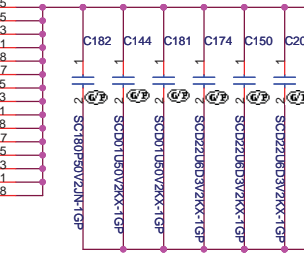
U54E



Bottom Side Decoupling



Place near to CPU



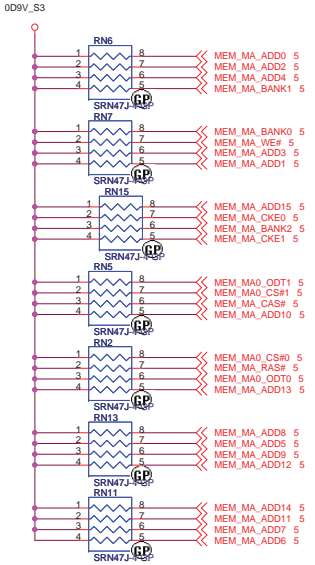
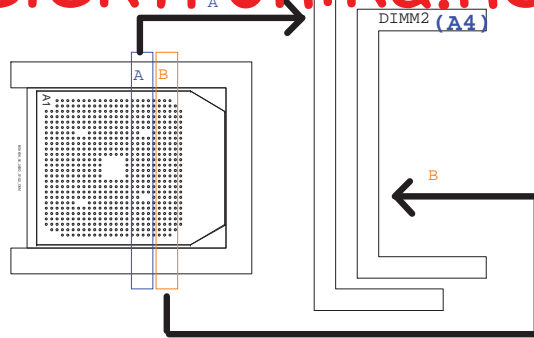
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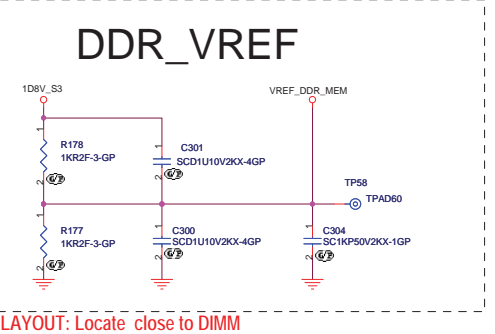
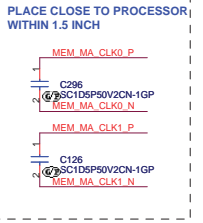
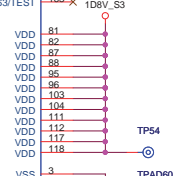
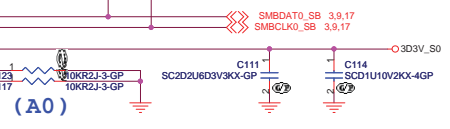
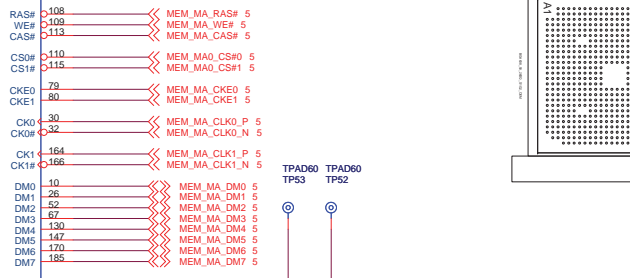
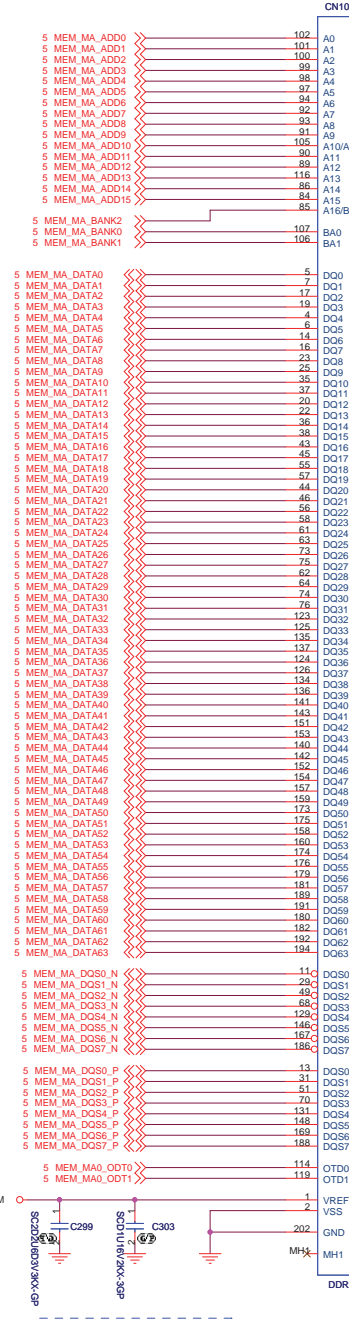
Title: **CPU Power (4/4)**

Size A3	Document Number	Rev
	S13	SC

Date: Friday, May 16, 2008 Sheet 7 of 44

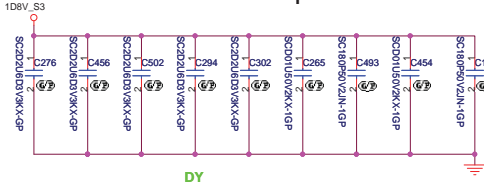


REVERSE TYPE



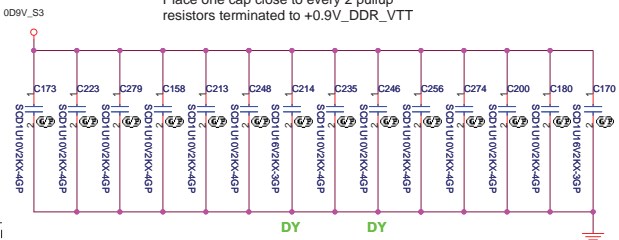
Decoupling Capacitor

Place these Caps near DM1



DY

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



DY DY

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR address and Control Signals.

Place C2.2uF and 0.1uF < 500mils from DDR connector

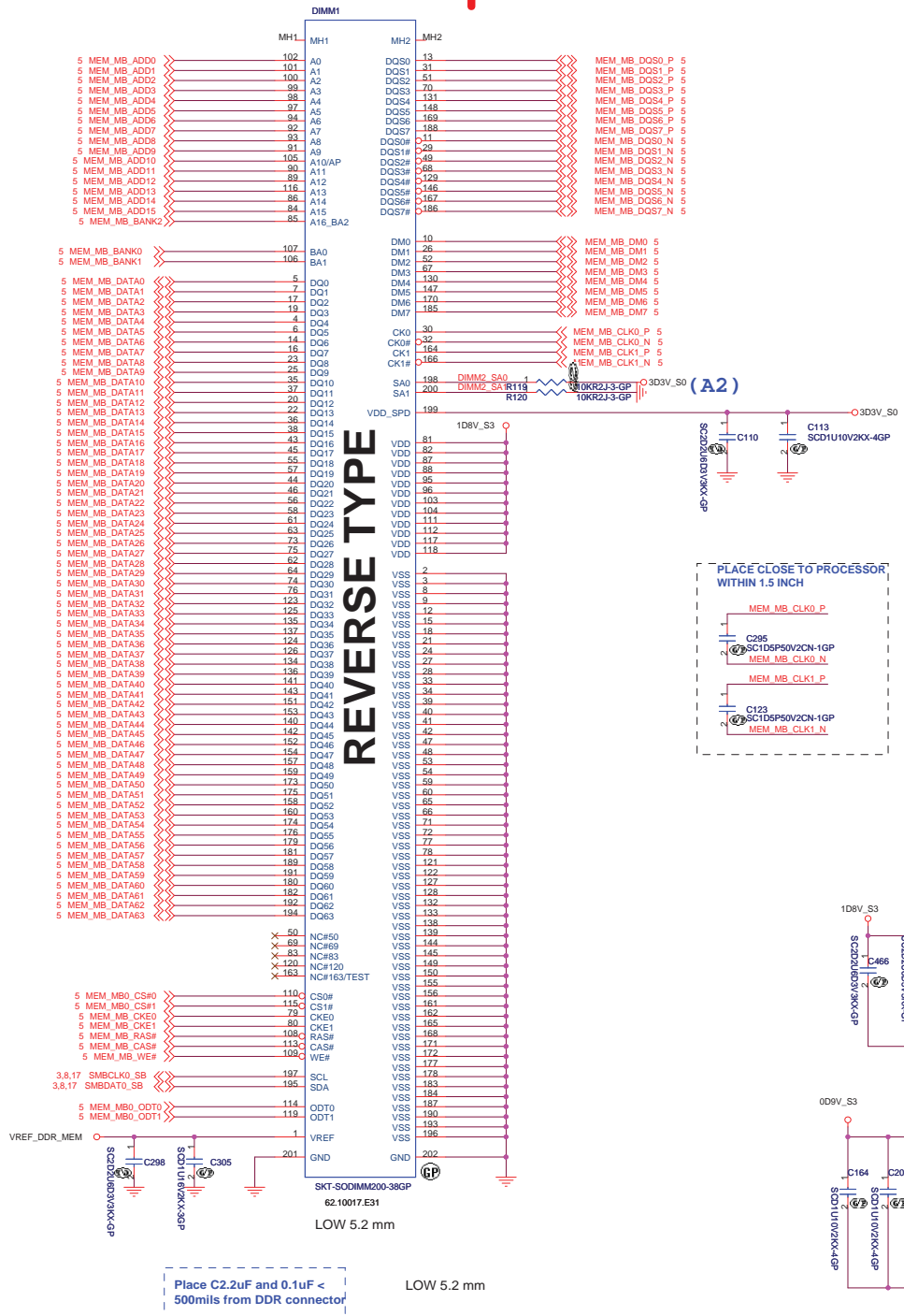
LAYOUT: Locate close to DIMM

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DDR DIMM1
S13

Rev SC

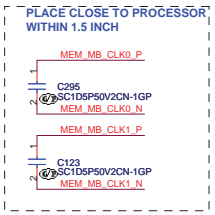
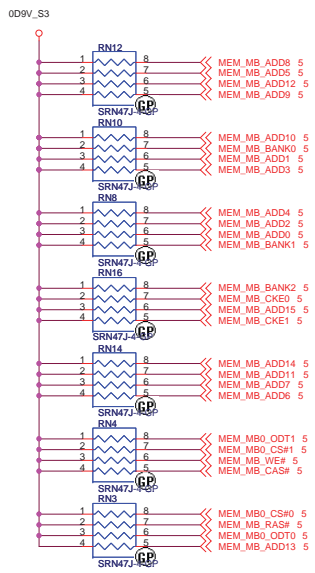
Date: Friday, May 16, 2008 Sheet 8 of 44



PARALLEL TERMINATION

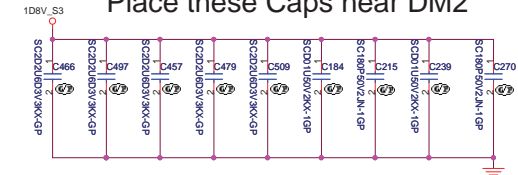
Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR address and Control Signals.

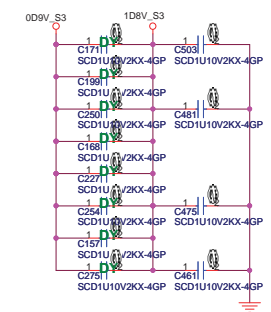
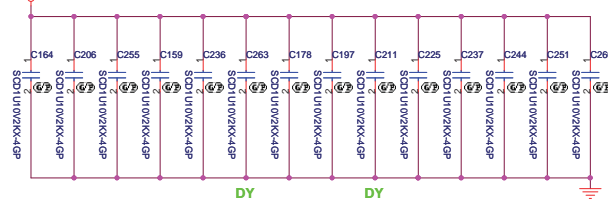


Decoupling Capacitor

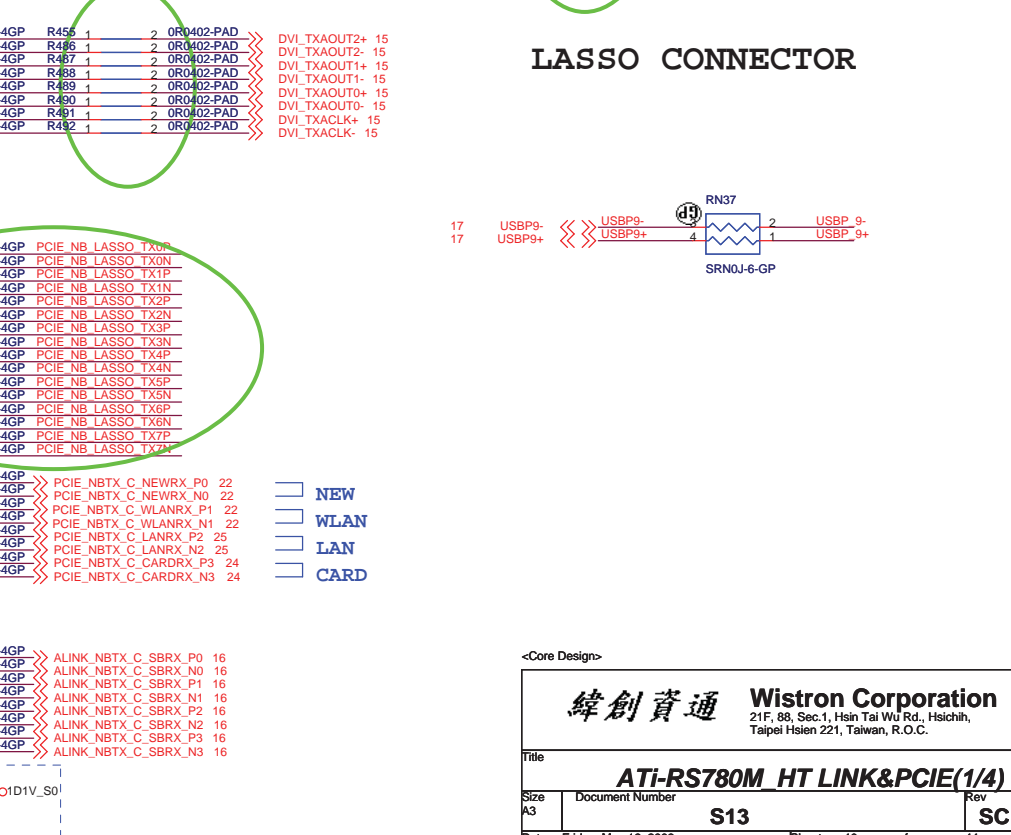
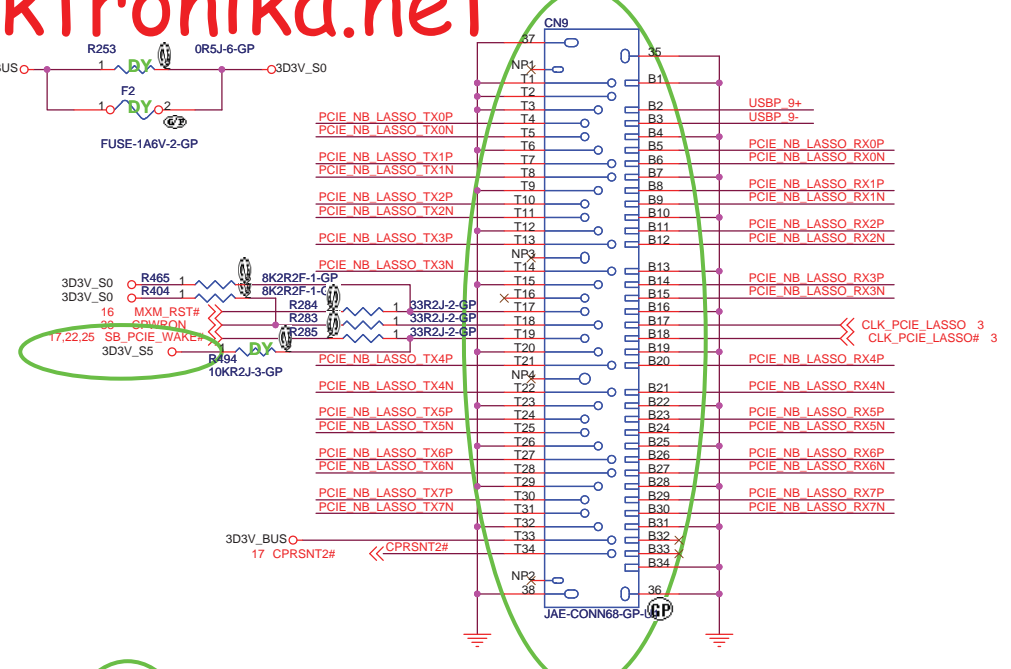
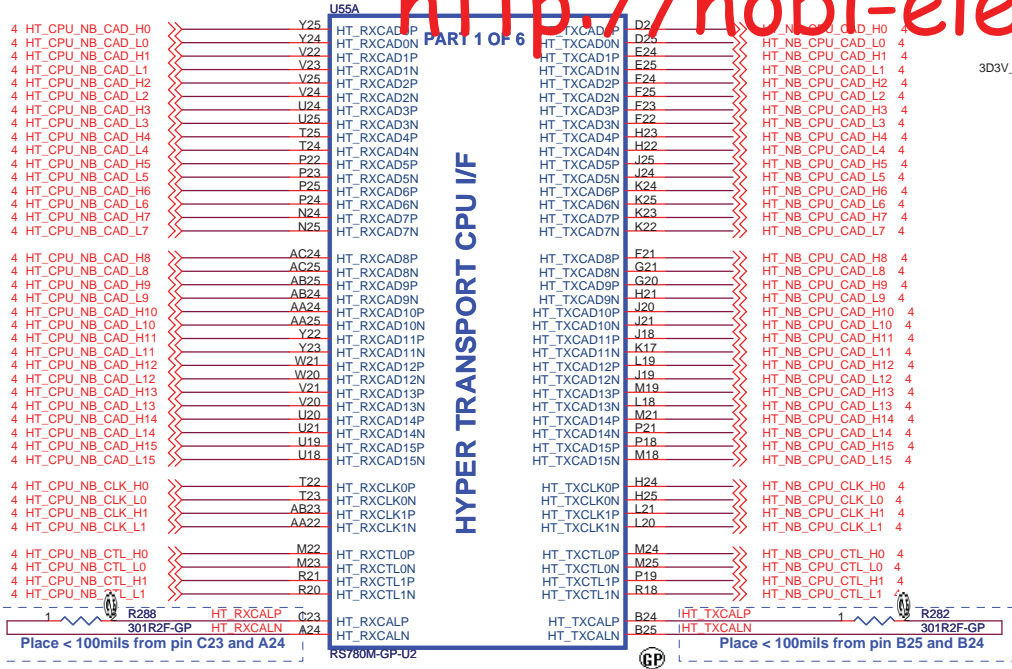
Place these Caps near DM2



Layout Note: **DY** Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



Place C2.2uF and 0.1uF < 500mils from DDR connector



- NEW
- WLAN
- LAN
- CARD

- NEW
- WLAN
- LAN
- CARD

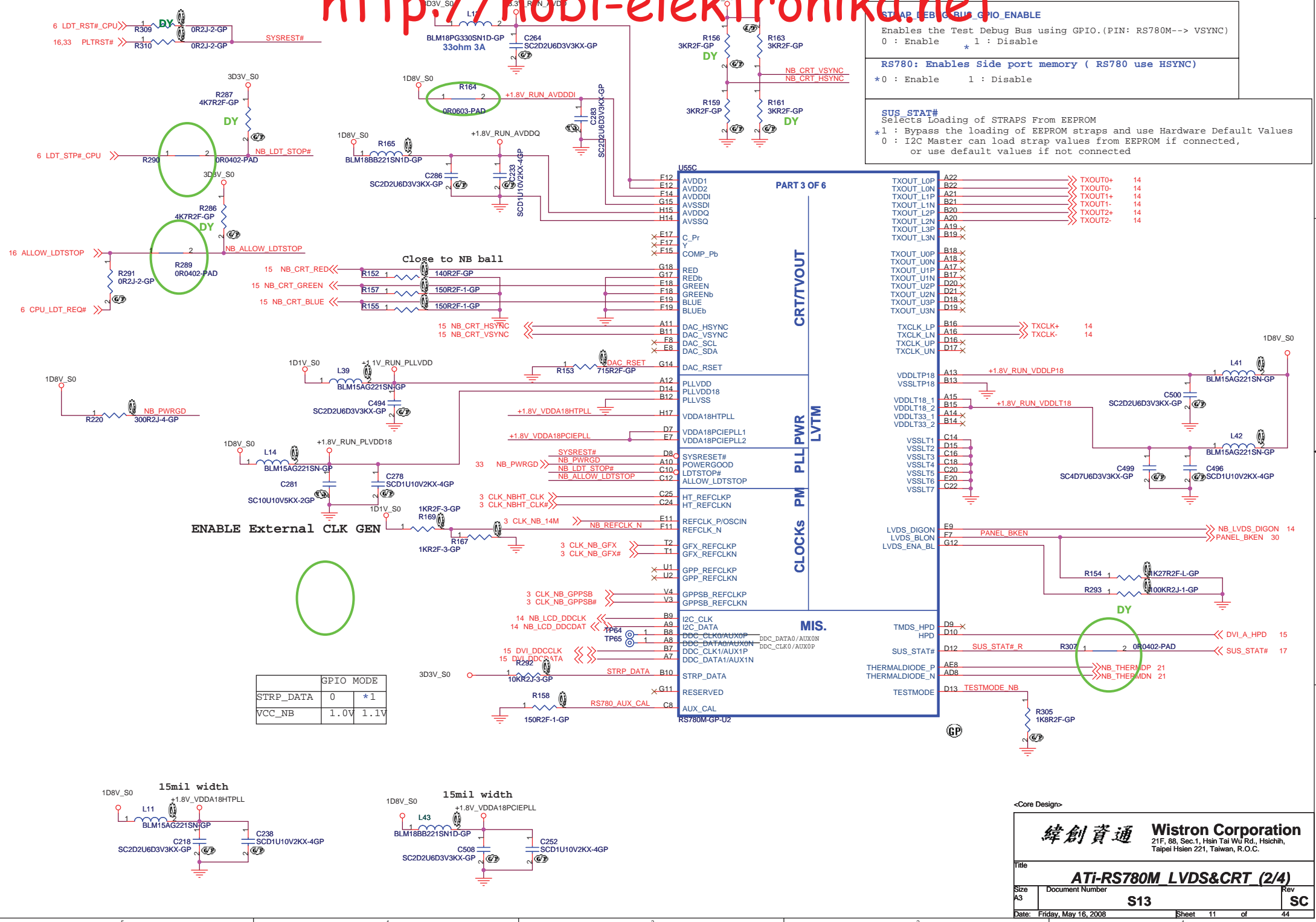
(Core Design)

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **ATI-RS780M HT LINK&PCIE(1/4)**

Size A3 Document Number **S13** Rev **SC**

Date: Friday, May 16, 2008 Sheet 10 of 44



STRAP EEPROM GPIO_ENABLE
 Enables the Test Debug Bus using GPIO. (PIN: RS780M--> VSYNC)
 0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)
 *0 : Enable 1 : Disable

SUS_STAT#
 Selects Loading of STRAPS From EEPROM
 *1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V

<Core Design>

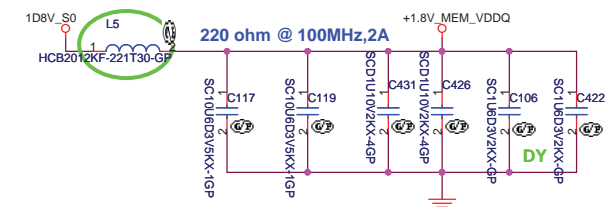
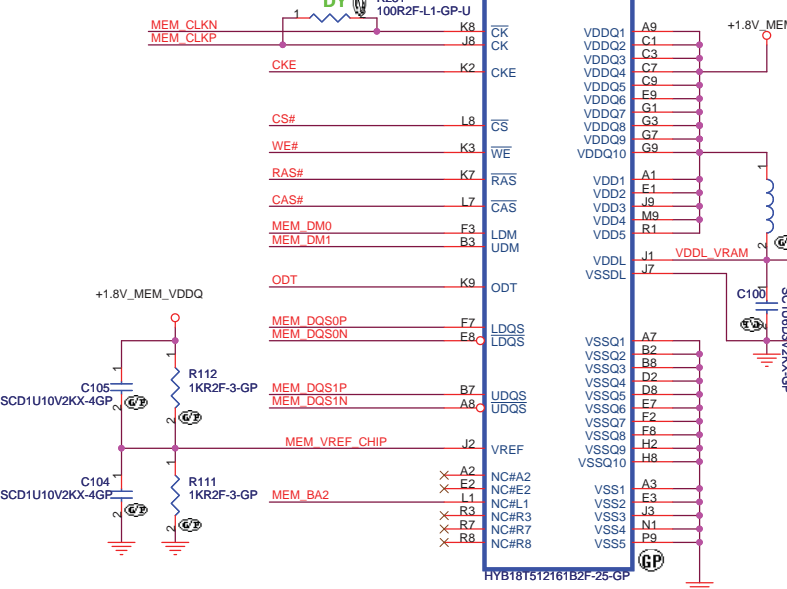
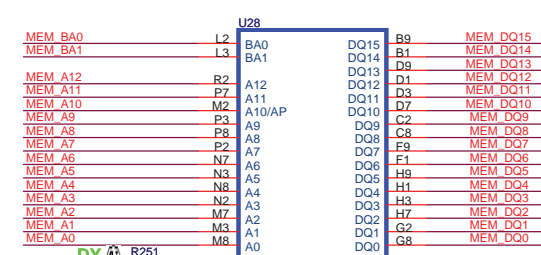
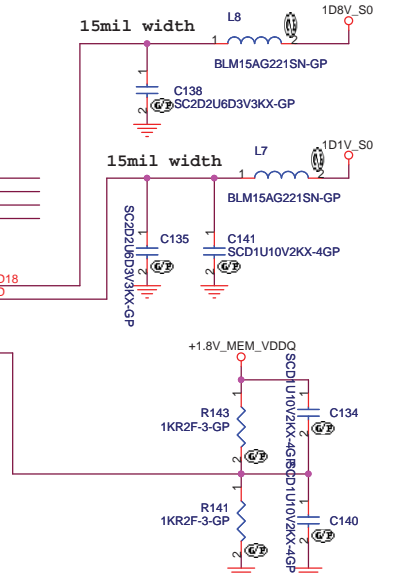
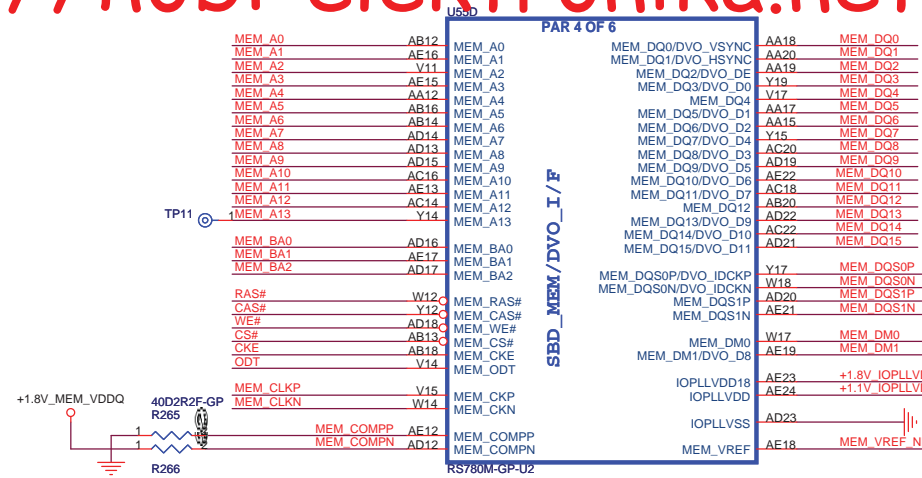
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS780M LVDS&CRT (2/4)**

Size A3 Document Number **S13** Rev **SC**

Date: Friday, May 16, 2008 Sheet 11 of 44

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions



<Core Design>

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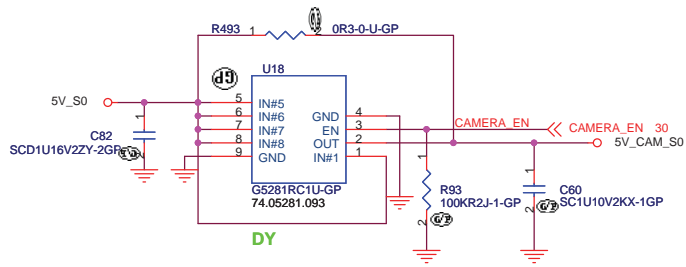
Title: **ATI-RS780M SidePort (3/4)**

Size A3 Document Number **S13** Rev **SC**

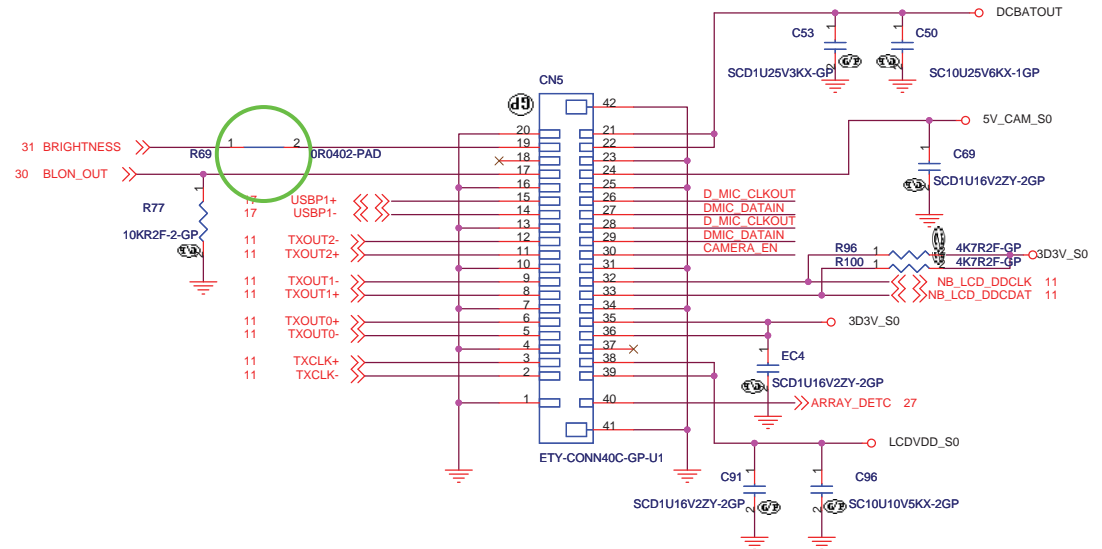
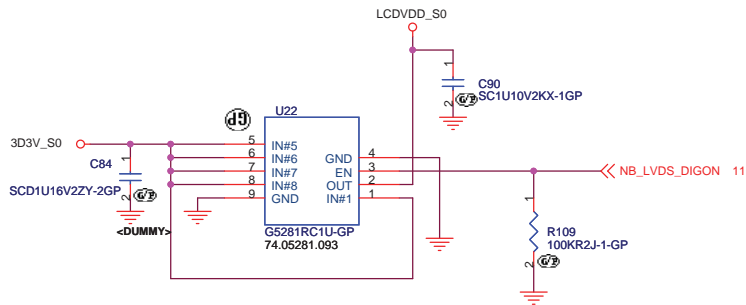
Date: Friday, May 16, 2008 Sheet 12 of 44

LCD CONNECTOR

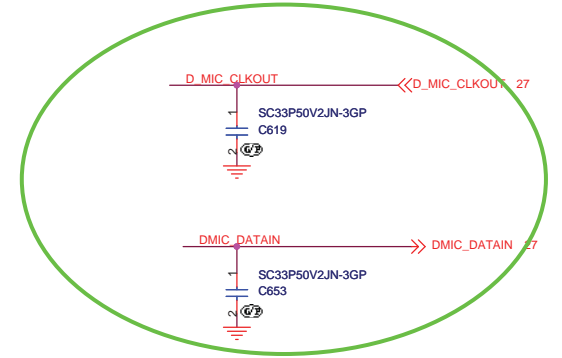
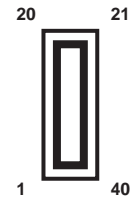
CAMERA POWER



DY



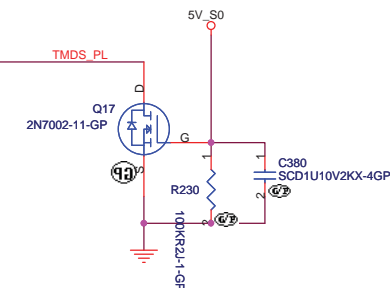
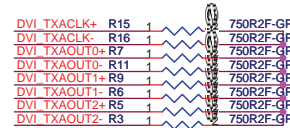
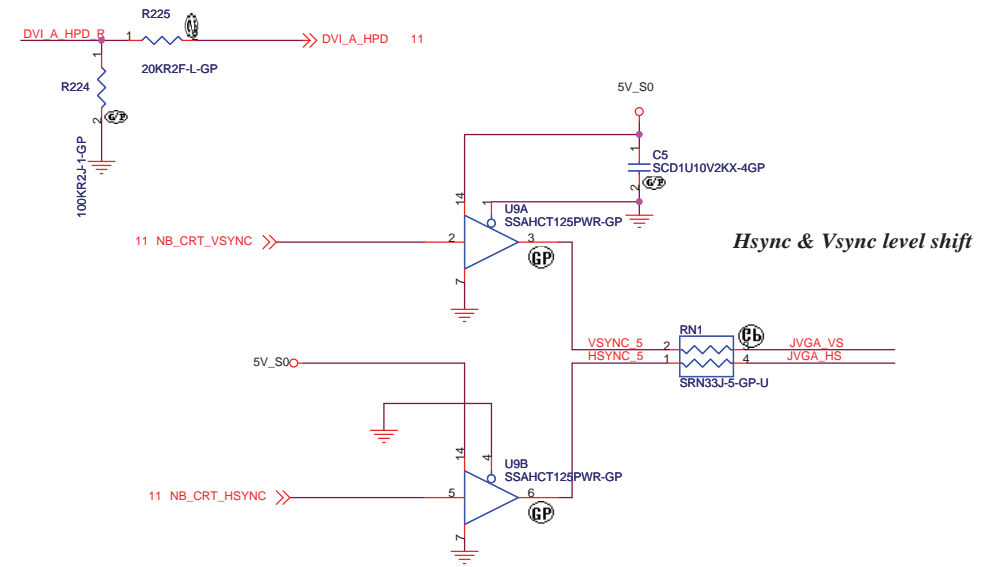
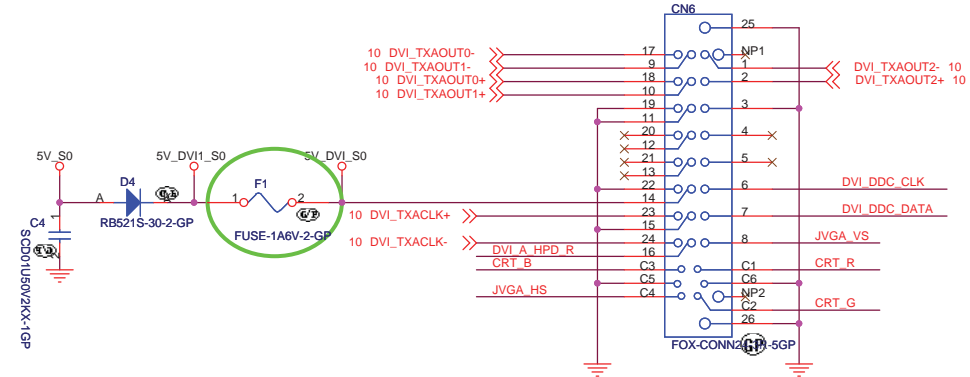
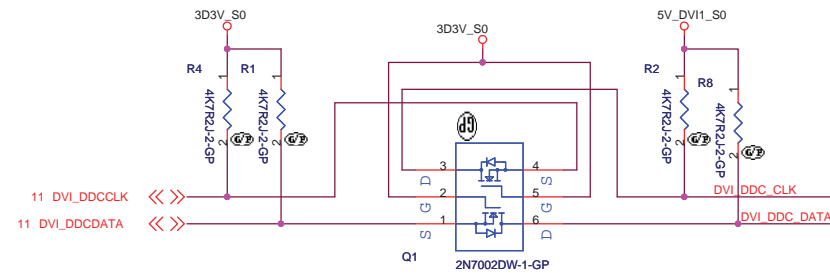
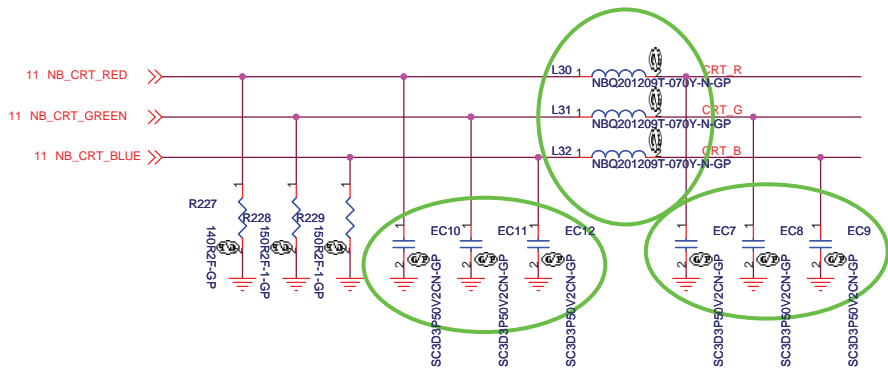
TOP VIEW



<Core Design>

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title LCD CONN/CAMERA</p>	
<p>Size A3</p>	<p>Document Number S13</p>
<p>Date: Friday, May 16, 2008</p>	<p>Rev SC</p>
<p>Sheet 14 of 44</p>	<p>Sheet 14 of 44</p>

Layout Note:
Place these resistors close to the connector



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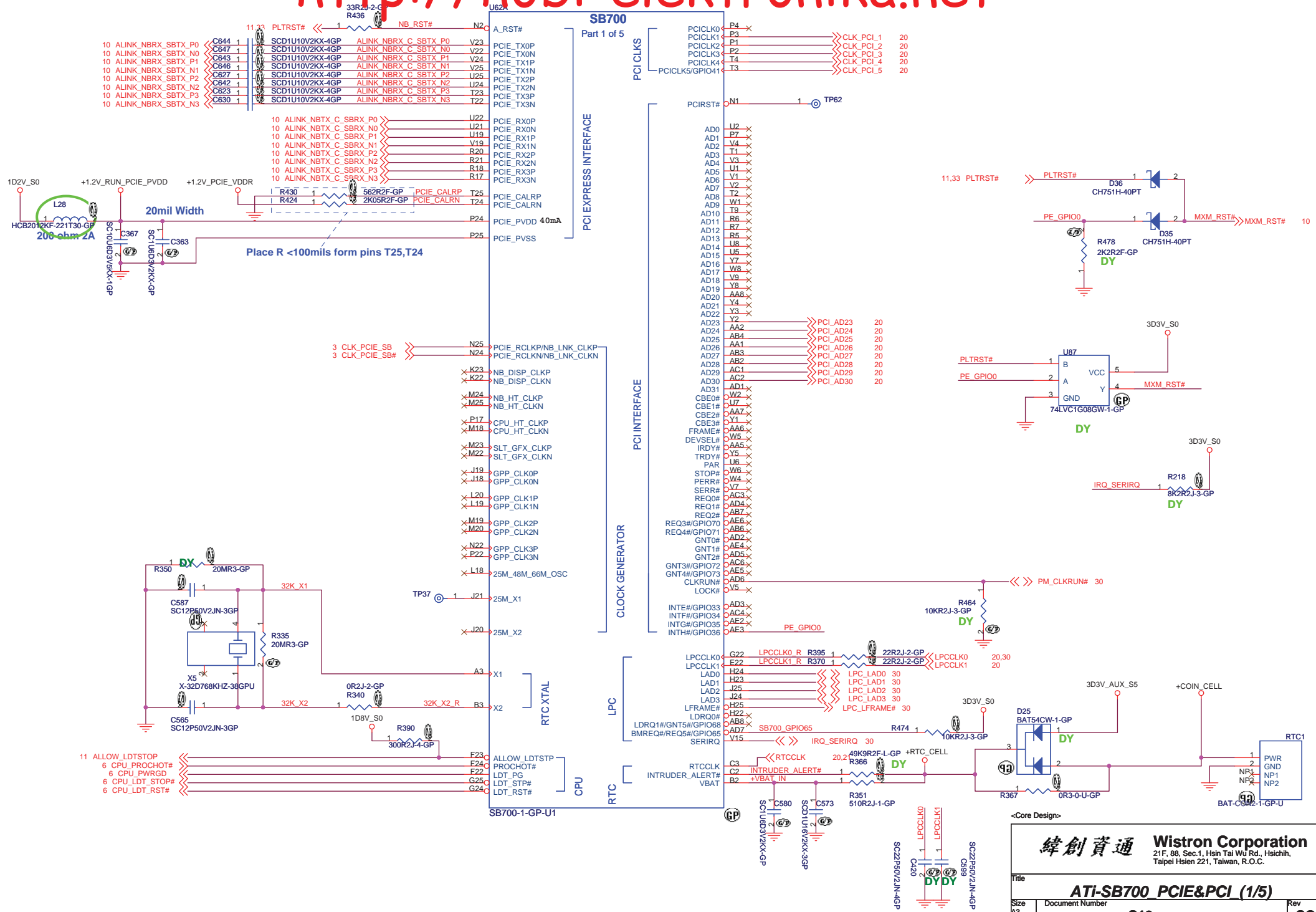
緯創資通

Core Design

Title: **DVI CONN**

Size A3	Document Number S13	Rev SC
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Date: Friday, May 16, 2008 Sheet 15 of 44

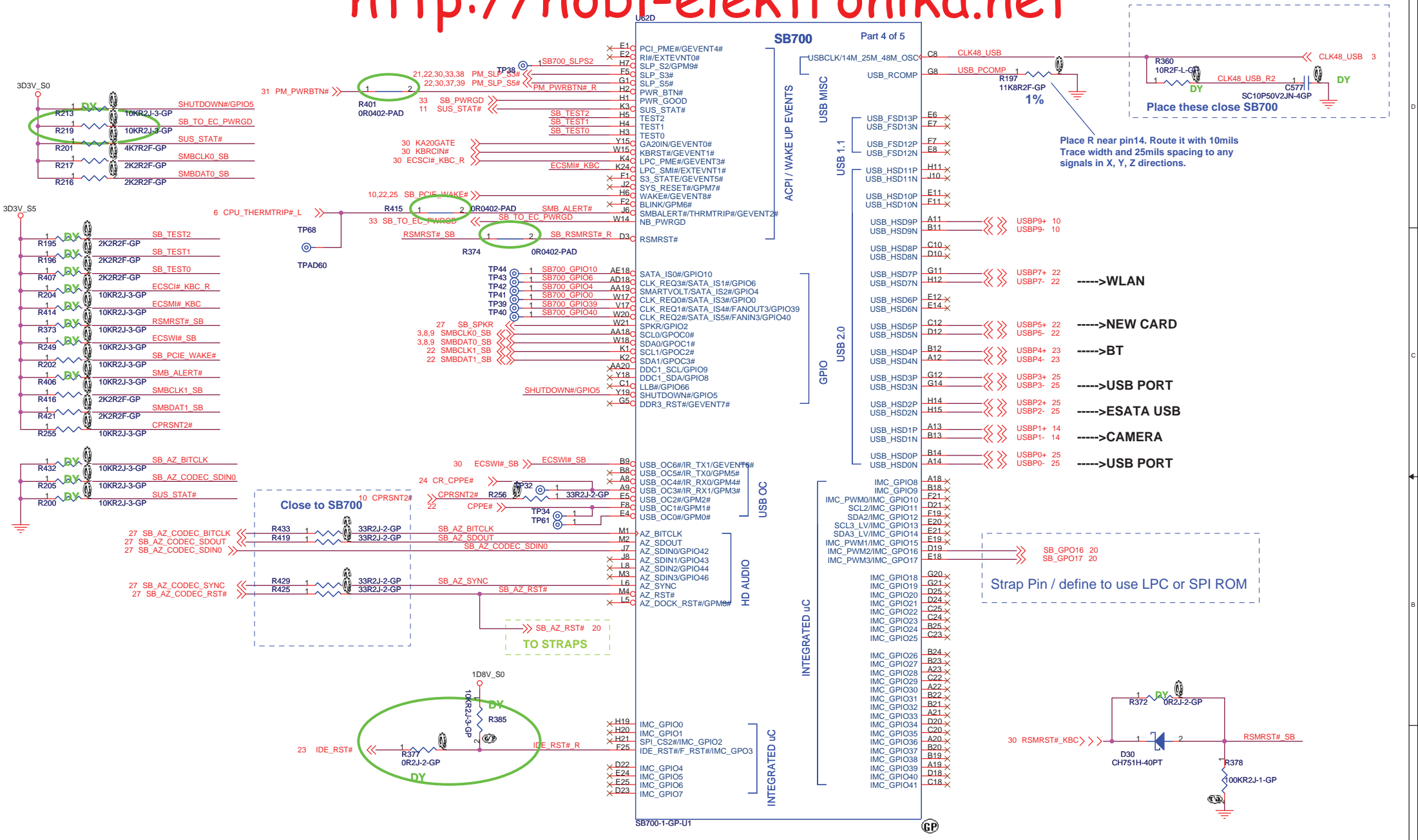


緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **ATI-SB700 PCIE&PCI (1/5)**

Size: A3 Document Number: **S13** Rev: **SC**

Date: Friday, May 16, 2008 Sheet 16 of 44



Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

----->WLAN

----->NEW CARD

----->BT

----->USB PORT

----->ESATA USB

----->CAMERA

----->USB PORT

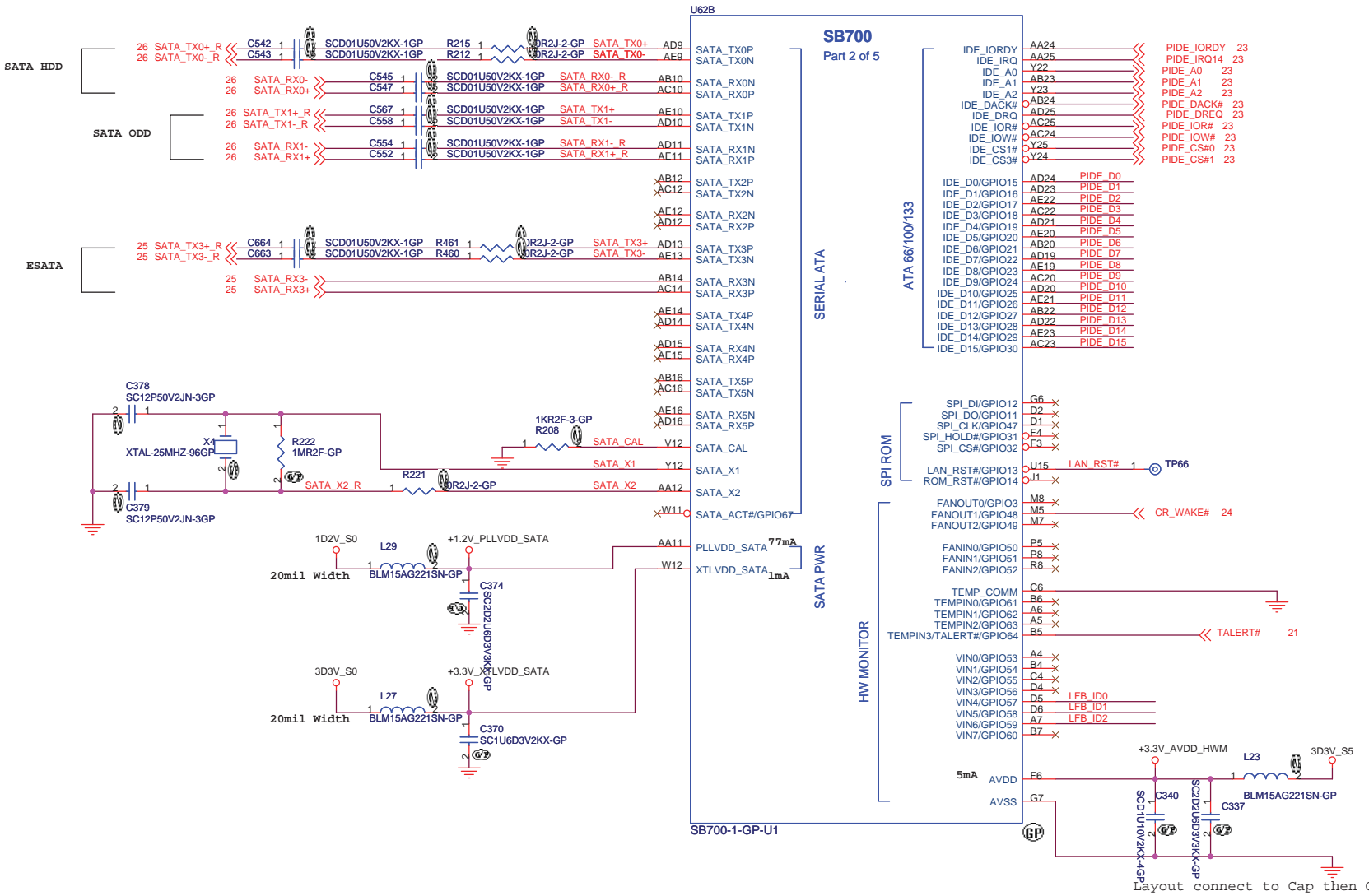
Strap Pin / define to use LPC or SPI ROM

<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

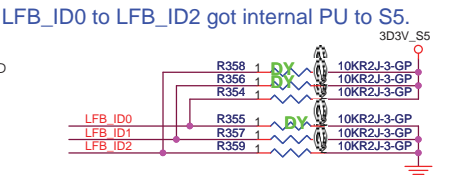
Title: **ATI-SB700 USB&GPIO (2/5)**

Size A3	Document Number S13	Rev SC
Date: Friday, May 16, 2008	Sheet 17 of 44	



Local Frame Buffer Strapping List
Copy from Becks.

	LFB_ID2	LFB_ID1	LFB_ID0
* Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0



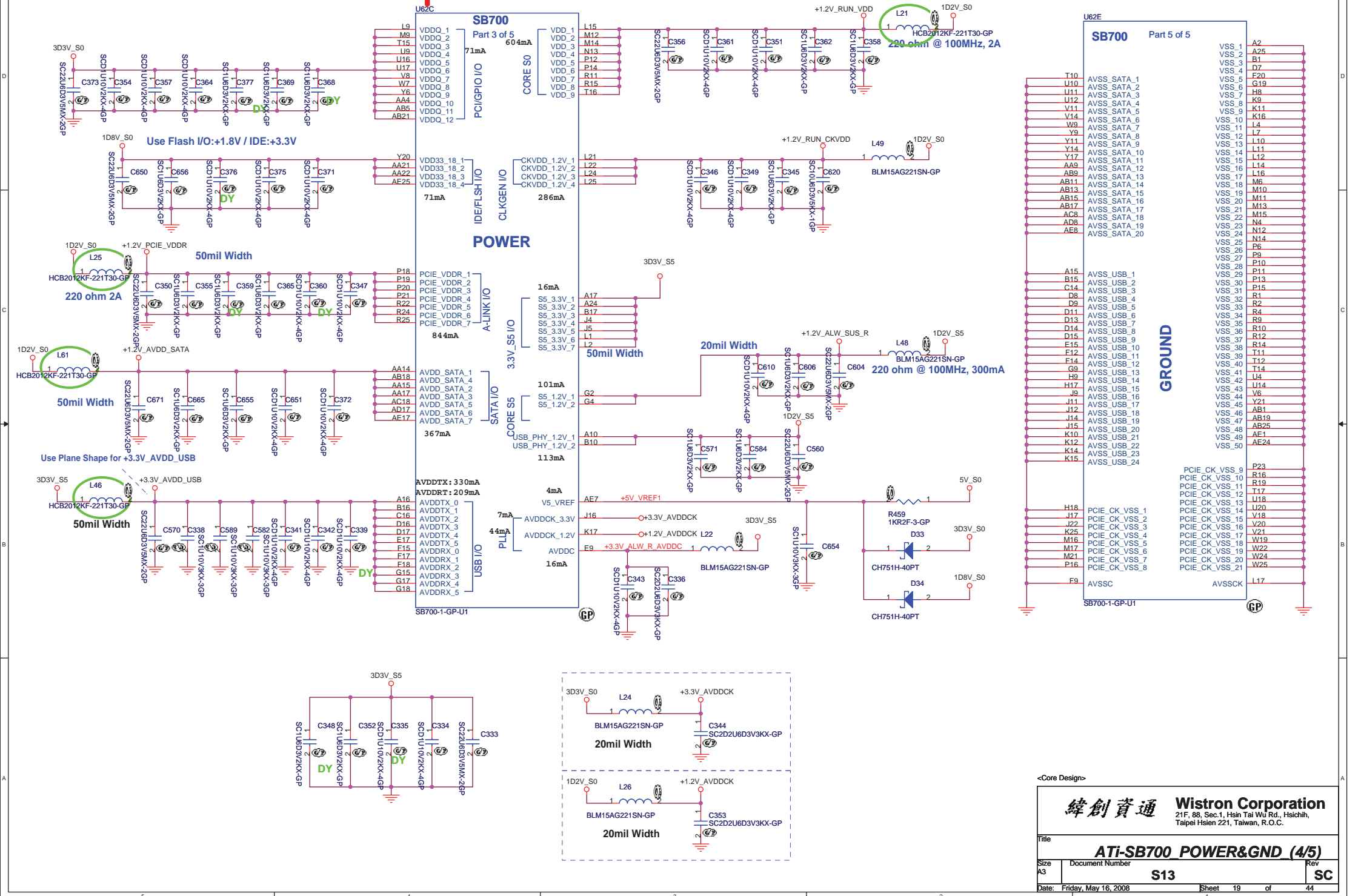
<-Core Design->

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB700 SATA-IDE (3/5)**

Size A3 Document Number **S13** Rev **SC**

Date: Friday, May 16, 2008 Sheet 18 of 44



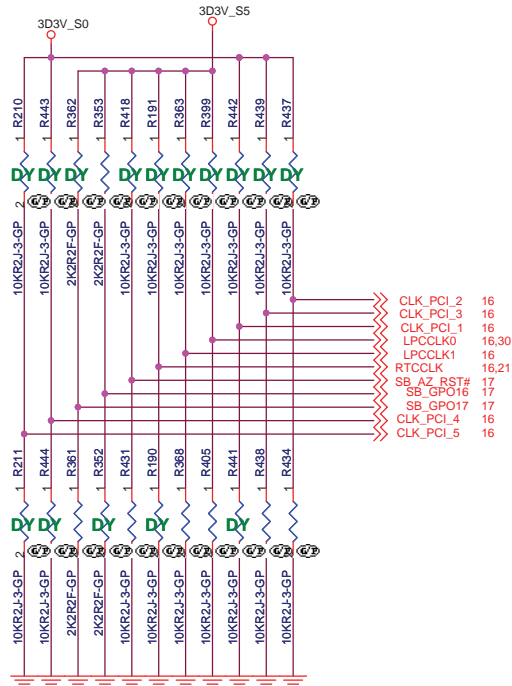
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB700 POWER&GND (4/5)**

Size A3	Document Number	S13	Rev	SC
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REQUIRED STRAPS

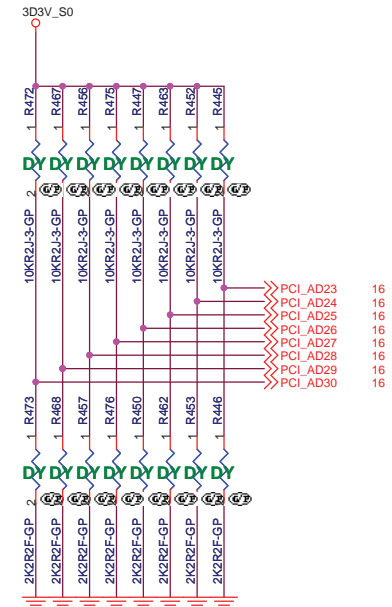


REQUIRED SYSTEM STRAPS

	CLK_PCI_2	CLK_PCI_3	CLK_PCI_4 CLK_PCI_5	LPCCLK0	LPCCLK1	RTCCLK	AZ_RST#	SB_GPO17, SBGPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	IMC ENABLED	ROM TYPE: H, H = Reserved
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	IMC DISABLED DEFAULT	H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	Reserved

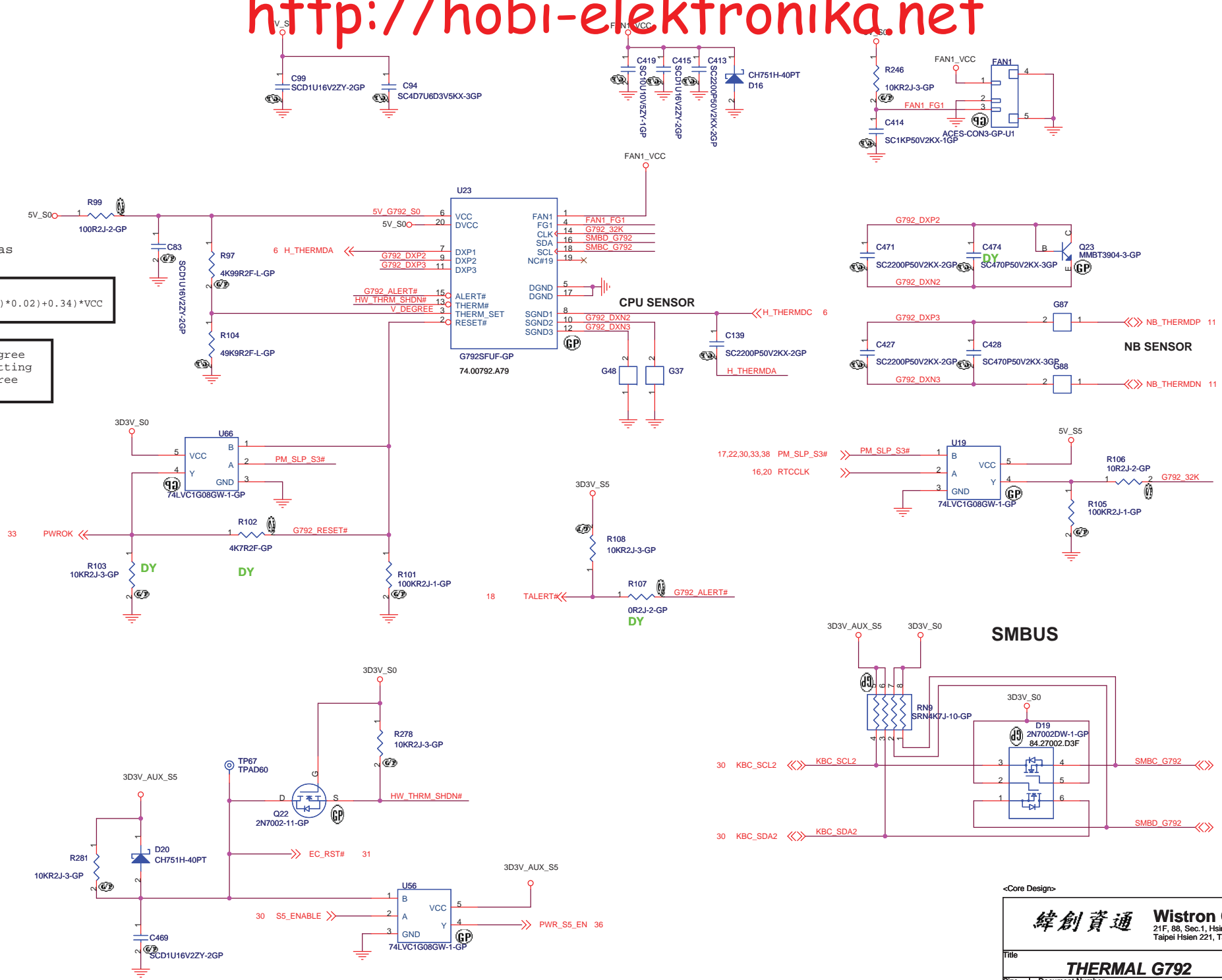
Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

<Core Design>

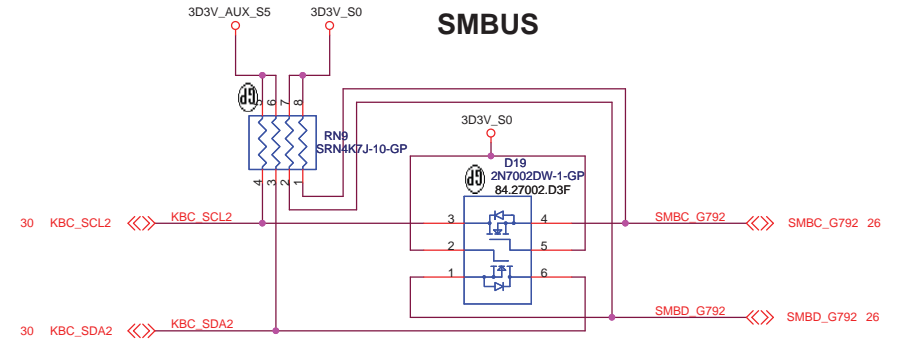
Setting T8 as 100 Degree

$$V_DEGREE = (((Degree-72) * 0.02) + 0.34) * VCC$$

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree



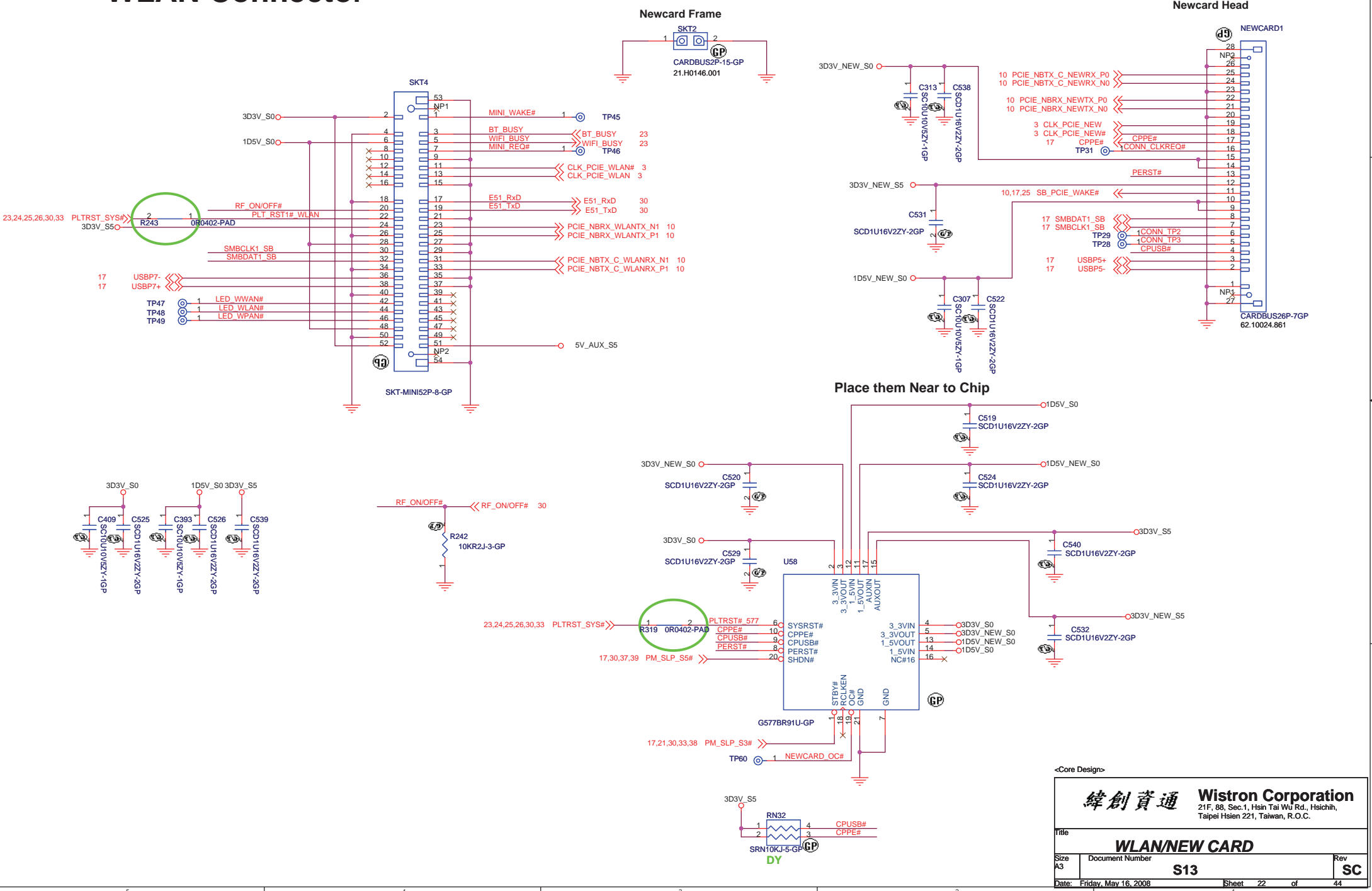
SMBUS



<Core Design>

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THERMAL G792	
Title	Rev
Size A3	SC
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WLAN Connector



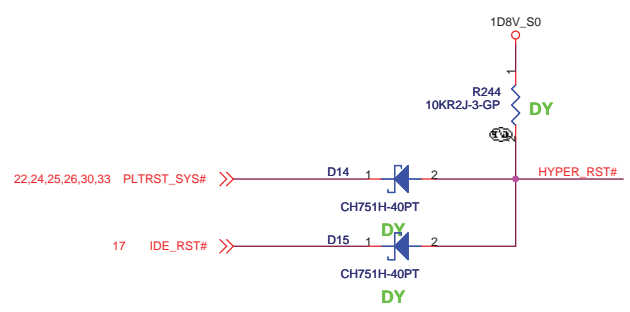
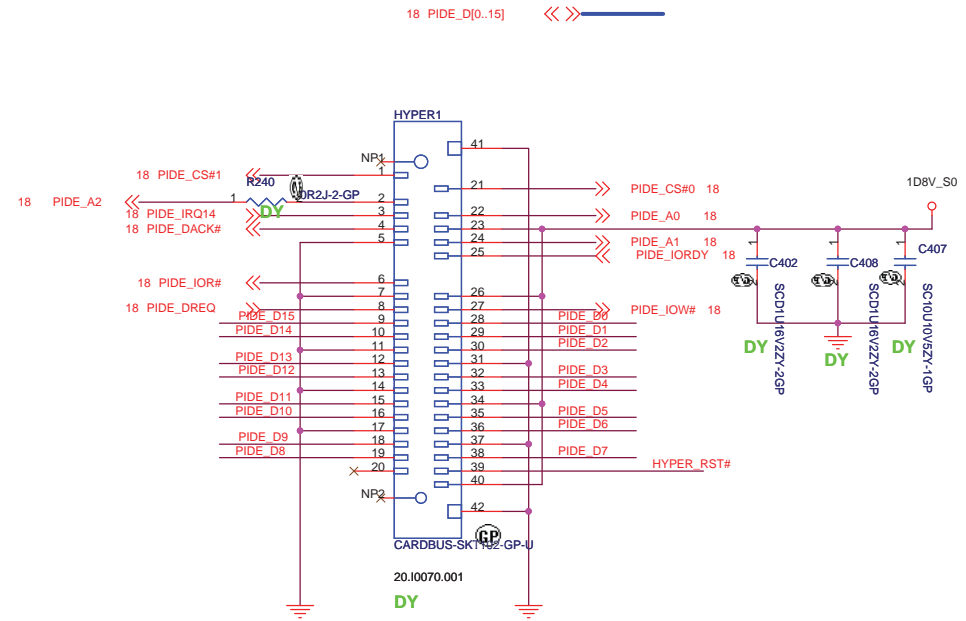
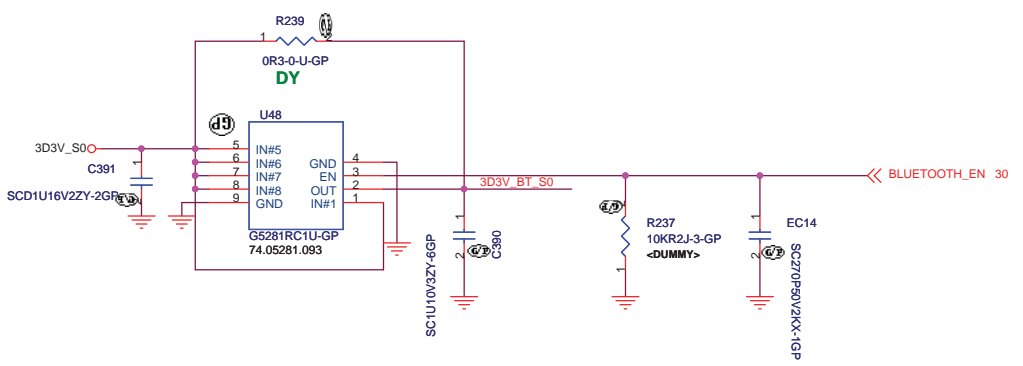
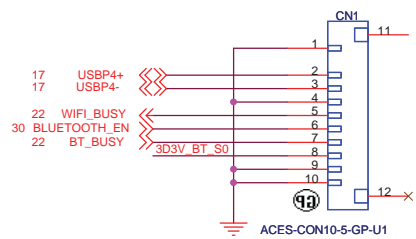
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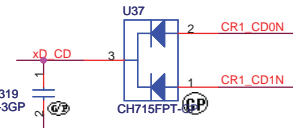
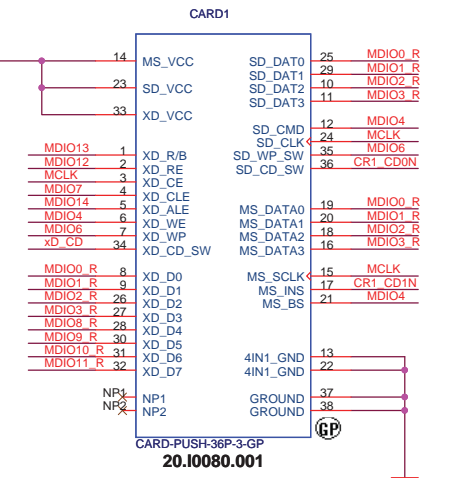
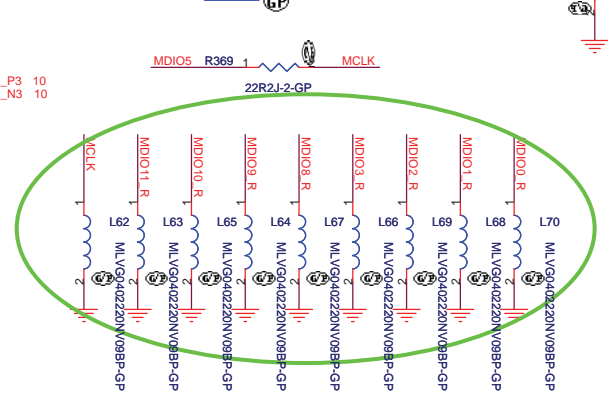
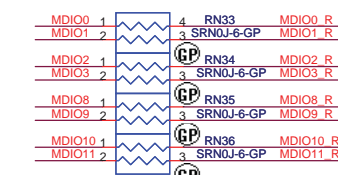
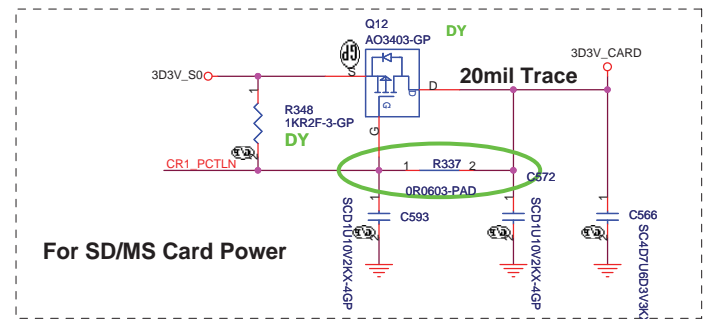
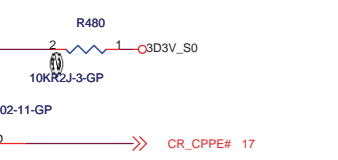
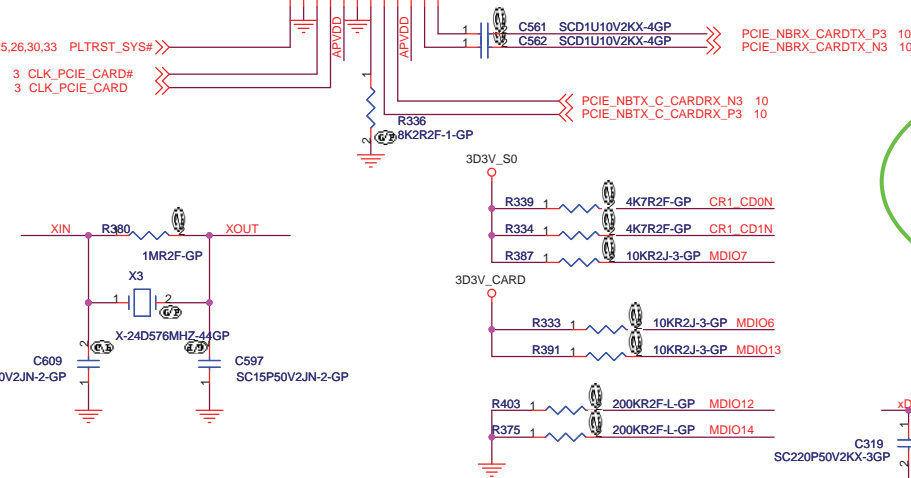
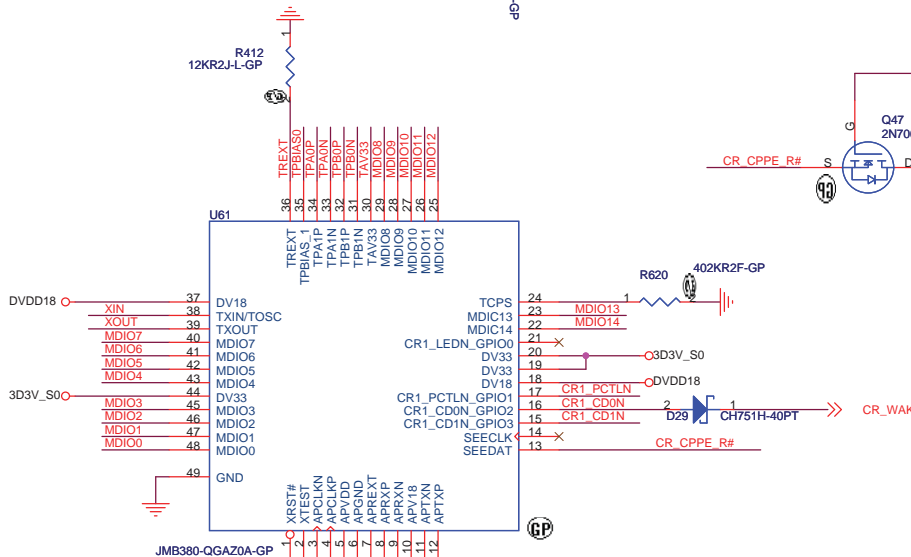
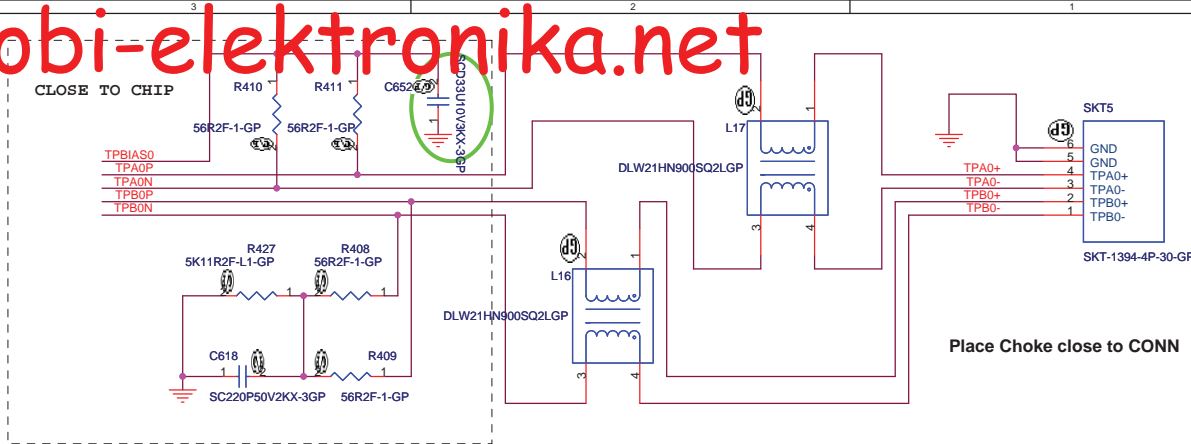
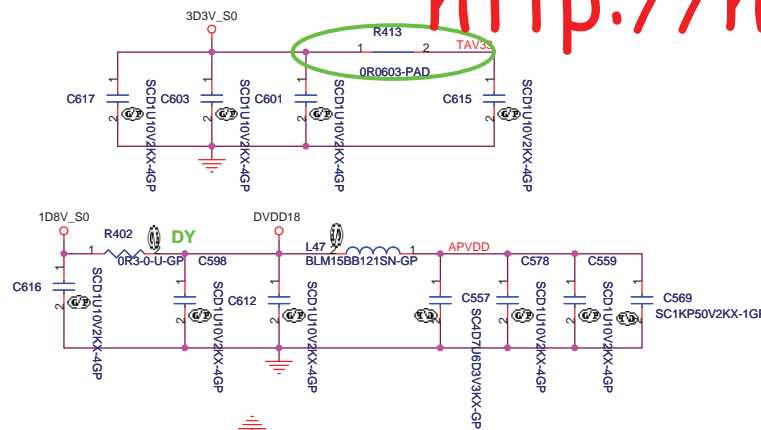
緯創資通 Wistron Corporation
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Title: **WLAN/NEW CARD**

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Bluetooth





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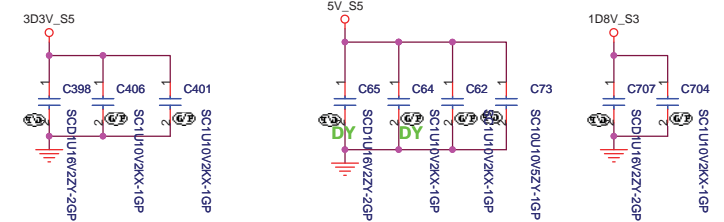
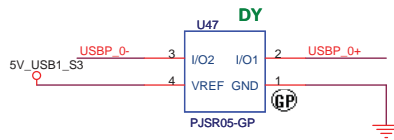
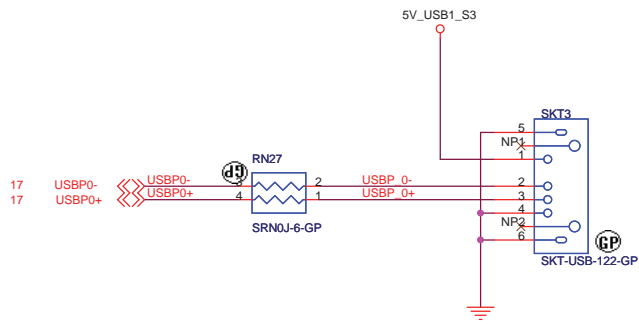
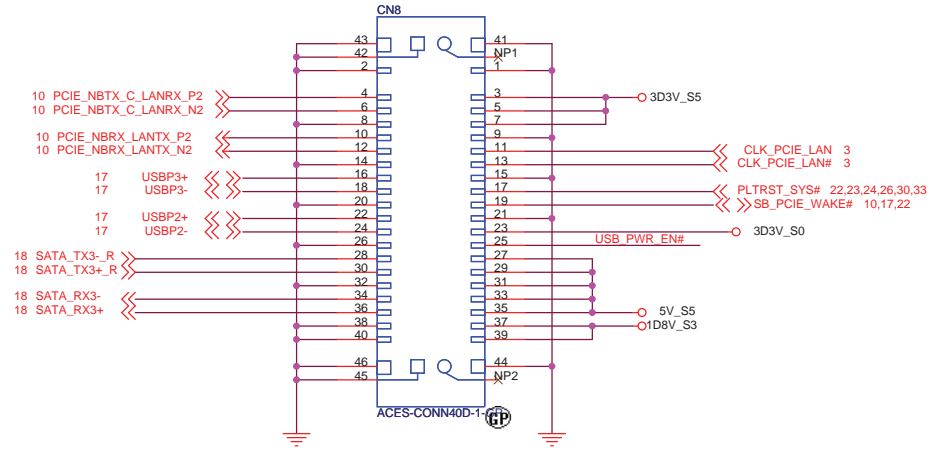
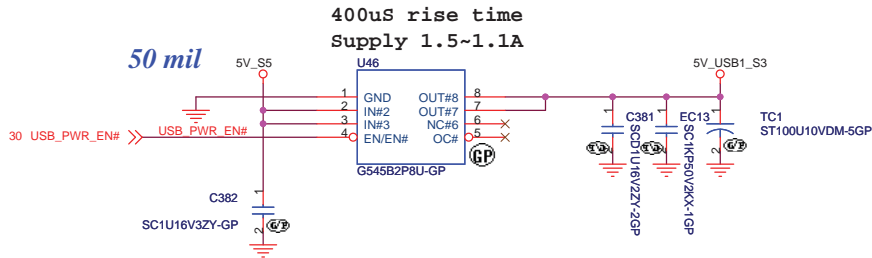
Core Design:
1394/CARD READER

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USB PORT

50 mil



<Core Design>

緯創資通

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Title

USB & DAUGHTER CONN

Size

Document Number

S13

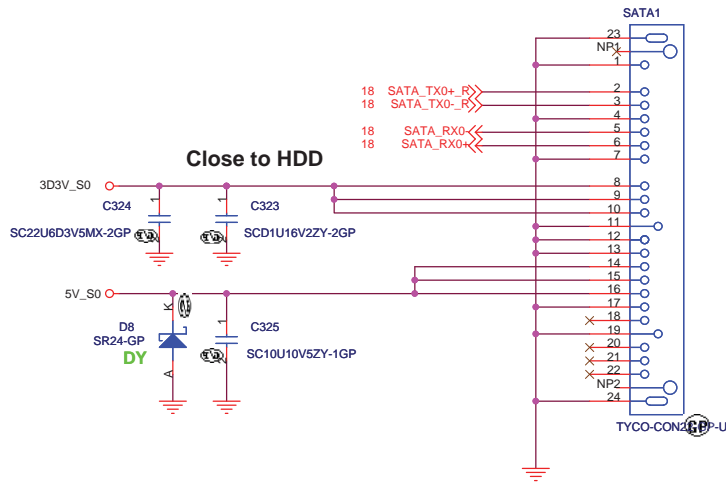
Rev

SC

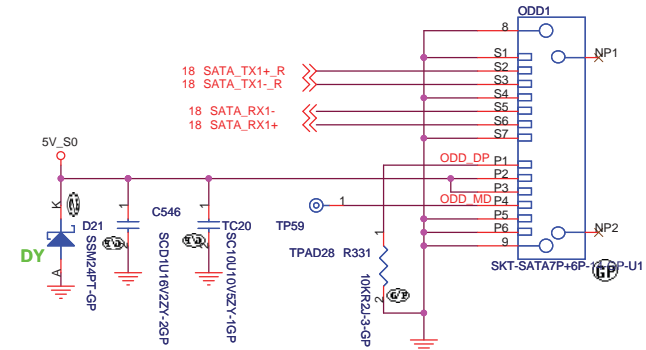
Date: Friday, May 16, 2008

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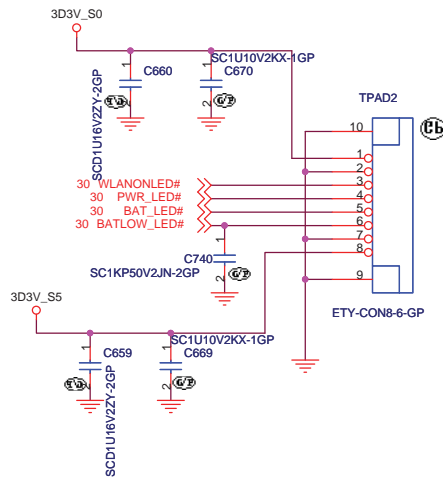
SATA HDD Connector



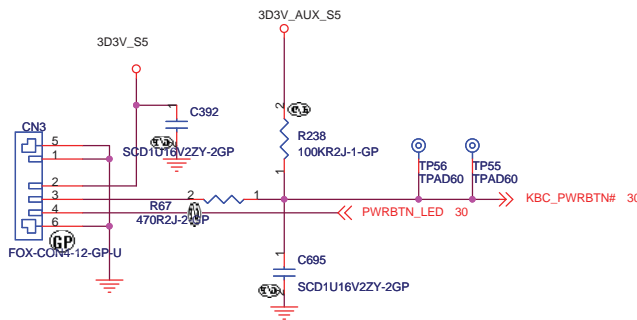
SATA ODD Connector



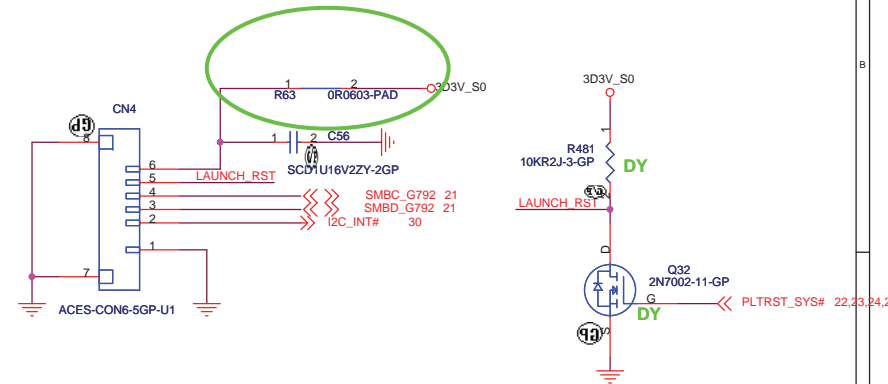
LED BD CONN



PWRBTN BD CONN

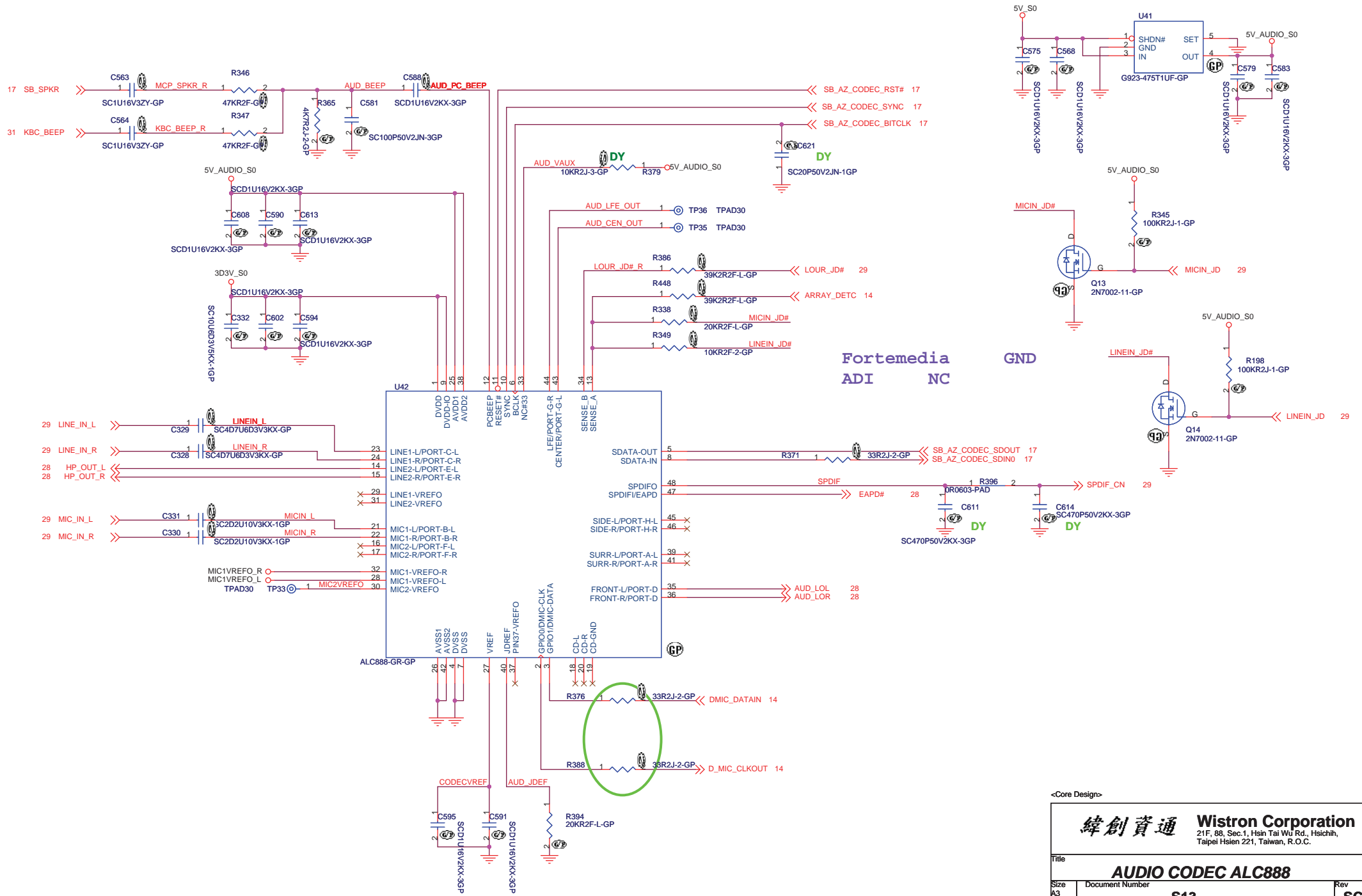


LAUNCH BD CONN



<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HDD/CDROM/LED/LAUNCH			
Title	Document Number		Rev
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<Core Design>

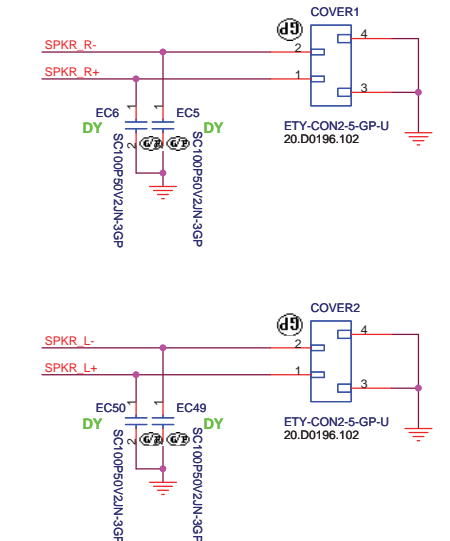
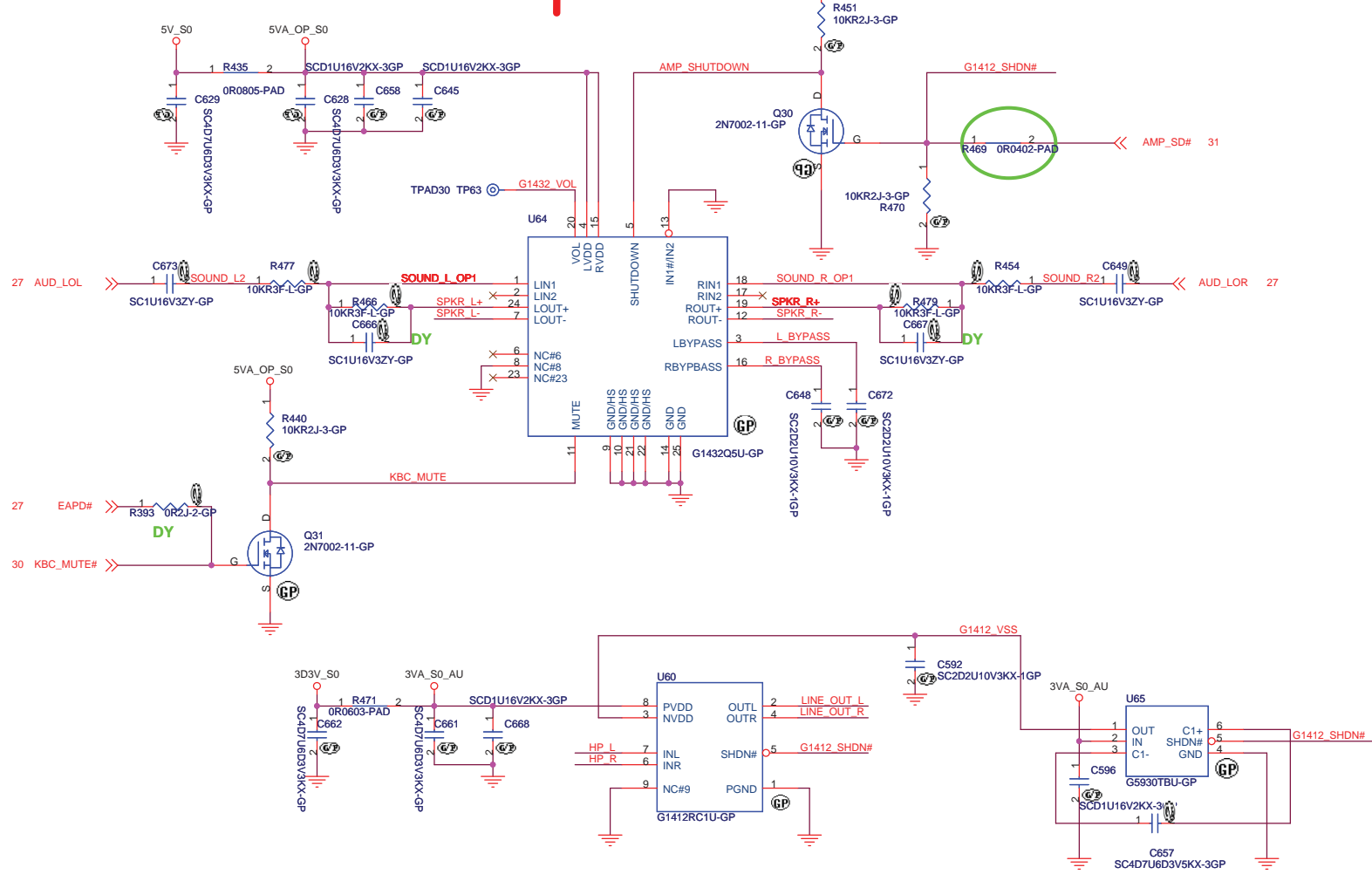
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC ALC888**

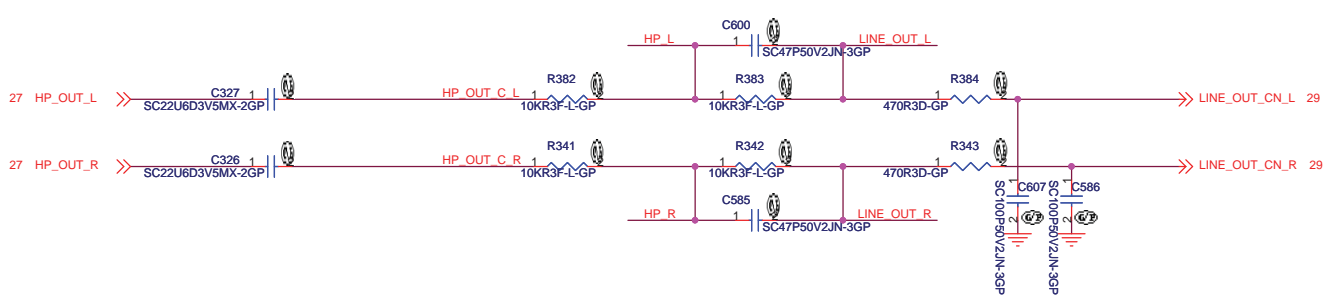
Size A3 Document Number **S13** Rev **SC**

Date: Friday, May 16, 2008 Sheet 27 of 44

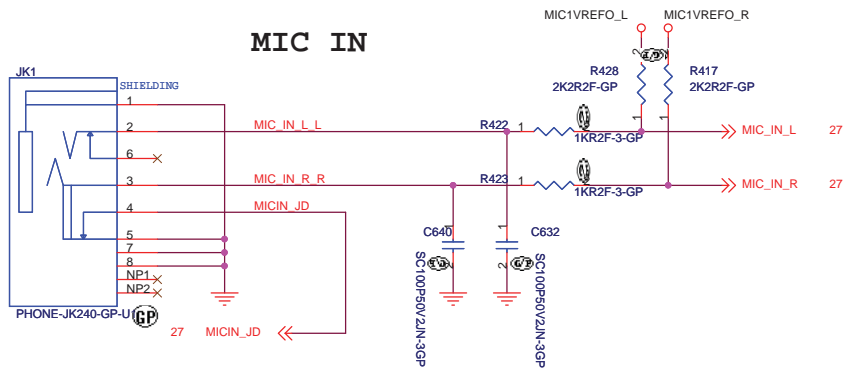
Internal Speaker



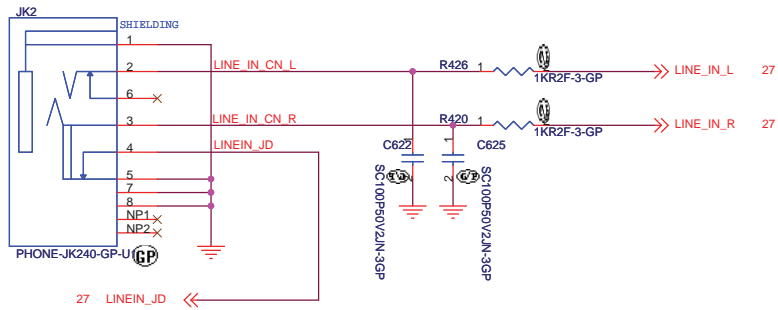
LINE Out



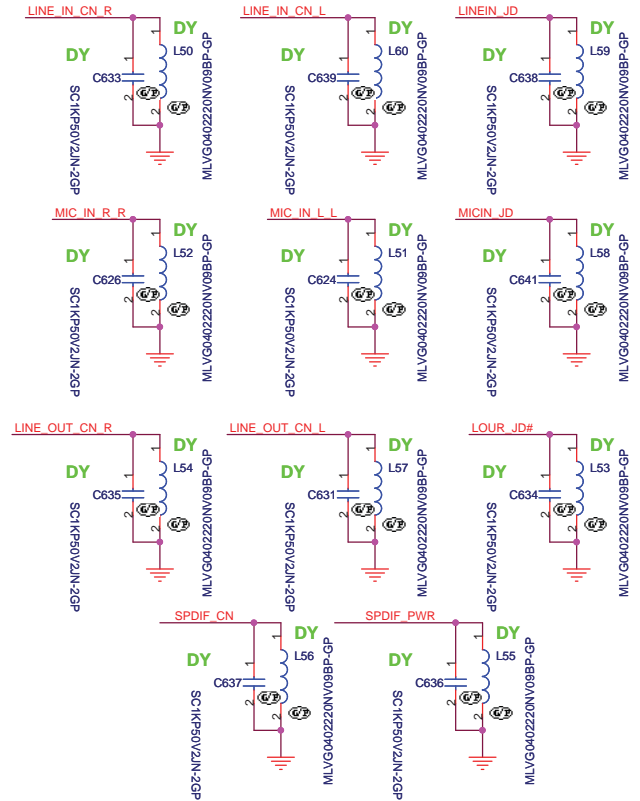
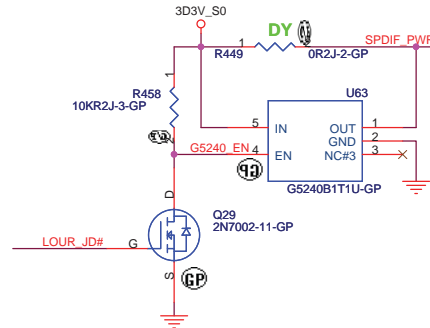
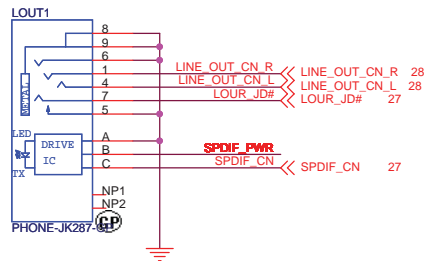
MIC IN



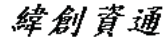
LINE IN

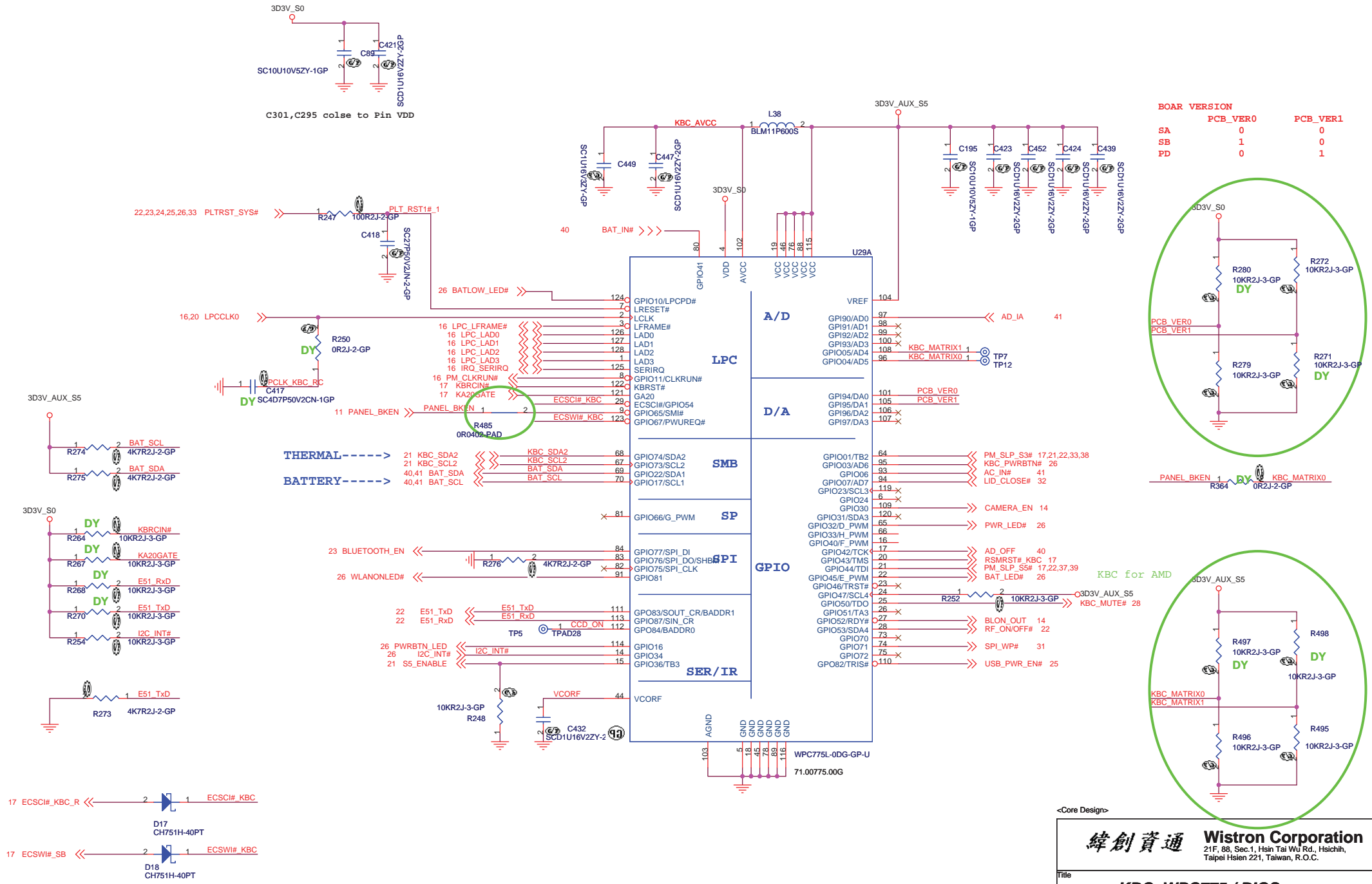


SPDIF / LINE OUT



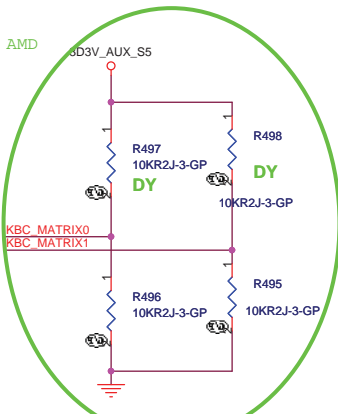
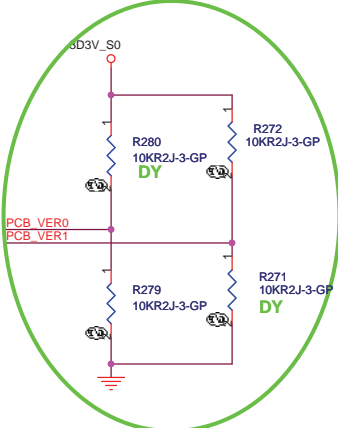
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 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
AUDIO CONN/SUBWOOFER		
Title		
Size	Document Number	Rev
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Date:	Friday, May 16, 2008	Sheet 29 of 44



BOARD VERSION

	PCB_VER0	PCB_VER1
SA	0	0
SB	1	0
PD	0	1



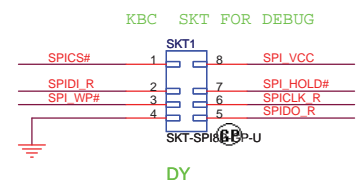
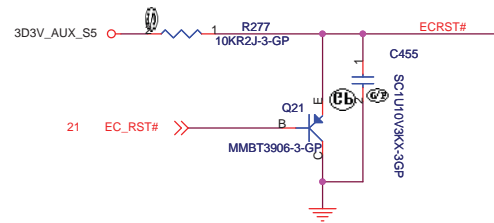
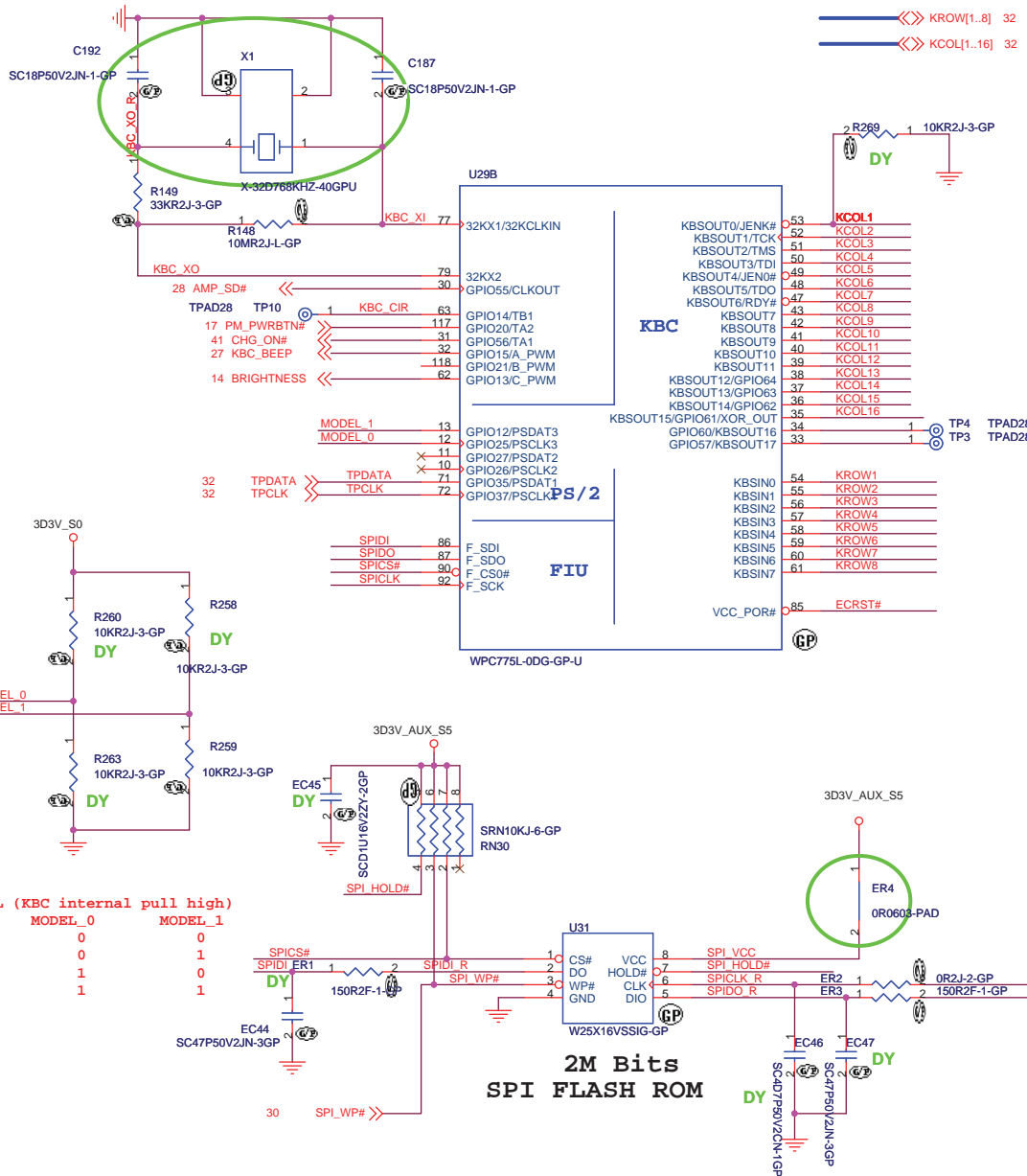
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC WPC775 / BIOS**

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MODEL (KBC internal pull high)

	MODEL_0	MODEL_1
X17	0	0
P15	0	1
S13	1	0
P1	1	1

**2M Bits
SPI FLASH ROM**

<Core Design>

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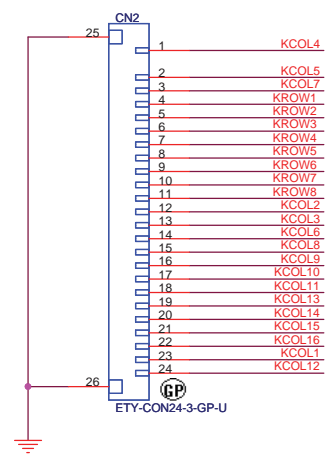
Title: **KBC WPC775 / BIOS(2/2)**

Size A3	Document Number S13	Rev SC
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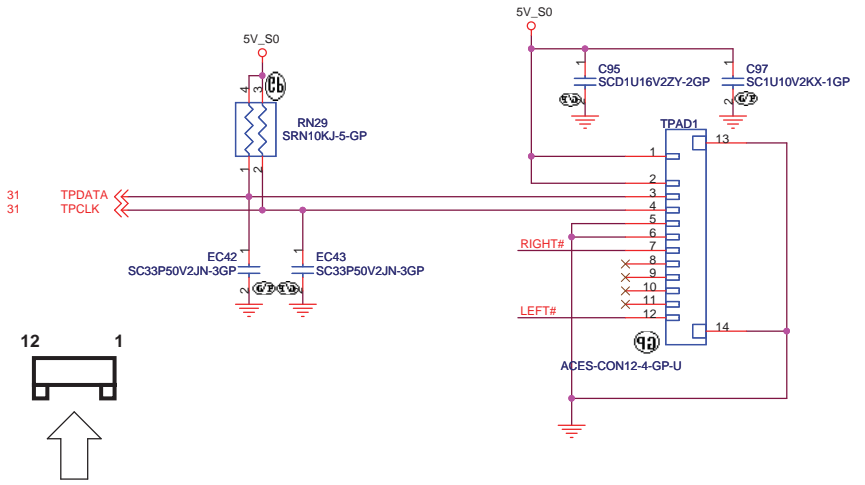
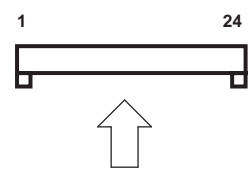
Date: Friday, May 16, 2008 Sheet 31 of 44

TouchPad Connector

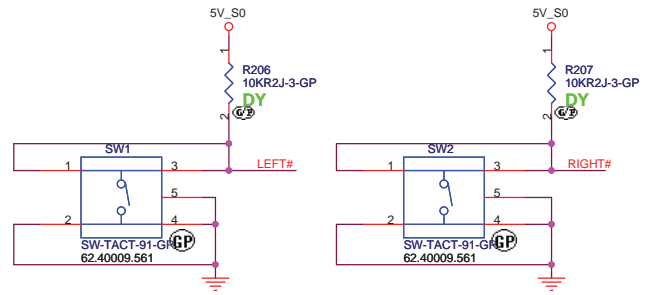
Internal KeyBoard Connector



⟷ KROW[1..8] 31
 ⟷ KCOL[1..16] 31

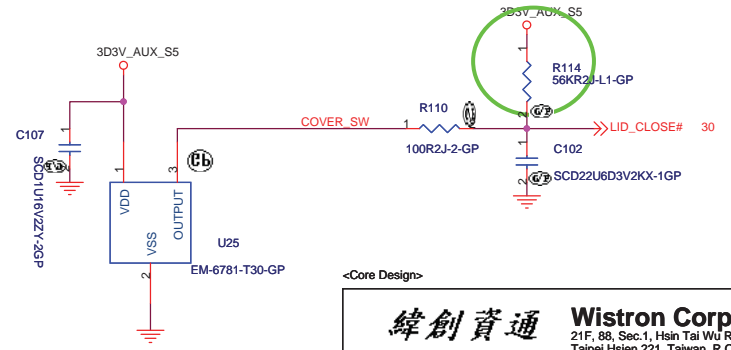


TOUCHPAD BUTTON SWITCH

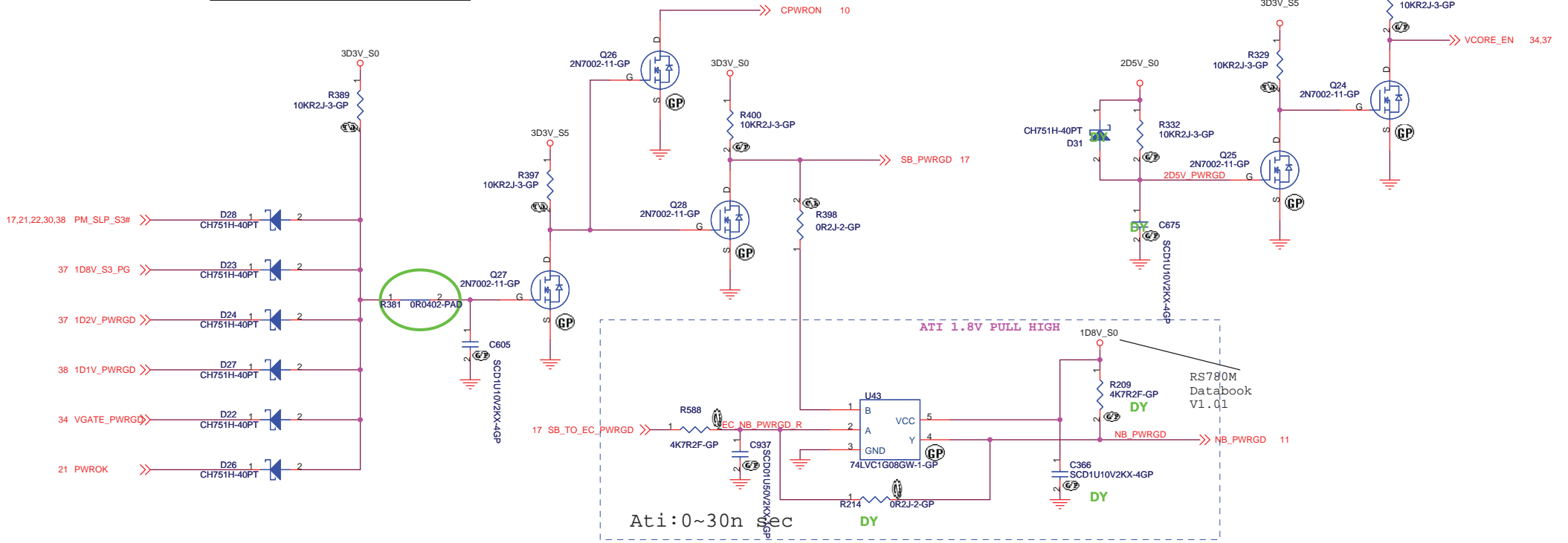


GOLDEN FINGER FOR DEBUG BOARD

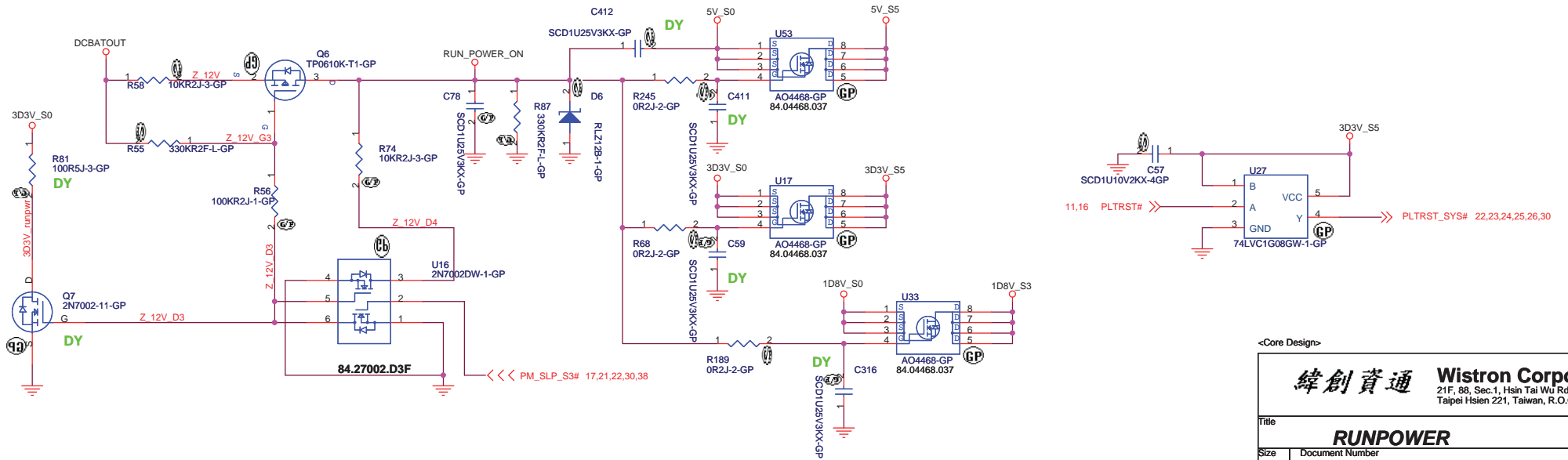
COVER SWITCH

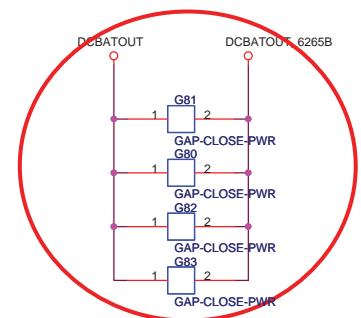
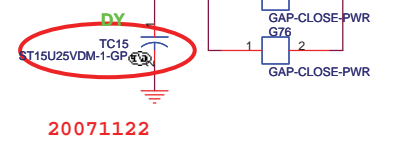
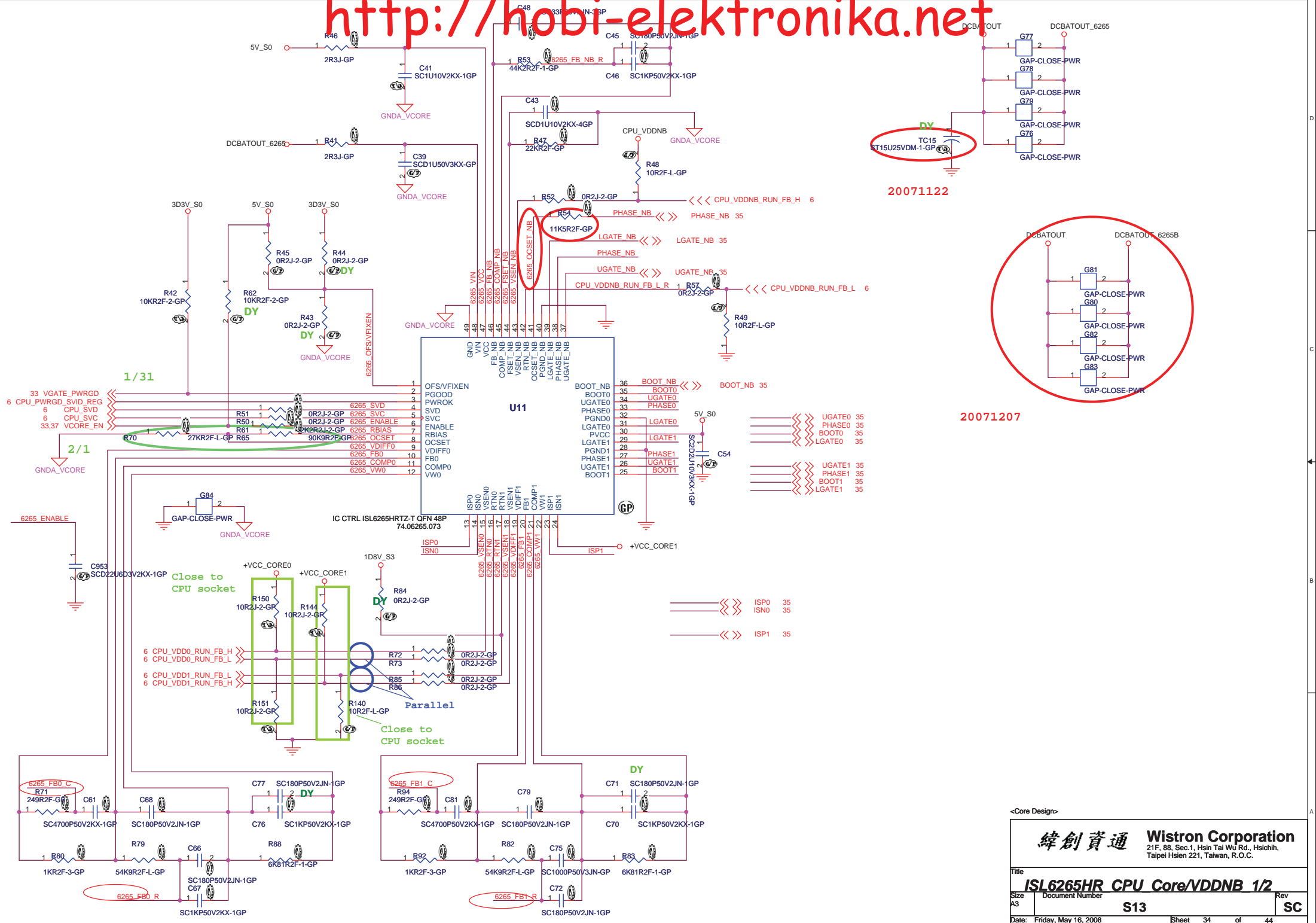


NB_SB POWERGOOD CIRCUIT



Run Power





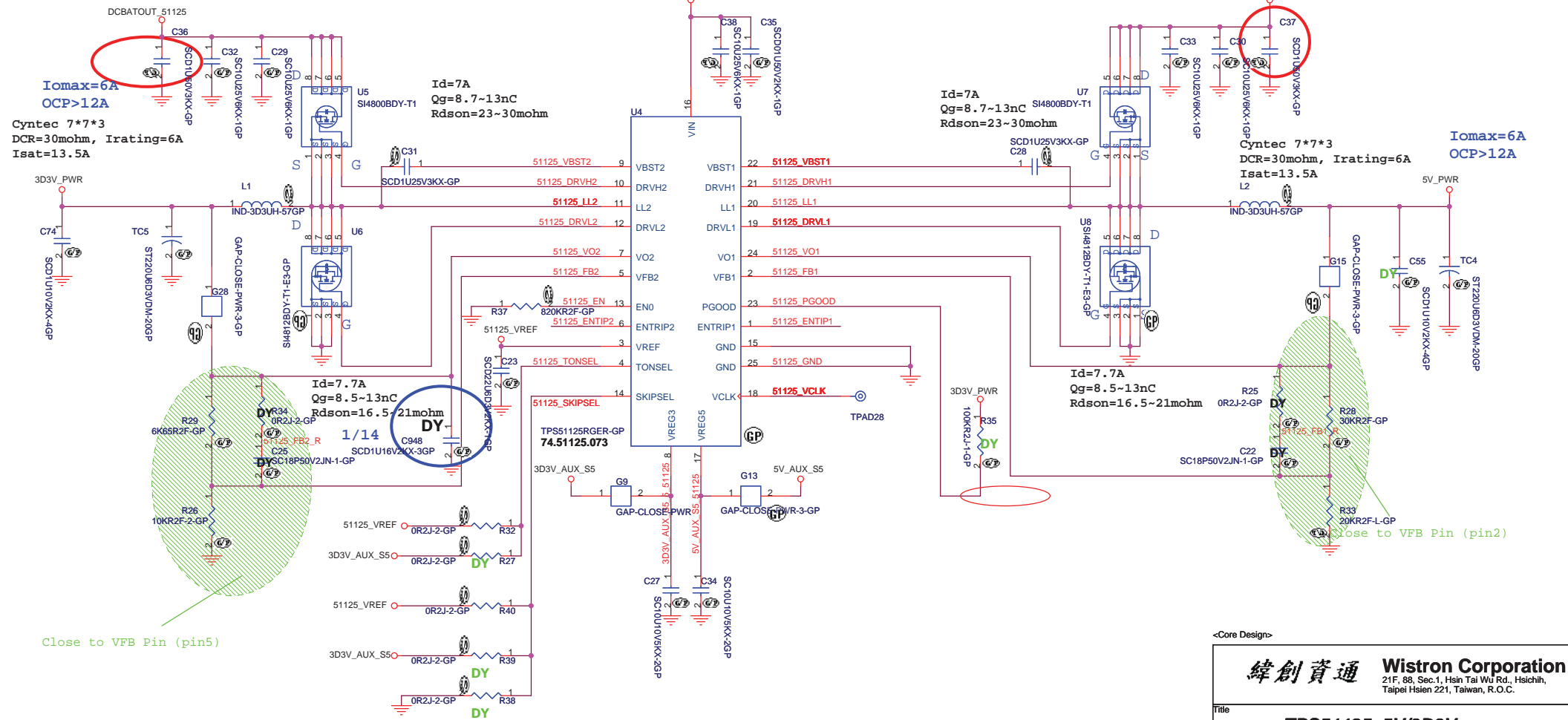
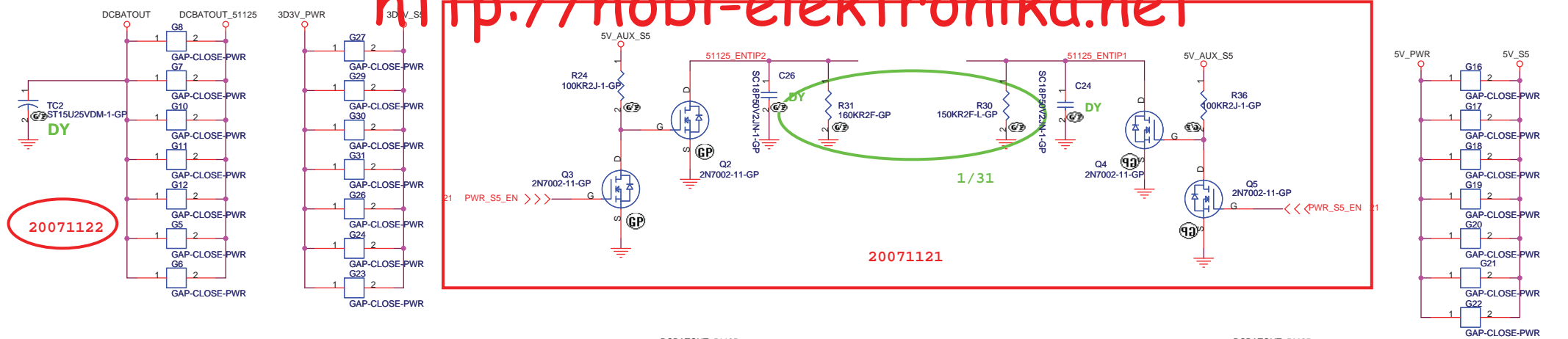
<Core Design>

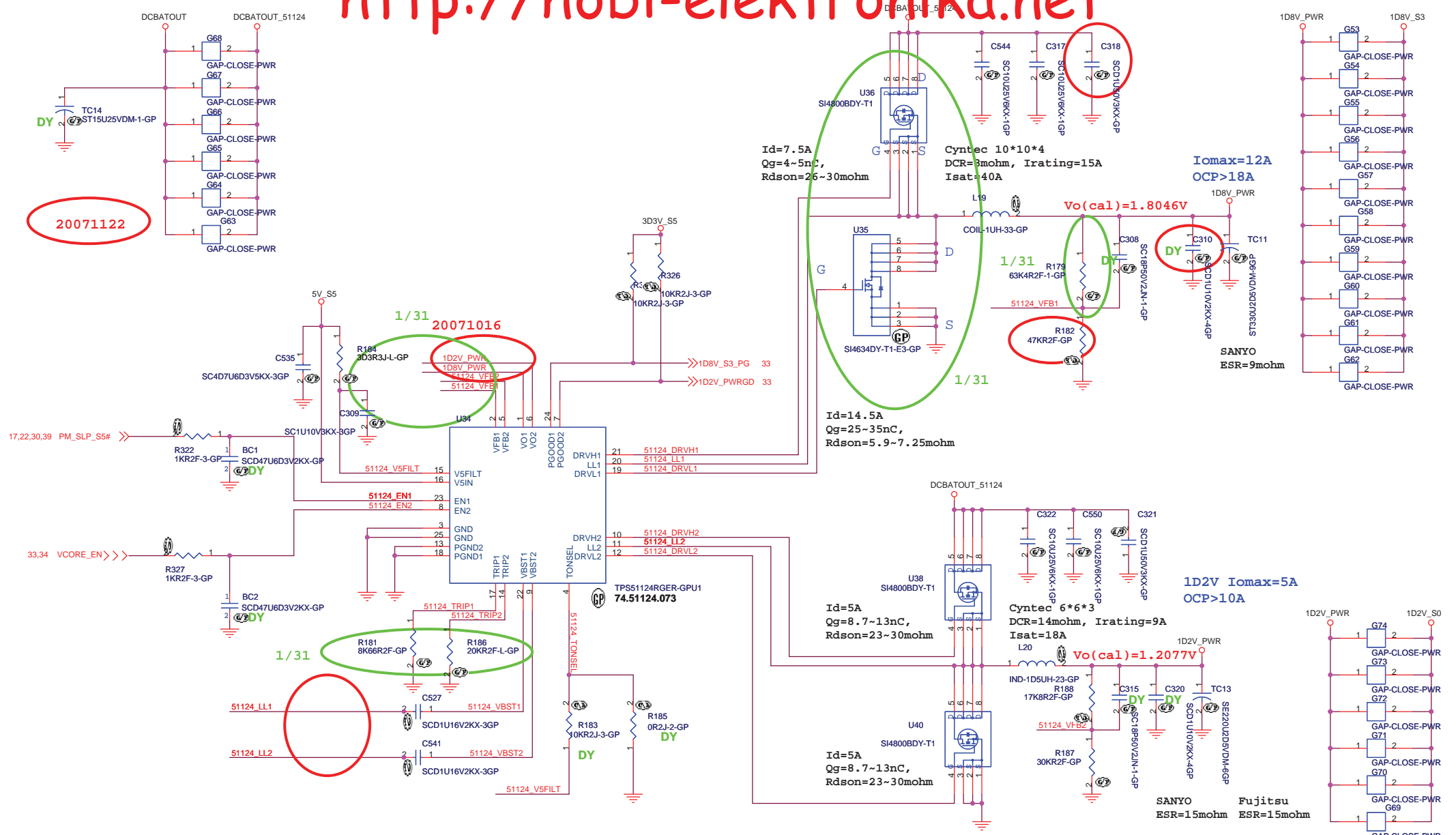
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL6265HR CPU Core/VDDNB 1/2**

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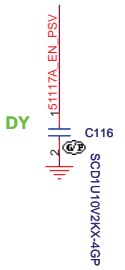
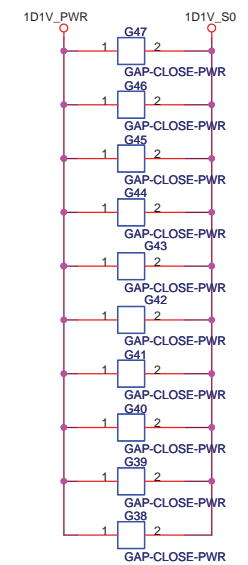
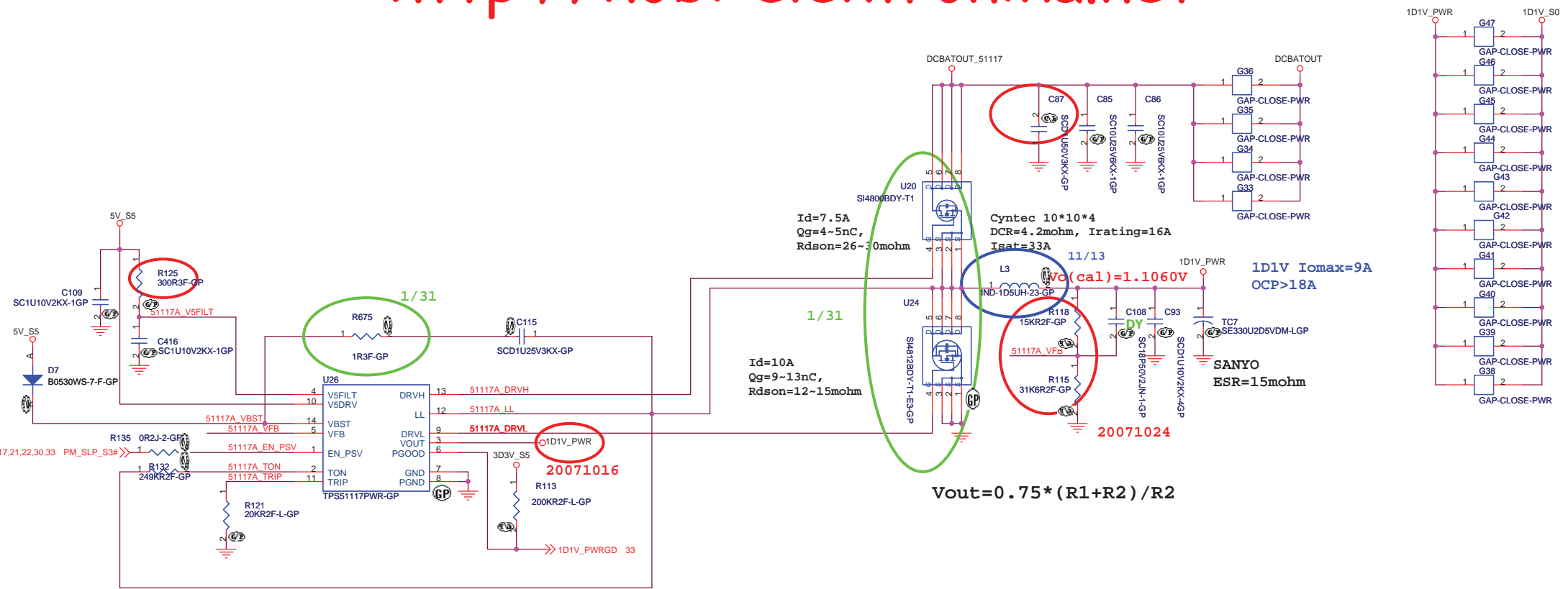


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

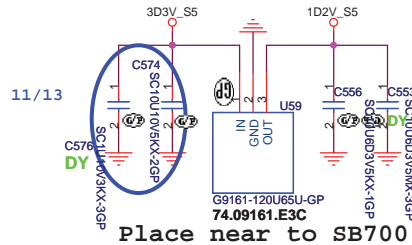
$V_{out} = 0.758V * (R1 + R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1 + R2) / R2$ --> Skip Mode

<Core Design>

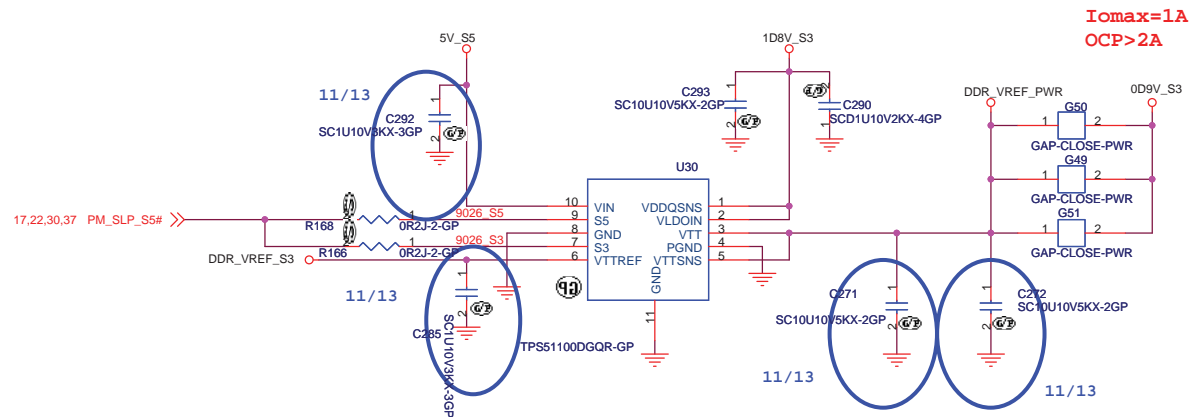
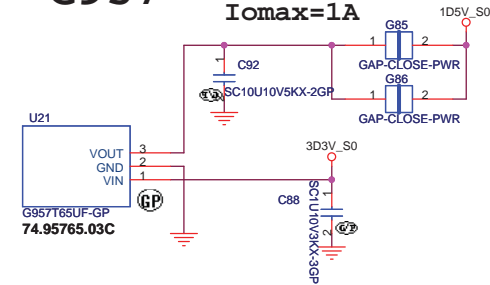
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
TPS51124 1D8V/1D2V			
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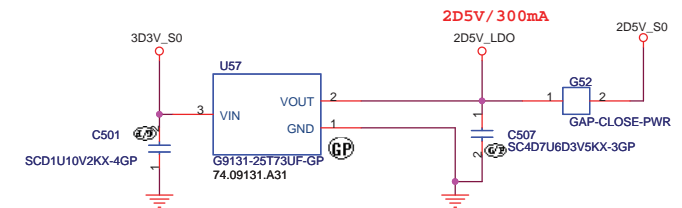
1D2V_S5
I_{omax}=400mA



G957 1D5V_S0
I_{omax}=1A



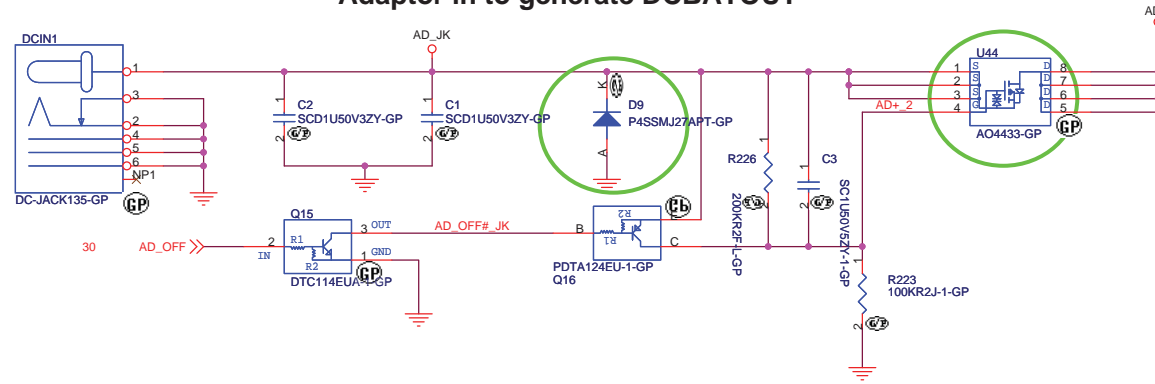
2D5V_S0
I_{omax}=0.3A



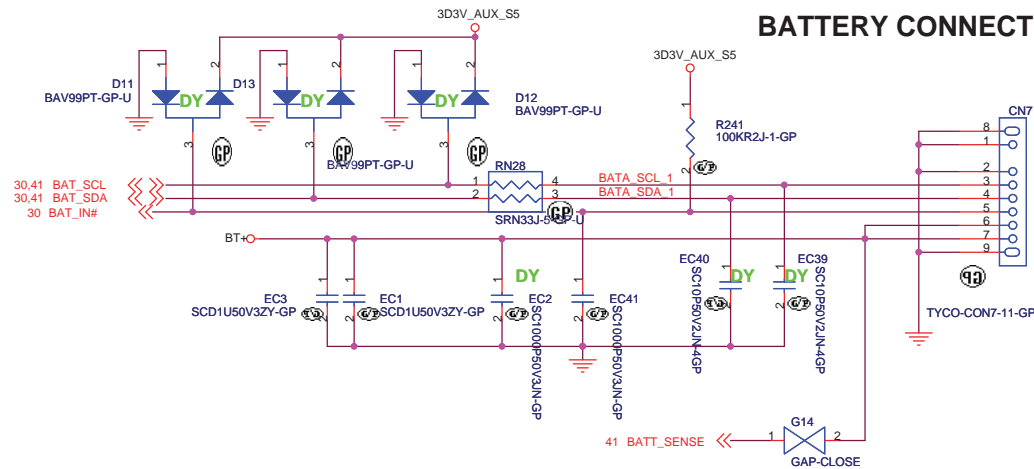
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緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 0D9V&2D5V&1D25V&1D5V	
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Adaptor in to generate DCBATOUT



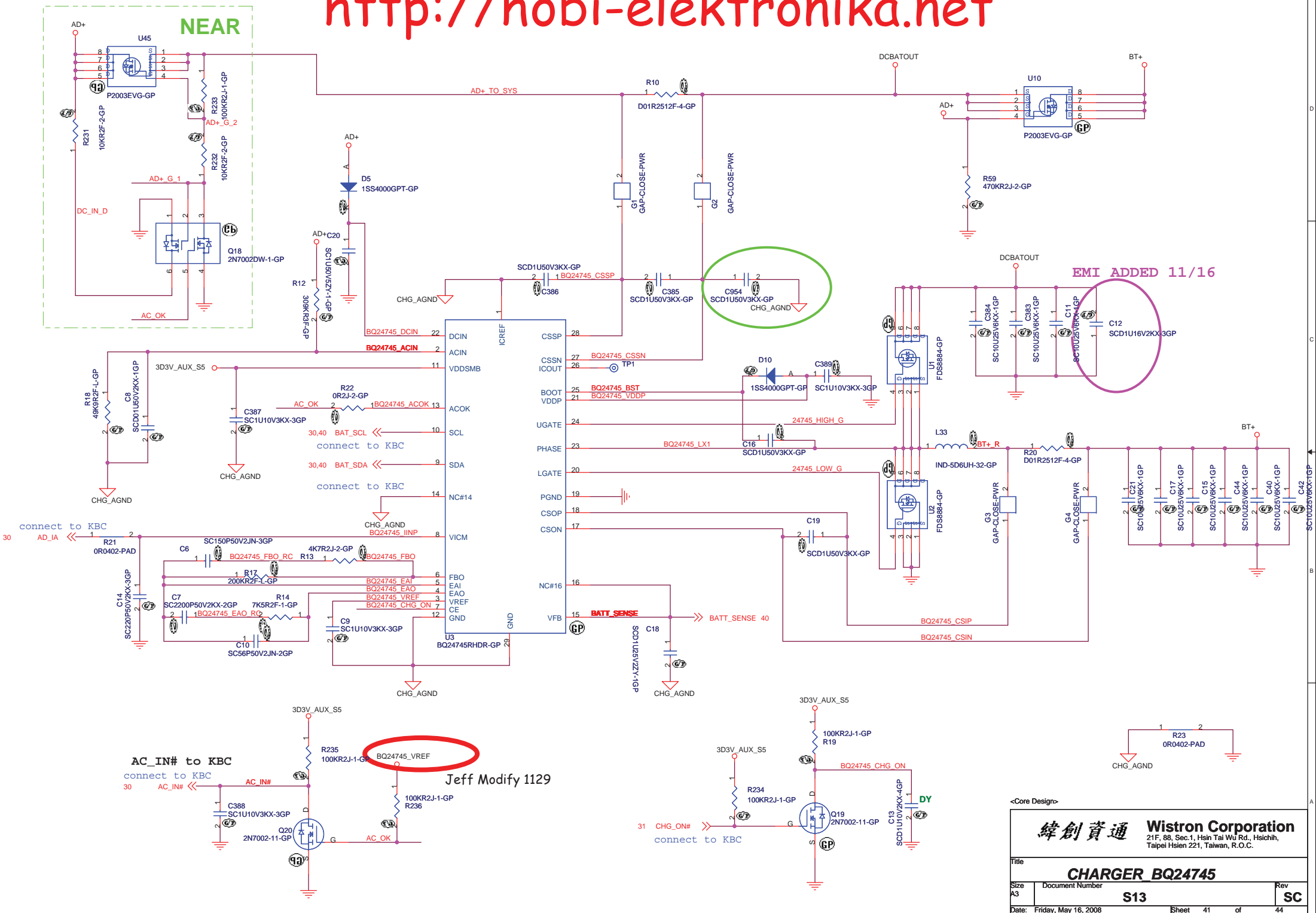
BATTERY CONNECTOR



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		AD IN/BTY SWITCH/GPURUN	
Size	Document Number	Rev	SC
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Date:	Friday, May 16, 2008	Sheet	40 of 44



AC_IN# to KBC

connect to KBC

Jeff Modify 1129

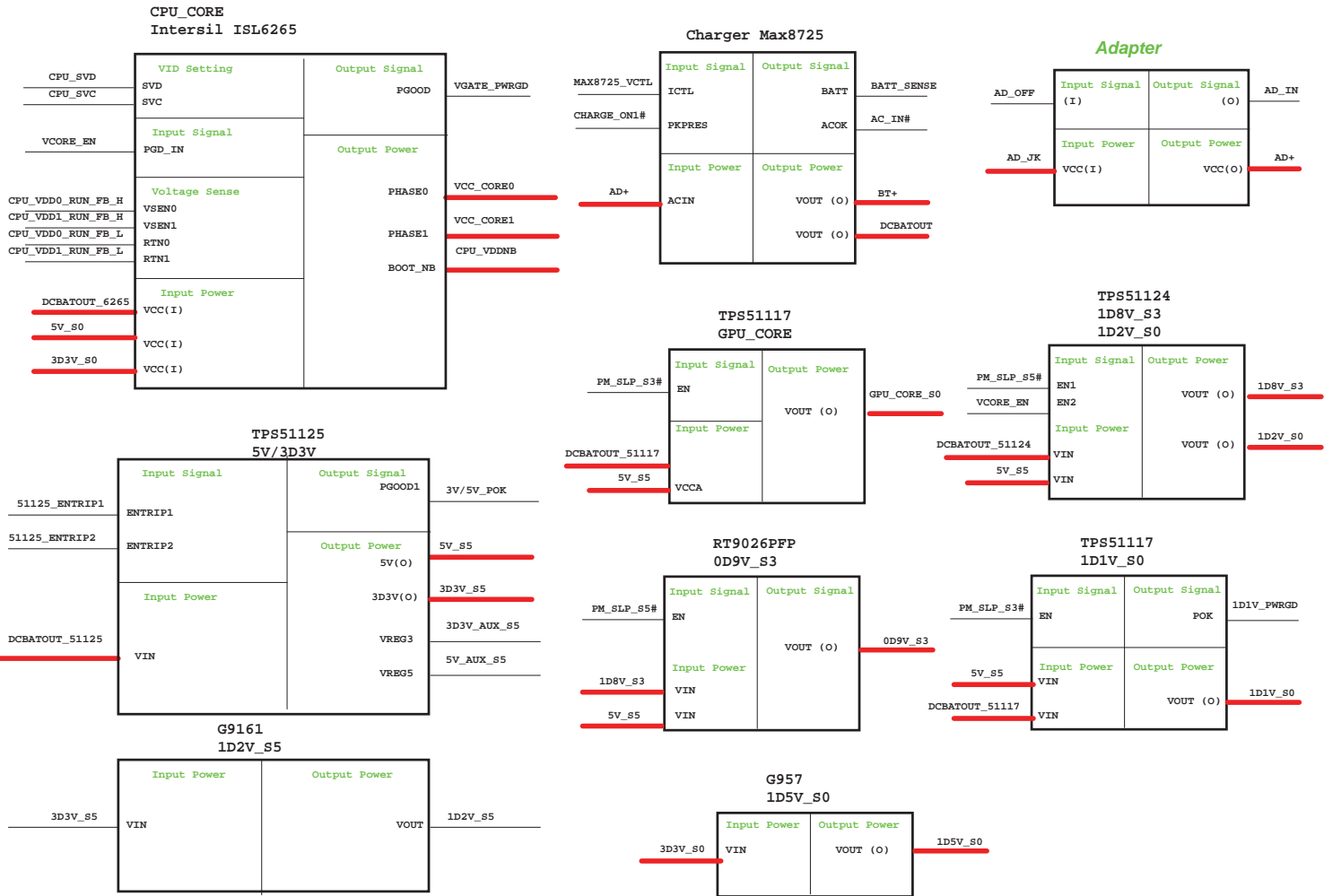
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

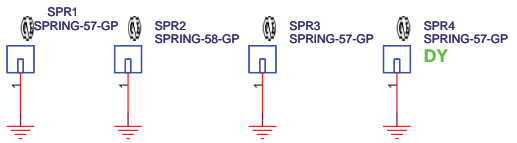
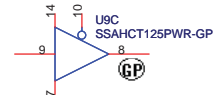
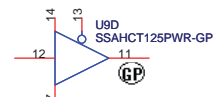
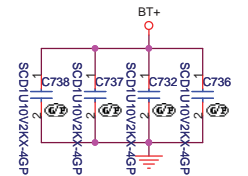
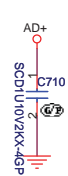
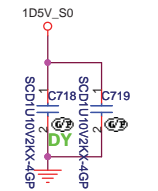
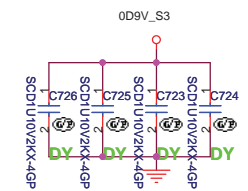
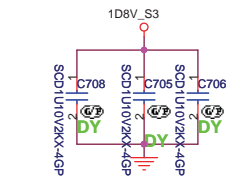
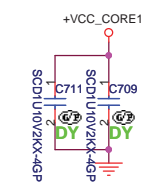
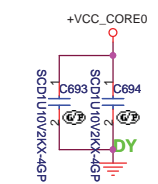
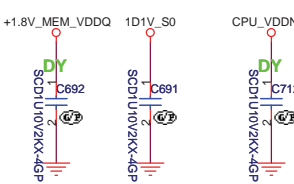
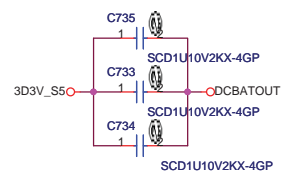
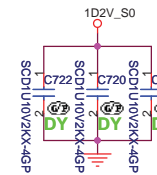
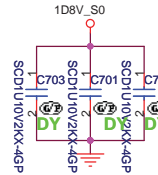
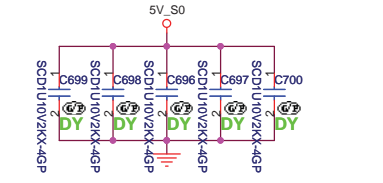
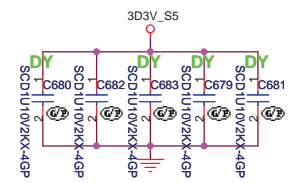
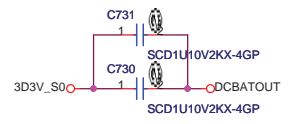
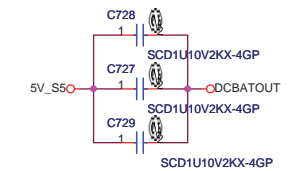
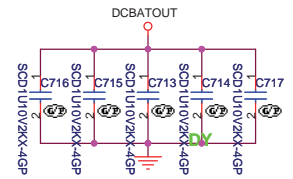
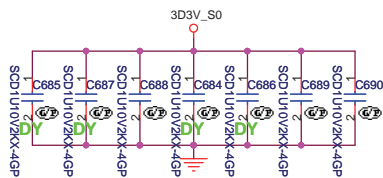
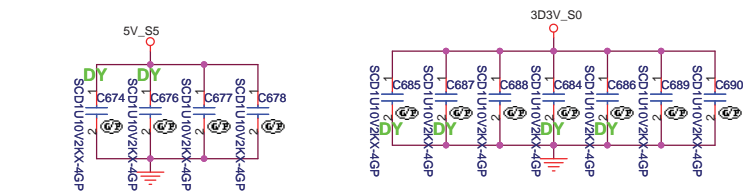
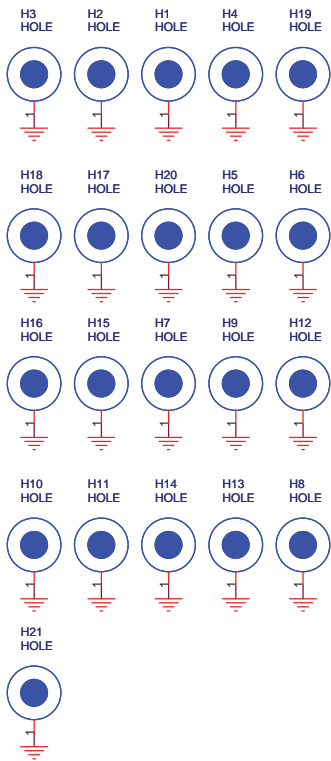
Title: **CHARGER BQ24745**

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<Core Design>



NOTICE

Change List

Common Part

- 1.RS780M_A12 U55 71.RS780.M12
- 2.SB700_A12 U62 71.SB700.M06
- 3.KBC U29 71.00773.00G
- 4.CLKGEN U32 71.09480.A03
- 5.SIDE PORT U28 72.18512.M0U
- 6.MOSFET U52,U51 84.07686.037
- 7.MOSFET U13,U12,U49,U50 84.04634.037
- 8.H18,H19 34.4H802.001
- 9.CARD1 20.I0043.001
- 10.U61 71.00380.003
- 11. U11 74.06265.A73
- 12. U42 71.00888.E0G
- 13. U31 72.25X16.A01

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
CHANGE LIST		
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