

Bitland Electronics Co.,LTD

Board name: Mother Board Schematic

Project name: BM5XXX

Version: REV:1.X

initial Date: 201X-0X-XX

New update:

1. System Block Diagram & Schematic page description;
2. Power Block Diagram & Discription;
3. Annotations & information;
4. Schematic modify Item and history;
5. Power on & off Sequence;
6. ACPI Mode Switch Timings;
7. Power On Sequence Map;
8. CLOCK Distribution;
9. Power Distribution;

Bitland Confidential

Hardware drawing by:


Hardware check by:

EMI Check by:

Power drawing by:

Power check by:

Manager Sign by:

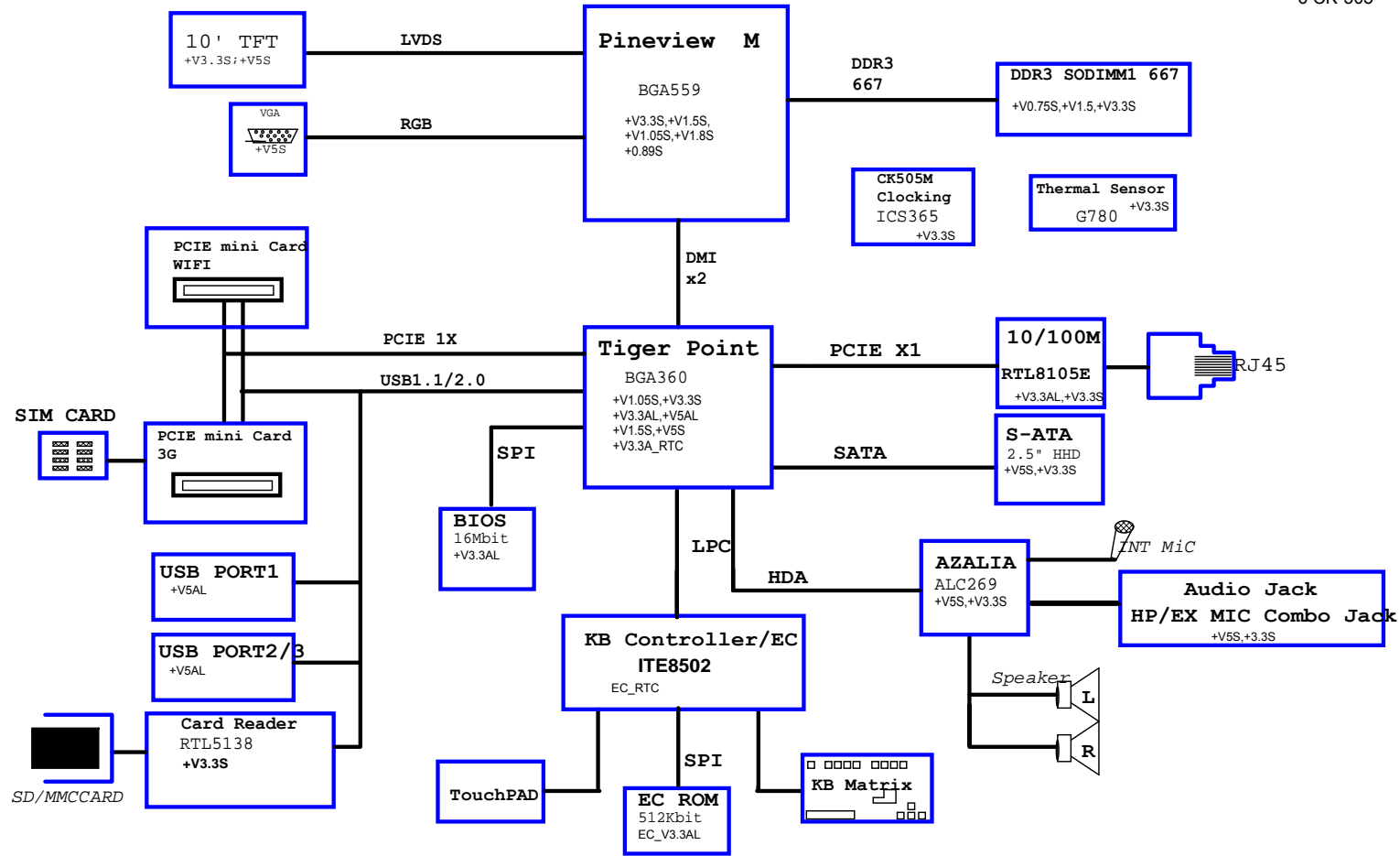
		Bitland Information Technology Co.,Ltd	
Page Name		Title	
Size A3	Project Name BM5080	Rev 1.2	
Date:		Sheet 1 of 42	
PROPERTY NOTE: this document contains information confidential and property to Bitland Technology Co.,Ltd. and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained with the expressed written consent of Bitland			


Bitland Electronics Co.,LTD

SYSTEM BLOCK Ver:C

CONTENT

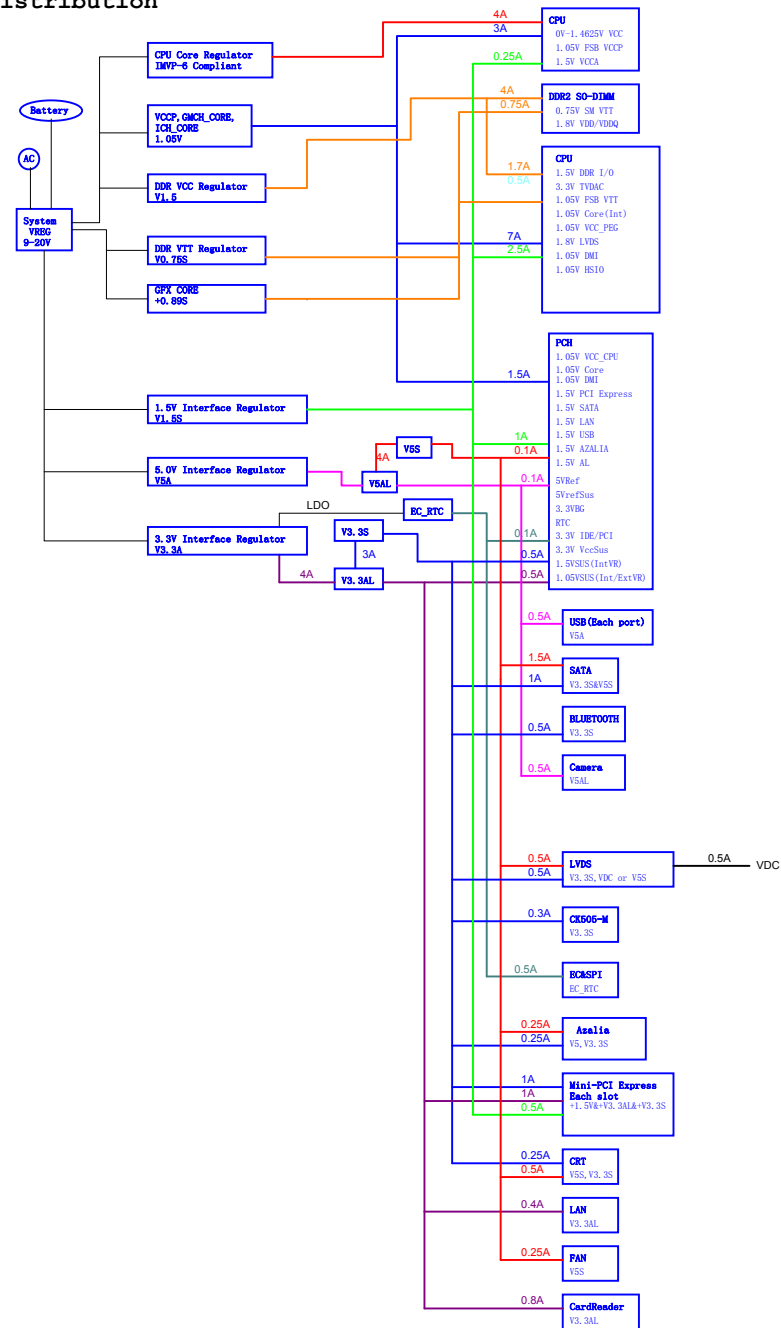
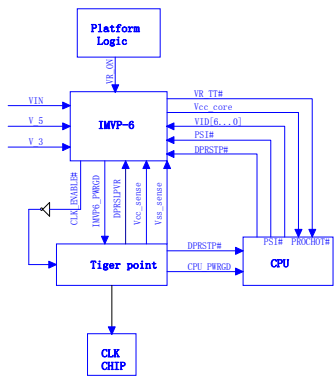
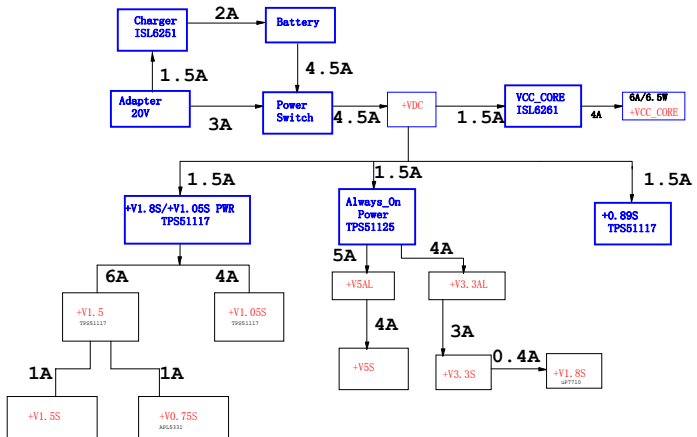
- 1 Title
- 2 System Block & Index
- 3 PWR Block & description
- 4 NOTE
- 5 Sch Modify and history
- 6 CK-505



 Bitland Information Technology Co.,Ltd		
Page Name		SYS BLOCK & SCH PAGE
Size B	Project Name	BM5080
		Rev 1.2
Date:	Sheet 2 of 42	
PROPERTY NOTE: this document contains information confidential and property to Bitland Technology Co.,Ltd. and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained with the expressed written consent of Bitland		

POWER Distribution

S18 POWER BLOCK Ver:A



Voltage Rails

+VDC	Primary DC system power supply (9V-20V)
+VBATTERY	Battery Power supply (9-20V)
+VCC_CORE	Core Voltage for CPU
+V1.05S	1.05V for Pineview & Tiger point core / FSB VTT
+V1.5	1.5V power rail for DDR3
+V0.75S	0.75V DDR3 Termination voltage
+V3.3AL	3.3V always on power rail
+V5AL	5V for ICH7-M's VCC5 Refsus
+V3.3S	3.3V main power rail
+V5S	5V main power rail
+V0.89S	0.89V for GFX

Board stack up description

PCB Layers	Trace Impedence:55ohm +/-15%
Top(Signal1)	
Power	
Ground	
Bottom(Signal4)	

USB Table

USB Port#	Function Description
0	
1	
2	
3	
4	
5	
6	
7	

I2C SMB Address

Device	Address	Hex	Master
Clock Generator	1101 001x	D2	ICH7-M
SO-DIMMO	1010 000x	A0	ICH7-M
CPU Thermal Sensor	1001 100x	98	KBC
Smart Battery	0001 011x	16	KBC
PCIE Slot	TBD	TBD	ICH7-M

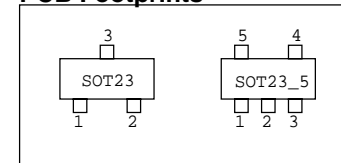
Power States

Signal	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*	+V*S	Clock
S0 (Full On)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (STM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (STD)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SoftOff)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Wake up Events


LID switch from EC
Power switch from EC

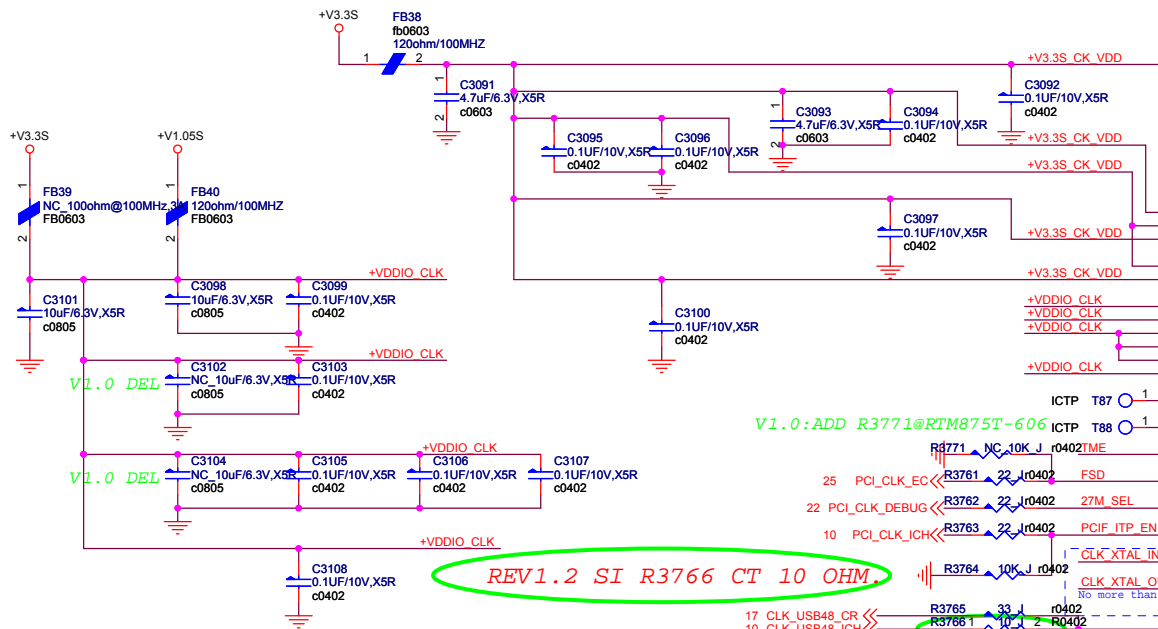
PCB Footprints



ns: Component marked "ns" is not stuff

Schematic modify Item and history:

		Bitland Information Technology Co.,Ltd	
Page Name		Sch Modify and history	
Size A3	Project Name	BM5080	Rev 1.2
Date:		Sheet 5 of 42	
PROPERTY NOTE: this document contains information confidential and property to Bitland Technology Co.,Ltd. and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained with the expressed written consent of Bitland			



U509 ICS9LPRS365 Issop64_0d5 8d0

VDD_PCI	48	IO_VOUT
VDD_48	9	
VDD_PLL3	16	
VDD_REF	61	
VDD_SRC	39	
VDD_CPU	55	
SRC5/PCI_STOP#	38	
SRC5/CPU_STOP#	37	
VDD_IO	12	
VDD_PLL3_IO	20	
VDD_SRC_IO_1	26	
VDD_SRC_IO_2	36	
VDD_SRC_IO_3	45	
VDD_CPU_IO	49	
PCI0/OE#_0/2_A	1	
SRC8/CPU2_ITP	47	
PCI1/OE#_1/4_ASRC8#CPU2#_ITP	46	
PCI2/TME	4	
SRC10	34	
PCI3/FSD	5	
SRC10#	35	
PCI4/SRC5_SEL	6	
SRC11#OE#_9	33	
PCIF#/ITP_EN	7	
SRC9	32	
SRC#	31	
XTAL_IN	60	
SRC7#OE#_6	44	
XTAL_OUT	59	
SRC7#OE#_6	43	
USB_48/FSA	41	
SRC6	40	
SRC#	40	
CLK_DM1_ICH#	10	
CLK_DM1_ICH#	10	
CLK_PCIE_EXPCARD	22	
CLK_PCIE_EXPCARD#	22	
FSB/TEST_MODE	27	
SRC4#	28	
SRC3#OE#_0/2_B	24	
SRC3#OE#_1/4_B	25	
SRC2/SATA#	21	
SRC2#/SATA#	22	
SRC1#SE1	17	
SRC1#/SE2	18	
DPL_REFSSCLKIN_DP	7	
DPL_REFSSCLKIN_DN	7	
CK_96M_DREF_DP	7	
CK_96M_DREF_DN	7	
VSS_PCI	8	
VSS_48	11	
VSS_IO	15	
VSS_PLL3	52	
VSS_CPU	23	
VSS_SRC_1	29	
VSS_SRC_2	58	
VSS_REF	42	
VSS_SRC3	56	
CK_PWRGD/PWRDWN#	56	

+V3.3S 7,8,9,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36
+V1.05S 8,9,10,11,12,34

Remove serial resistor swap pins for layout

V1.0:ADD R3771@RTM875T-606

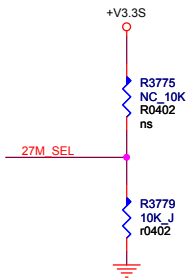
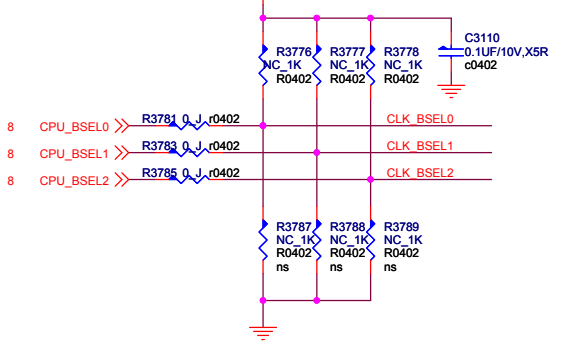
V1.1 ADD R3773 R3774 R3772

REV1.2 SI R3766 CT 10 OHM.

0610 add 1k resistor

REV1.2 DEL R3774 R3772

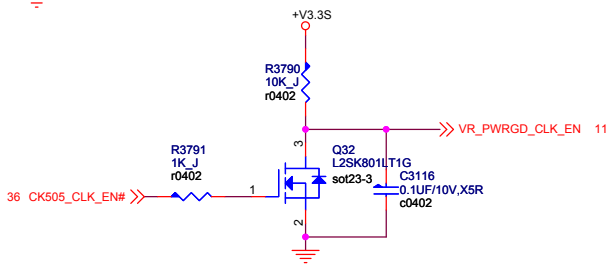
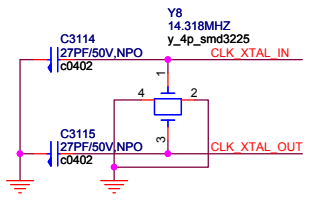
BUS FREQUENCE SELECT



TME R3780 10K J r0402
0: overlocking enable
1: overlocking disable

V1.0 ADD C11

CLK_ICH14	C3109	22PF/50V,NPO
CLK_USB48_ICH	C3111	22PF/50V,NPO
PCI_CLK_DEBUG	C11	c0402
PCI_CLK_EC	C3112	22PF/50V,NPO
PCI_CLK_ICH	C3113	22PF/50V,NPO



BTC Bitland Information Technology Co.,Ltd

Page Name CK505M

Size A3 Project Name BM5080 Rev 1.2

Date: Sheet 6 of 42

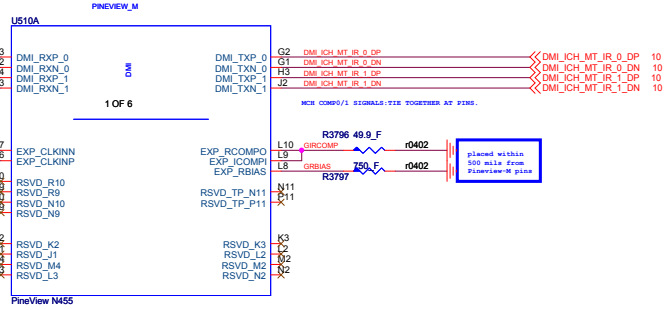
PROPERTY NOTE: this document contains information confidential and property to Bitland Technology Co.,Ltd. and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained with the expressed written consent of Bitland

6.8.9,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36

6.8.9,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36 +V3.3S +V3.3S

10 DM_LICH_IT_MR_0_DP << C3118 c0402 0.1UF/10V_X5R
10 DM_LICH_IT_MR_0_DN << C3117 c0402 0.1UF/10V_X5R
10 DM_LICH_IT_MR_1_DP << C3119 c0402 0.1UF/10V_X5R
10 DM_LICH_IT_MR_1_DN << C3120 c0402 0.1UF/10V_X5R

6 CLK_MCH_3GPLL# << N7
6 CLK_MCH_3GPLL << N8



13 MA_A_A0[14:0] << MA_A_A0 AH19
MA_A_A1 AJ18
MA_A_A2 AK18
MA_A_A3 AK16
MA_A_A4 AJ14
MA_A_A5 AH14
MA_A_A6 AK14
MA_A_A7 AJ12
MA_A_A8 AK13
MA_A_A9 AK12
MA_A_A10 AH12
MA_A_A11 AH11
MA_A_A12 AJ11
MA_A_A13 AJ10
MA_A_A14 AJ10

13 MA_A_WEB# << MA_A_WEB# AK22
13 MA_A_CAS# << MA_A_CAS# AJ22
13 MA_A_RAS# << MA_A_RAS# AK21

13 M_CS#0 << M_CS#0 AH22
13 M_CS#1 << M_CS#1 AJ21
13 M_CS#2 << M_CS#2 AJ20

13 M_CKE0 << M_CKE0 AH10
13 M_CKE1 << M_CKE1 AH9
13 M_CKE2 << M_CKE2 AJ8
13 M_CKE3 << M_CKE3 AK10

13 M_CLK_DDR0 << M_CLK_DDR0 AG15
13 M_CLK_DDR#0 << M_CLK_DDR#0 AF15
13 M_CLK_DDR#1 << M_CLK_DDR#1 AD13
13 M_CLK_DDR#4 << M_CLK_DDR#4 AC13

AC15 << MA_A_CK_3
AD16 << MA_A_CK_3
AF13 << MA_A_CK_4
AG14 << MA_A_CK_4

AD17 << RSVD_AD17
AC17 << RSVD_AC17
AB18 << RSVD_AB15
AB19 << RSVD_AB17

AB4 << VSS_AB4
AK8 << RSVD_AK8

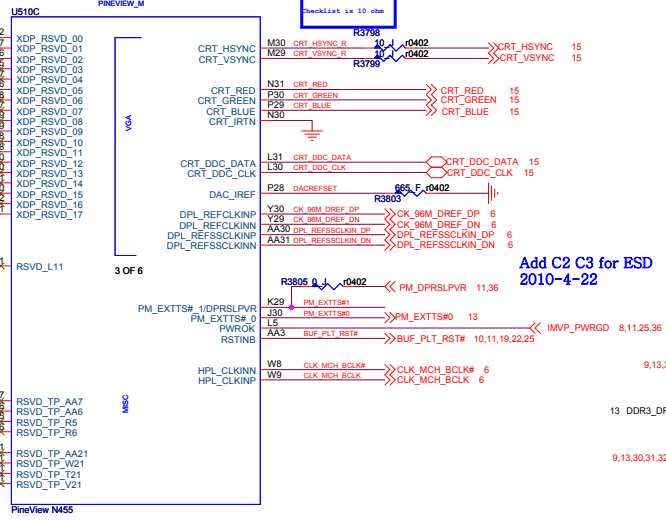
AL28 << MCH_VREF
AK28 << MCH_DDR_RPU
AJ26 << MCH_DDR_RPU

AK29 << RSVD_AK29

AD17 << RSVD_AD17
AC17 << RSVD_AC17
AB18 << RSVD_AB15
AB19 << RSVD_AB17

AA24 << MA_DATA56
AB25 << MA_DATA57
W24 << MA_DATA58
W22 << MA_DATA59
AA24 << MA_DATA56
AB25 << MA_DATA57
W24 << MA_DATA58
W22 << MA_DATA59

AA23 << MA_DATA62
W27 << MA_DATA63



ICTP T60 << 1 MCH_BSEL0 D12
ICTP T61 << 1 MCH_BSEL1 A7
ICTP T62 << 1 MCH_BSEL2 C6

R3800 << NC 0.5% R0402
R3802 << NC 0.5% R0402
R3804 << NC 0.5% R0402

XDP_RSVD_00 << XDP_RSVD_01
XDP_RSVD_02 << XDP_RSVD_03
XDP_RSVD_04 << XDP_RSVD_05
XDP_RSVD_06 << XDP_RSVD_07
XDP_RSVD_08 << XDP_RSVD_09
XDP_RSVD_10 << XDP_RSVD_11
XDP_RSVD_12 << XDP_RSVD_13
XDP_RSVD_14 << XDP_RSVD_15
XDP_RSVD_16 << XDP_RSVD_17

DPL_REFCLKINP << DPL_REFCLKINP
DPL_REFSSCLKINP << DPL_REFSSCLKINP

PM_EXTTS# << 1/DPRS_LVPR
PM_EXTTS# << 1/DPRS_LVPR
PWRCK << PWRCK
RSTINB << RSTINB

HPL_CLKINN << HPL_CLKINN
HPL_CLKINP << HPL_CLKINP

RSVD_TP_AA7 << RSVD_TP_AA6
RSVD_TP_R5 << RSVD_TP_R6

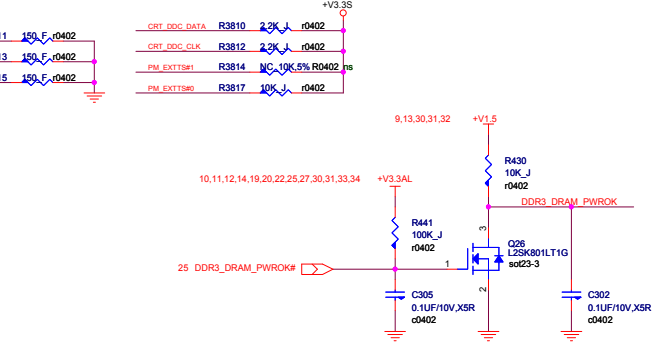
RSVD_TP_AA21 << RSVD_TP_W21
RSVD_TP_T21 << RSVD_TP_T21
RSVD_TP_V21 << RSVD_TP_V21

CRT_RED << R3811 150 F 0402
CRT_GREEN << R3813 150 F 0402
CRT_BLUE << R3815 150 F 0402

CRT_DDC_DATA << R3810 2.2K 0402
CRT_DDC_CLK << R3812 2.2K 0402
PM_EXTTS#1 << R3814 NC 10K 5% R0402 ns
PM_EXTTS#0 << R3817 10K 0402

10,11,12,14,19,20,22,25,27,30,31,33,34 +V3.3AL

25 DDR3_DRAM_PWROK# << R441 100K J R0402



DDR_A_MA_0 << MA_A_MA_0 AH19
DDR_A_MA_1 << MA_A_MA_1 AJ18
DDR_A_MA_2 << MA_A_MA_2 AK18
DDR_A_MA_3 << MA_A_MA_3 AK16
DDR_A_MA_4 << MA_A_MA_4 AJ14
DDR_A_MA_5 << MA_A_MA_5 AH14
DDR_A_MA_6 << MA_A_MA_6 AK14
DDR_A_MA_7 << MA_A_MA_7 AJ12
DDR_A_MA_8 << MA_A_MA_8 AK13
DDR_A_MA_9 << MA_A_MA_9 AK12
DDR_A_MA_10 << MA_A_MA_10 AH12
DDR_A_MA_11 << MA_A_MA_11 AH11
DDR_A_MA_12 << MA_A_MA_12 AJ11
DDR_A_MA_13 << MA_A_MA_13 AJ10
DDR_A_MA_14 << MA_A_MA_14 AJ10

DDR_A_WEB << MA_A_WEB# AK22
DDR_A_CASB << MA_A_CAS# AJ22
DDR_A_CASB << MA_A_RAS# AK21

DDR_A_CS_0 << M_CS#0 AH22
DDR_A_CS_1 << M_CS#1 AJ21
DDR_A_CS_2 << M_CS#2 AJ20
DDR_A_CS_3 << M_CS#3 AJ19

DDR_A_CKE_0 << M_CKE0 AH10
DDR_A_CKE_1 << M_CKE1 AH9
DDR_A_CKE_2 << M_CKE2 AJ8
DDR_A_CKE_3 << M_CKE3 AK10

DDR_A_CK_0 << M_CLK_DDR0 AG15
DDR_A_CK_1 << M_CLK_DDR#0 AF15
DDR_A_CK_2 << M_CLK_DDR#1 AD13
DDR_A_CK_3 << M_CLK_DDR#4 AC13

DDR_A_CS_3 << MA_A_CK_3
DDR_A_CS_4 << MA_A_CK_4

RSVD_AD17 << RSVD_AD17
RSVD_AC17 << RSVD_AC17
RSVD_AB15 << RSVD_AB15
RSVD_AB17 << RSVD_AB17

VSS_AB4 << VSS_AB4
RSVD_AK8 << RSVD_AK8

MCH_VREF << MCH_VREF
MCH_DDR_RPU << MCH_DDR_RPU

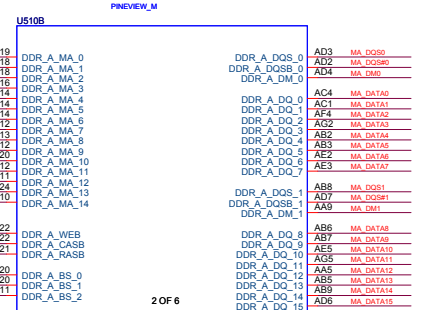
RSVD_AK29 << RSVD_AK29

RSVD_AD17 << RSVD_AD17
RSVD_AC17 << RSVD_AC17
RSVD_AB15 << RSVD_AB15
RSVD_AB17 << RSVD_AB17

MA_DATA56 << MA_DATA56
MA_DATA57 << MA_DATA57
MA_DATA58 << MA_DATA58
MA_DATA59 << MA_DATA59

MA_DATA62 << MA_DATA62
MA_DATA63 << MA_DATA63

MA_DQS[7:0] 13
MA_DQS# [7:0] 13
MA_DM[7:0] 13
MA_DATA[63:0] 13



DDR_A_CS_0 << M_CS#0 AH22
DDR_A_CS_1 << M_CS#1 AJ21
DDR_A_CS_2 << M_CS#2 AJ20
DDR_A_CS_3 << M_CS#3 AJ19

DDR_A_CKE_0 << M_CKE0 AH10
DDR_A_CKE_1 << M_CKE1 AH9
DDR_A_CKE_2 << M_CKE2 AJ8
DDR_A_CKE_3 << M_CKE3 AK10

DDR_A_CK_0 << M_CLK_DDR0 AG15
DDR_A_CK_1 << M_CLK_DDR#0 AF15
DDR_A_CK_2 << M_CLK_DDR#1 AD13
DDR_A_CK_3 << M_CLK_DDR#4 AC13

DDR_A_CS_3 << MA_A_CK_3
DDR_A_CS_4 << MA_A_CK_4

RSVD_AD17 << RSVD_AD17
RSVD_AC17 << RSVD_AC17
RSVD_AB15 << RSVD_AB15
RSVD_AB17 << RSVD_AB17

VSS_AB4 << VSS_AB4
RSVD_AK8 << RSVD_AK8

MCH_VREF << MCH_VREF
MCH_DDR_RPU << MCH_DDR_RPU

RSVD_AK29 << RSVD_AK29

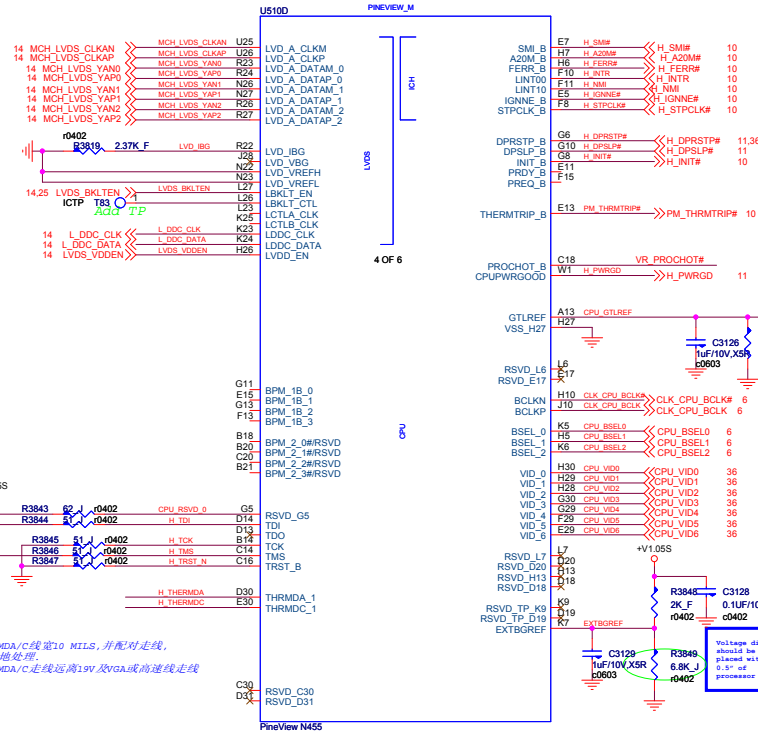
RSVD_AD17 << RSVD_AD17
RSVD_AC17 << RSVD_AC17
RSVD_AB15 << RSVD_AB15
RSVD_AB17 << RSVD_AB17

MA_DATA56 << MA_DATA56
MA_DATA57 << MA_DATA57
MA_DATA58 << MA_DATA58
MA_DATA59 << MA_DATA59

MA_DATA62 << MA_DATA62
MA_DATA63 << MA_DATA63

○ +V3.3S 6,7,9,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36
 ○ +V1.05S 6,9,10,11,12,34
 ○ EC_RTC 11,25,33

6,7,9,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36 +V3.3S +V3.3S

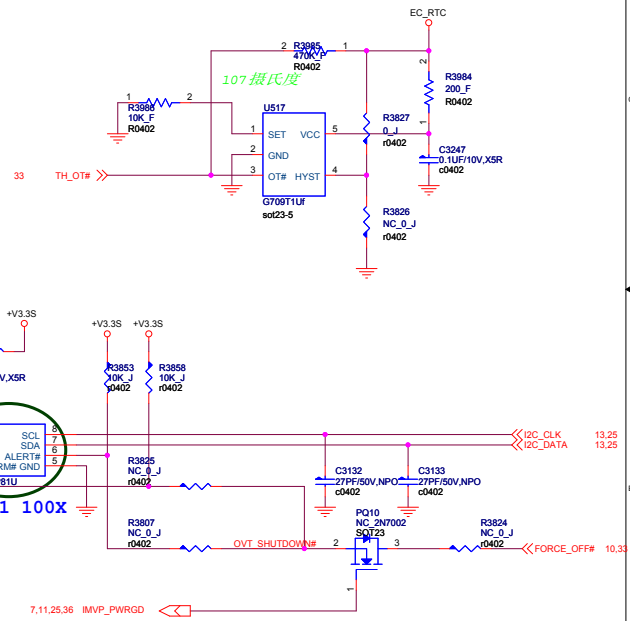


H_DPDRSTP#
 This Daisy-Chain CMOS topology should be routed from Signal Point to Input WPT-0, then to Processor processor (in this order exact).

Voltage divider should be placed within 0.5" of processor pin.

Voltage divider should be placed within 0.5" of processor pin.

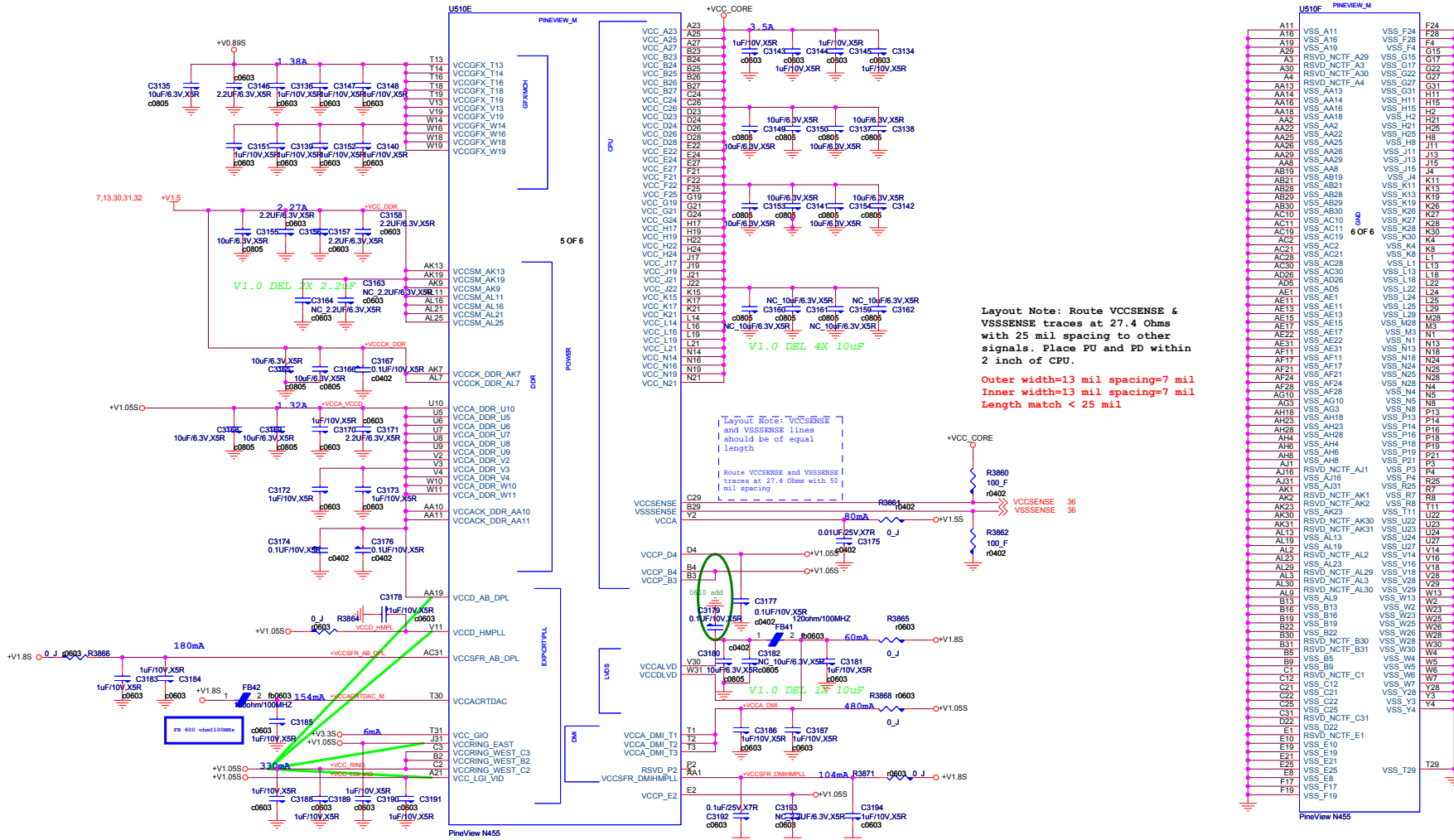
NOTE
 1. H_THERMDA/C线宽10 MILS, 并配1对走线, 然后再包地处理.
 2. H_THERMDA/C走线远离1.9V及VGA或高速线走线



Bilid Information Technology Co.,Ltd		
Page Name	Pineview-M HOST LVDS	
Size	Project Name	Rev
C	BM5090	1.2
Date:	Sheet 8 of 42	
PROPERTY NOTE: this document contains information confidential and property to Bilid Technology Co.,Ltd. and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained with the expressed written consent of Bilid.		

- +V3.3S 6,7,8,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36
- +VCC_CORE 36
- +V1.05S 6,8,10,11,12,34
- +V1.5S 12,22,30
- +V0.89S 32,34
- +V1.8S 34

6,7,8,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36 +V3.3S +V3.3S



Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 2 inch of CPU.

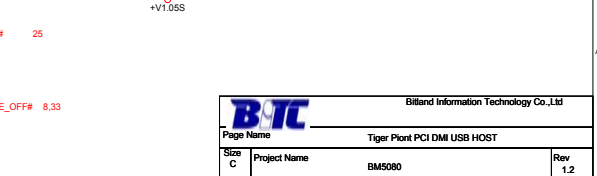
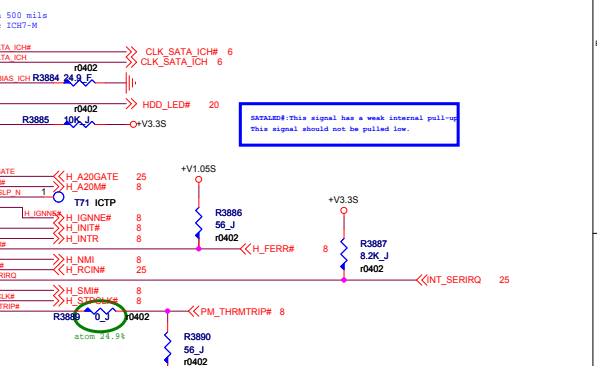
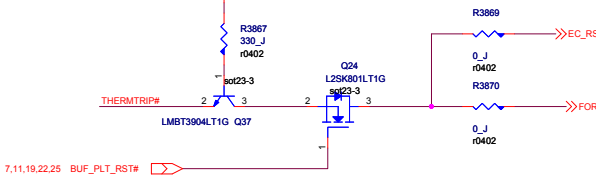
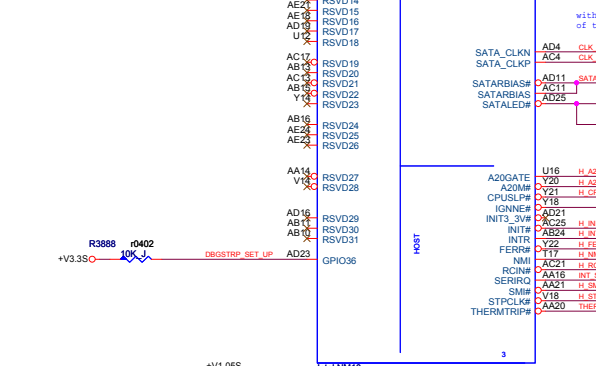
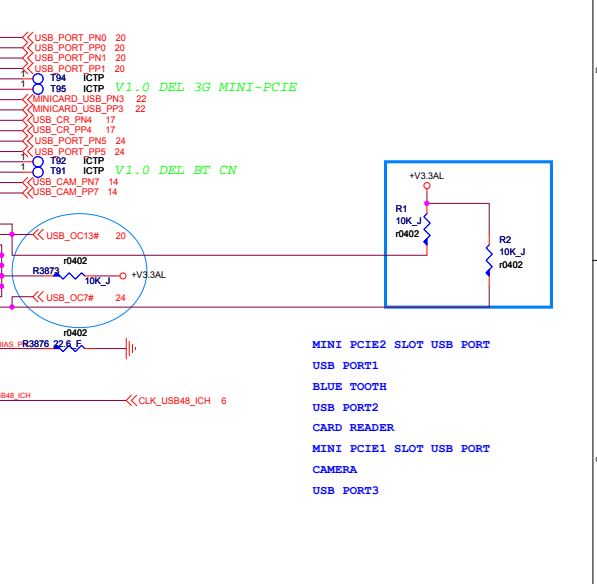
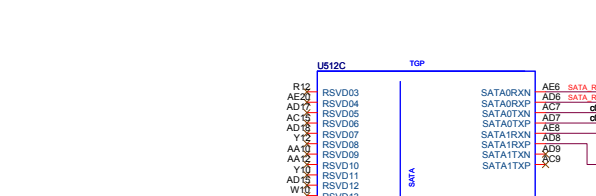
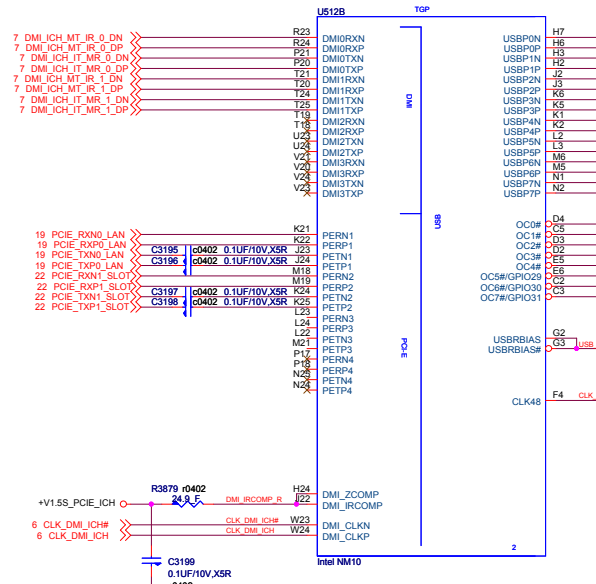
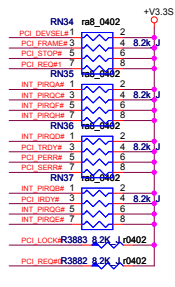
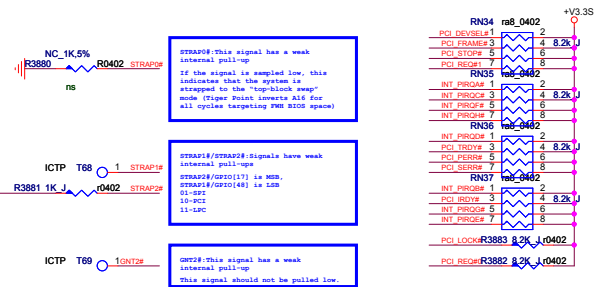
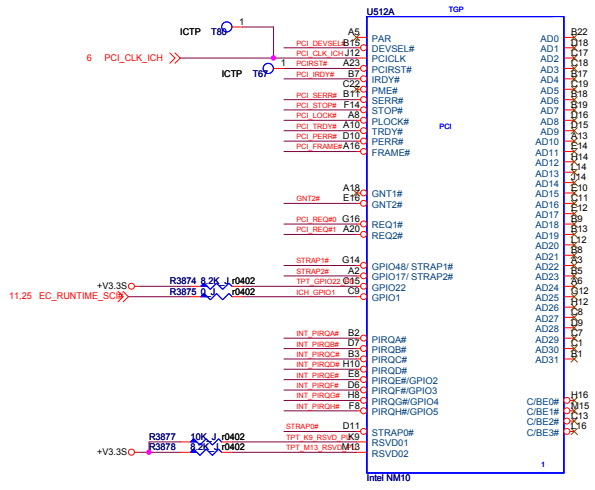
Outer width=13 mil spacing=7 mil
Inner width=13 mil spacing=7 mil
Length match < 25 mil

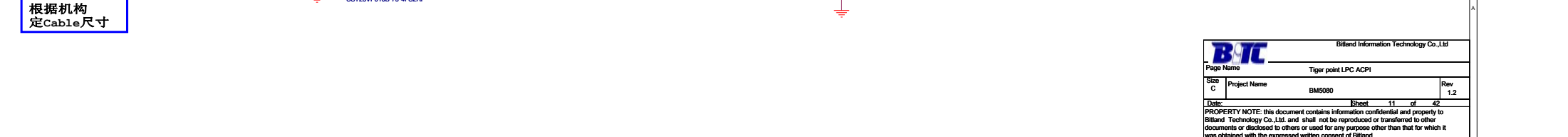
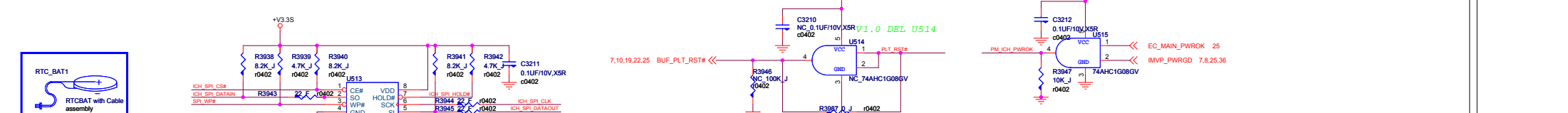
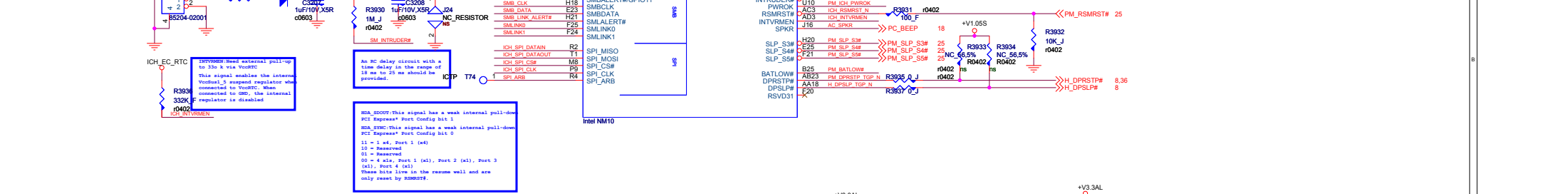
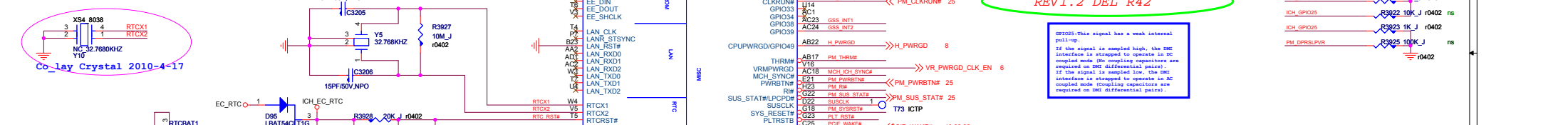
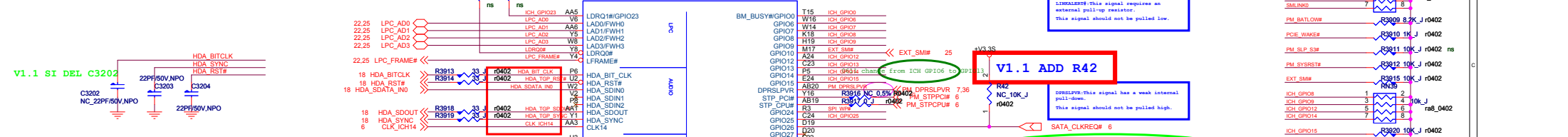
Layout Note: VCCSENSE and VSSSENSE traces should be of equal length

Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing

- +V3.3AL 7,11,12,14,19,20,22,25,27,30,31,33,34
- +V3.3S 6,7,8,9,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36
- +V1.5S_PCIE_ICH 12
- +V1.05S 6,8,9,11,12,34

- 6,7,8,9,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36
- +V3.3S
- +V3.3S





NOTE: The signal has a weak internal pull-down resistor. If the signal is sampled high, this indicates that the system is stopped in the "No reboot" mode (Tiger Point chipset will disable the TCC timer system reboot feature. The status of this strap is readable via the NO_REBOOT bit).

NOTE: This signal should be connected to power monitoring logic and should go high no sooner than 10 ns after both VDDC3_3 and VDDC3_3 have reached their nominal voltages.

NOTE: The SMBUS# signal of the Tiger Point chipset must transition from 20% signal level to 80% signal level and vice-versa in 50 ps or less.

LIBRARYDEF: This signal requires an external pull-up resistor. This signal should not be pulled low.

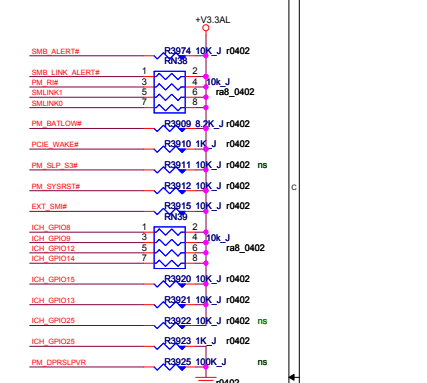
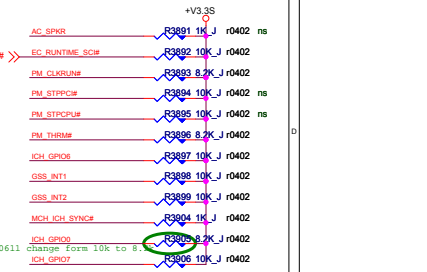
NOTE: This signal has a weak internal pull-down. This signal should not be pulled high.

NOTE: This signal has a weak internal pull-up. If the signal is sampled high, the ONT interface is stopped to operate in AC coupled mode (No coupling capacitors are specified on ONT differential pairs). If the signal is sampled low, the ONT interface is stopped to operate in DC coupled mode (Coupling capacitors are specified on ONT differential pairs).

NOTE: This signal has a weak internal pull-down. This signal should not be pulled low.

NOTE: This signal has a weak internal pull-down. This signal should not be pulled low.

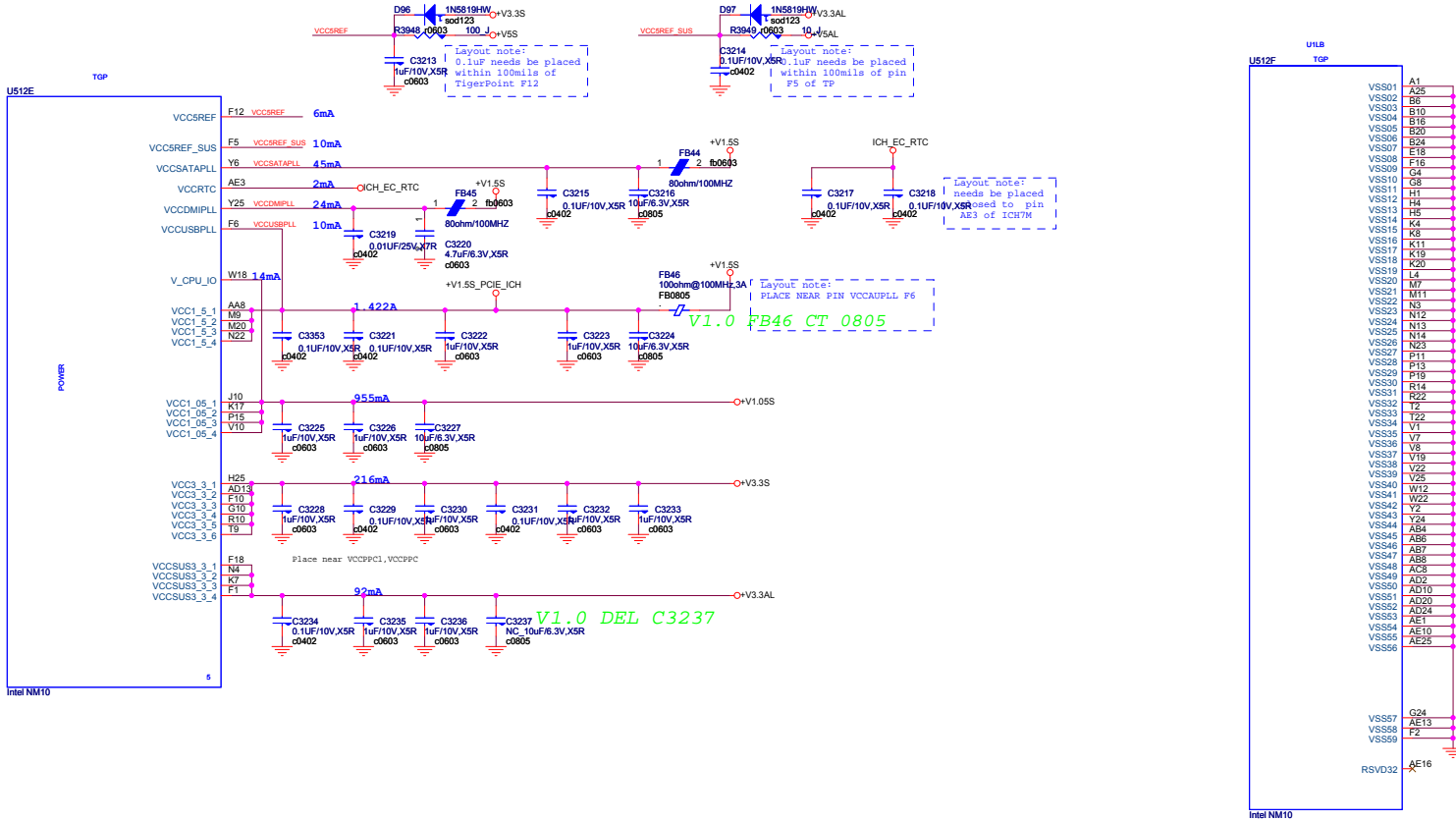
NOTE: This signal has a weak internal pull-down. This signal should not be pulled low.

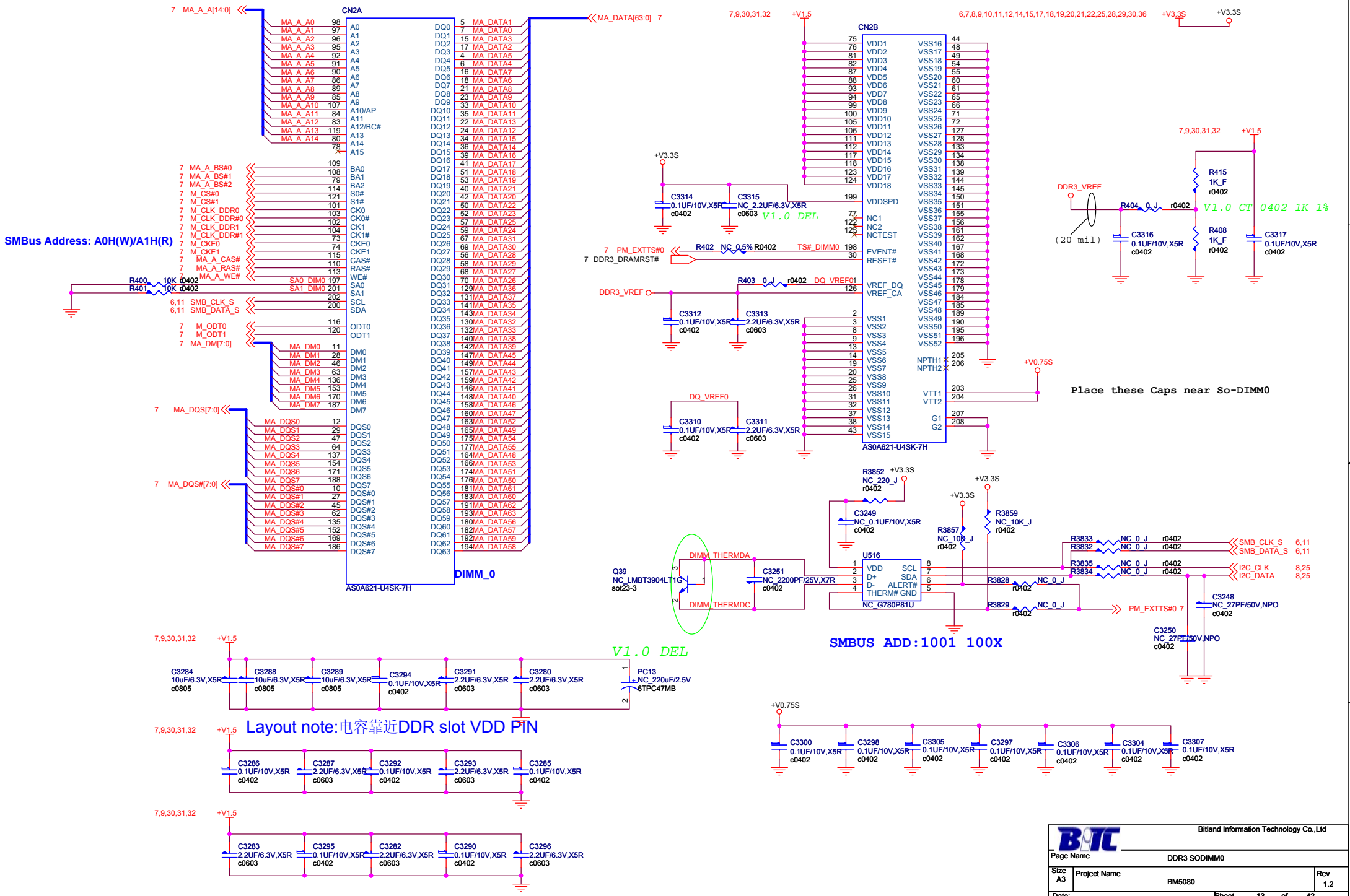


根据机构
定Cable尺寸

- ICH_EC_RTC 11
- +V3.3AL 7,10,11,14,19,20,22,25,27,30,31,33,34
- +V5AL 14,20,24,30,31,32,33,34
- +V3.3S 6,7,8,9,10,11,13,14,15,17,18,19,20,21,22,25,28,29,30,36
- +V5S 14,15,16,18,20,21,30,32,36
- +V1.05S 6,8,9,10,11,34
- +V1.5S 9,22,30
- +V1.5S_PCIE_ICH 10

6,7,8,9,10,11,13,14,15,17,18,19,20,21,22,25,28,29,30,36 +V3.3S +V3.3S





Layout note: 电容靠近DDR slot VDD PIN

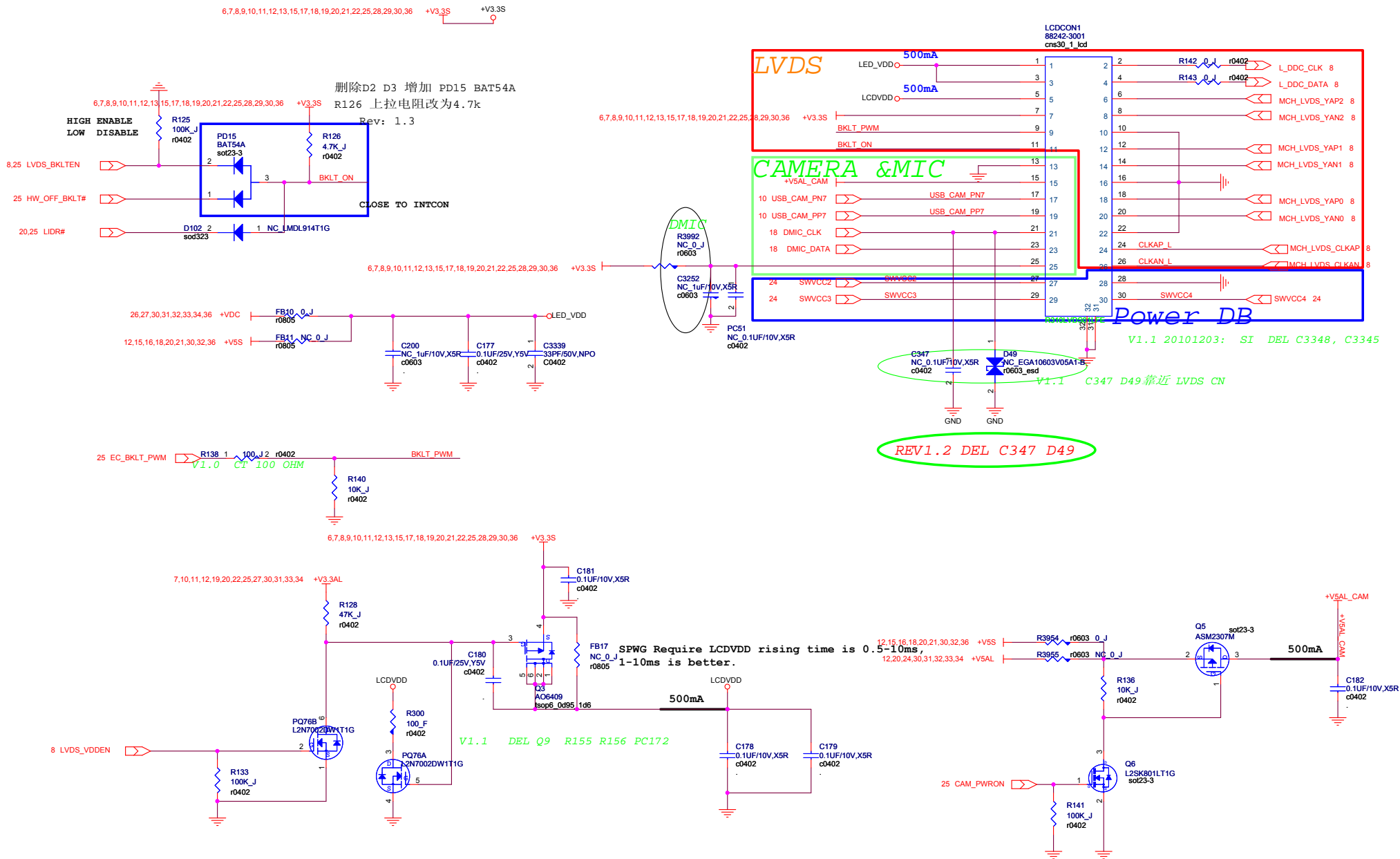
BTC Bitland Information Technology Co., Ltd

Page Name: DDR3 SODIMMO

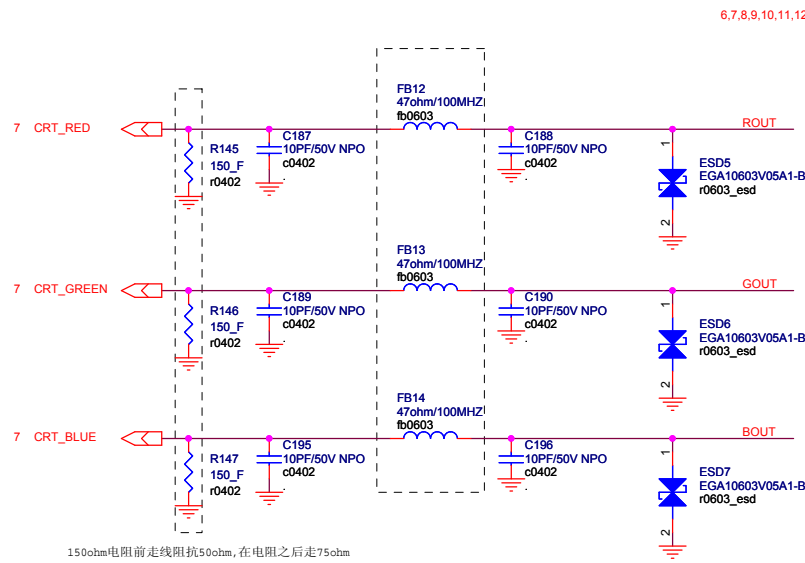
Size A3 Project Name: BM5080 Rev: 1.2

Date: Sheet 13 of 42

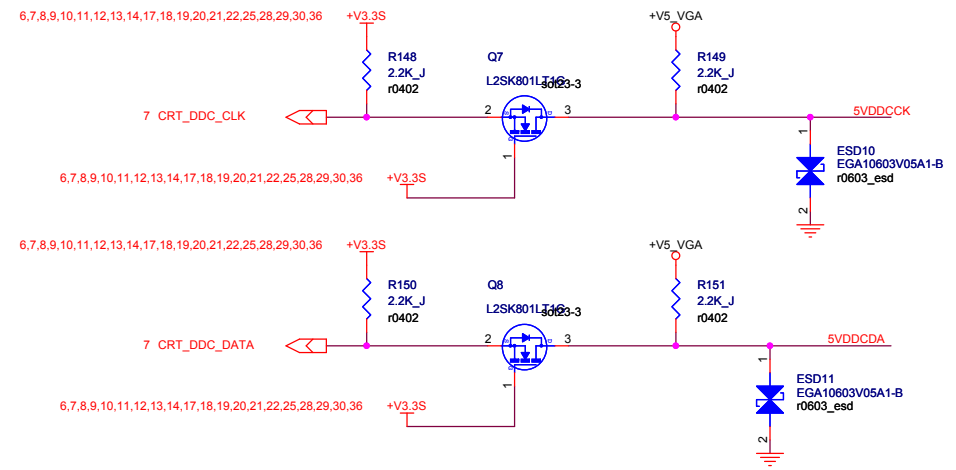
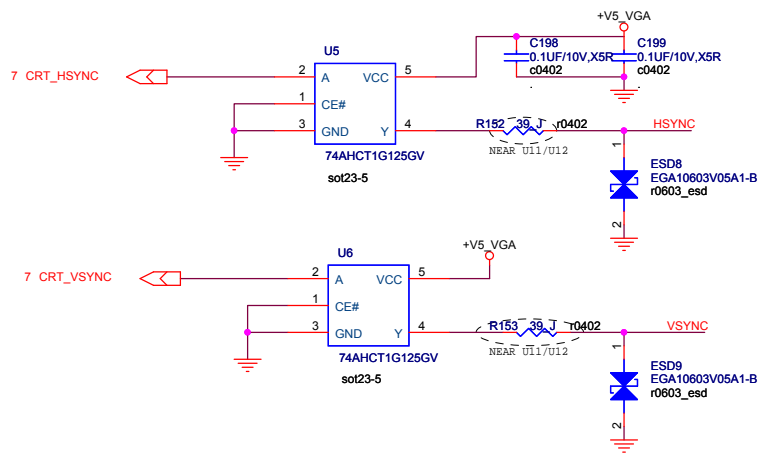
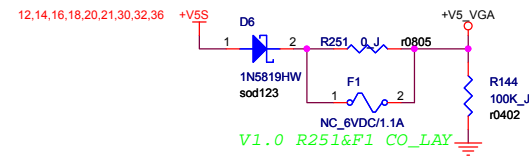
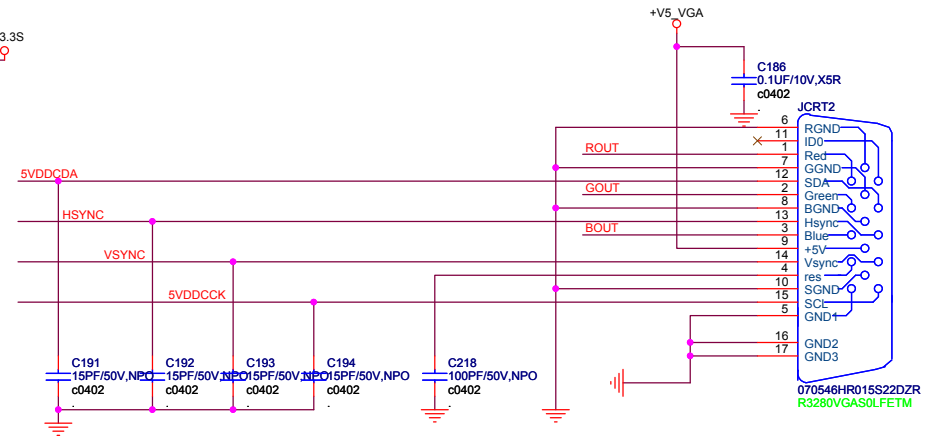
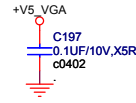
PROPERTY NOTE: this document contains information confidential and property to Bitland Technology Co., Ltd. and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained with the expressed written consent of Bitland



		Bitland Information Technology Co.,Ltd. 4-F, #7 Building, XIII Tongfuyi Industrial Town Nanshan District, Shenzhen	
		BITC_PN: BM5080 ID: LVDS Date:	Rev: 1.2 Size: Custom Sheet: 14 of 42

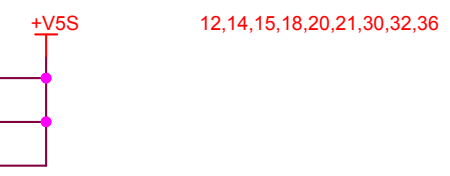
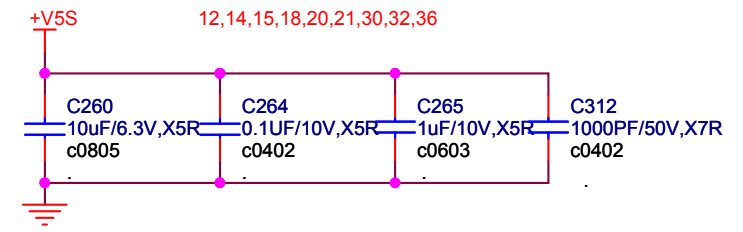
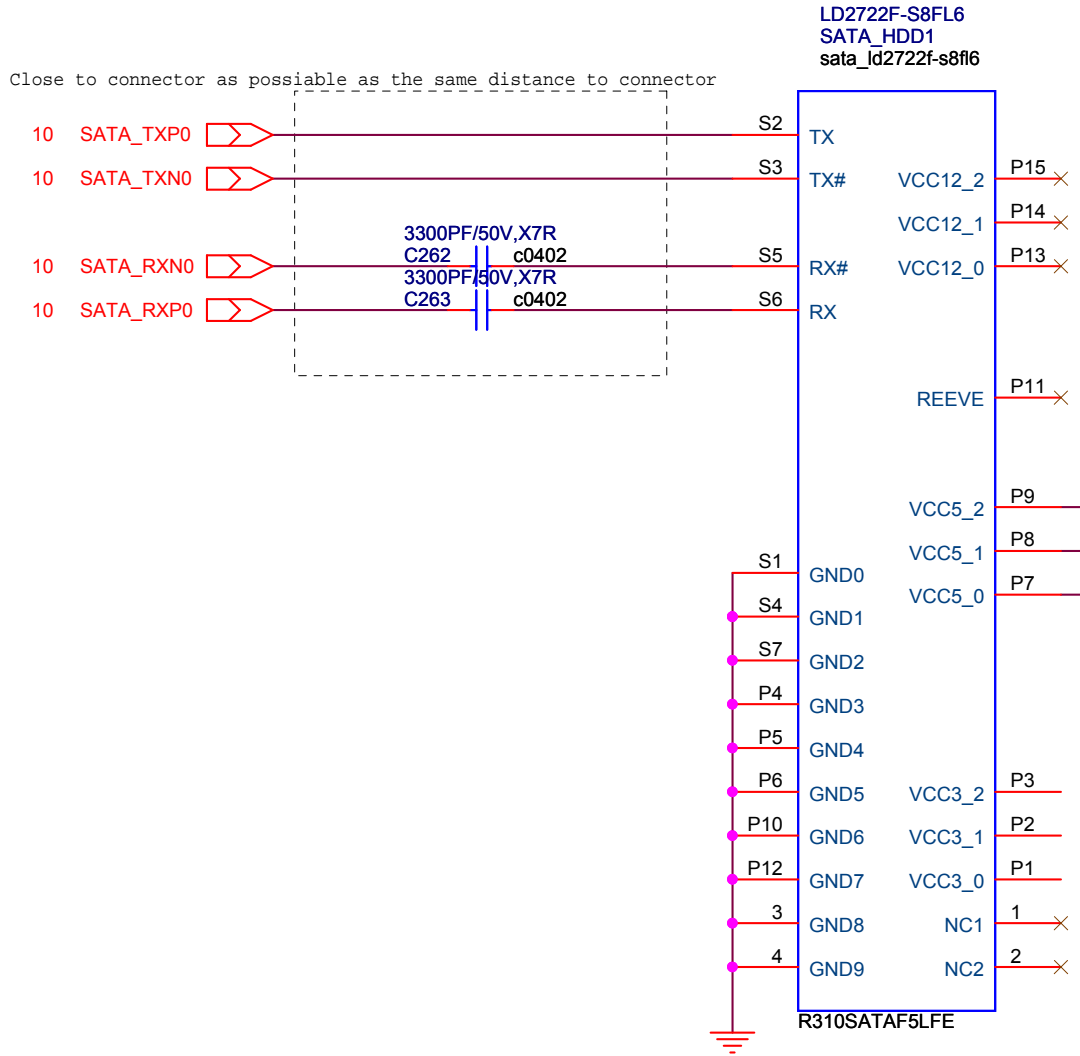



V1.1 20101203: SI
 C188 C190, C196, C189, C195. C187 10pF



BITC Bitland Information Technology Co.,Ltd.
 4-6F,#7Building,XIII Tongfuyu Industrial Town Nanshan District,Shenzhen

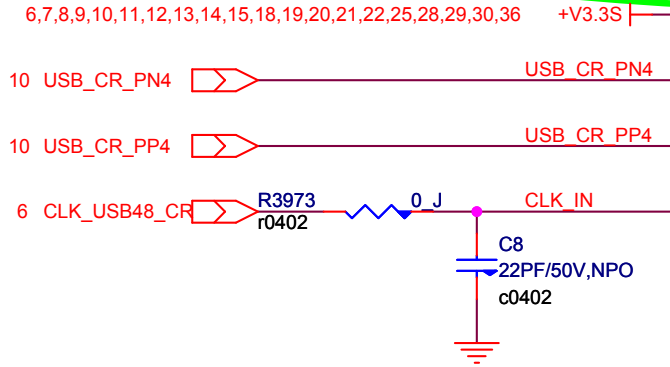
TITLE	Netbook	BITC_PN	BM5080	Rev	1.2
PAGE DETAIL	<Doc>	ID	CRT	Size	A3
		Date		Sheet	15 of 42



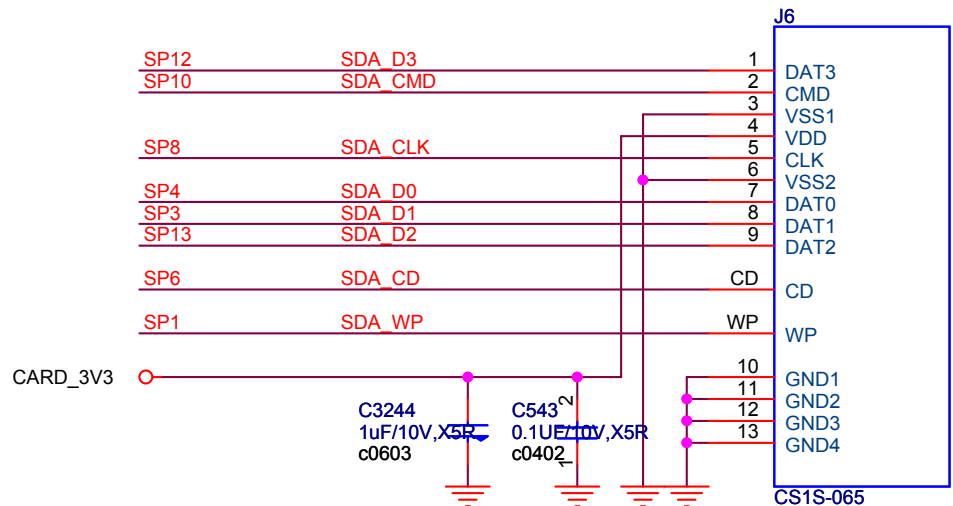
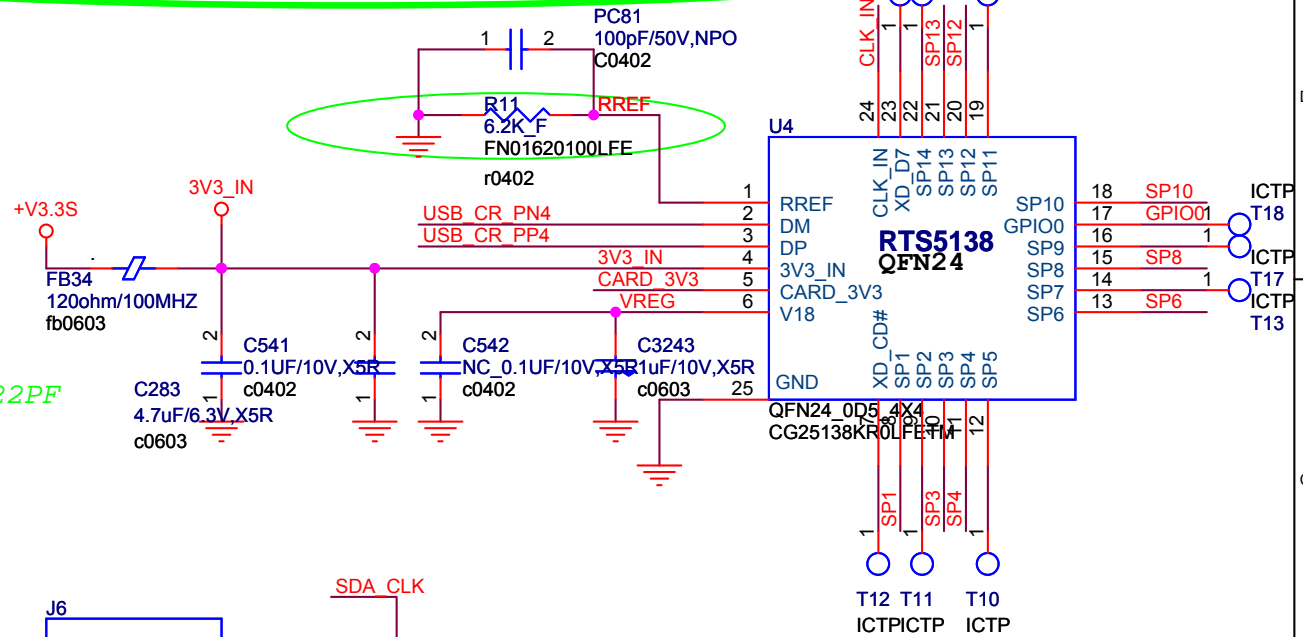
 Bitland Information Technology Co.,Ltd. 4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen		Rev	1.2
		ID	SATA
BITC_PN	BM5080	Size	A
Date		Sheet	16 of 42

TITLE	Netbook
PAGE DETAIL	<Doc>

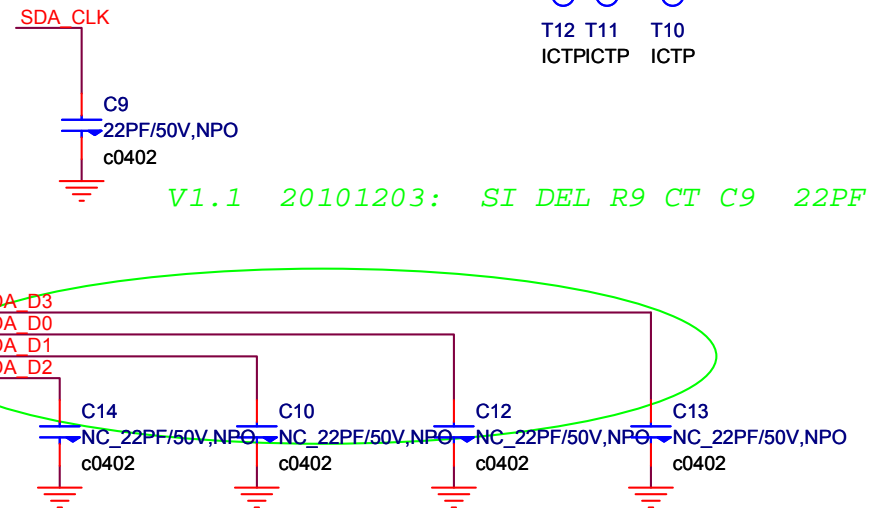
REV1.2 R11 's Footprint change 0603 to 0402



V1.1 20101203: SI DEL R8 CT C8 22PF



Internal SD/MMC Card CN

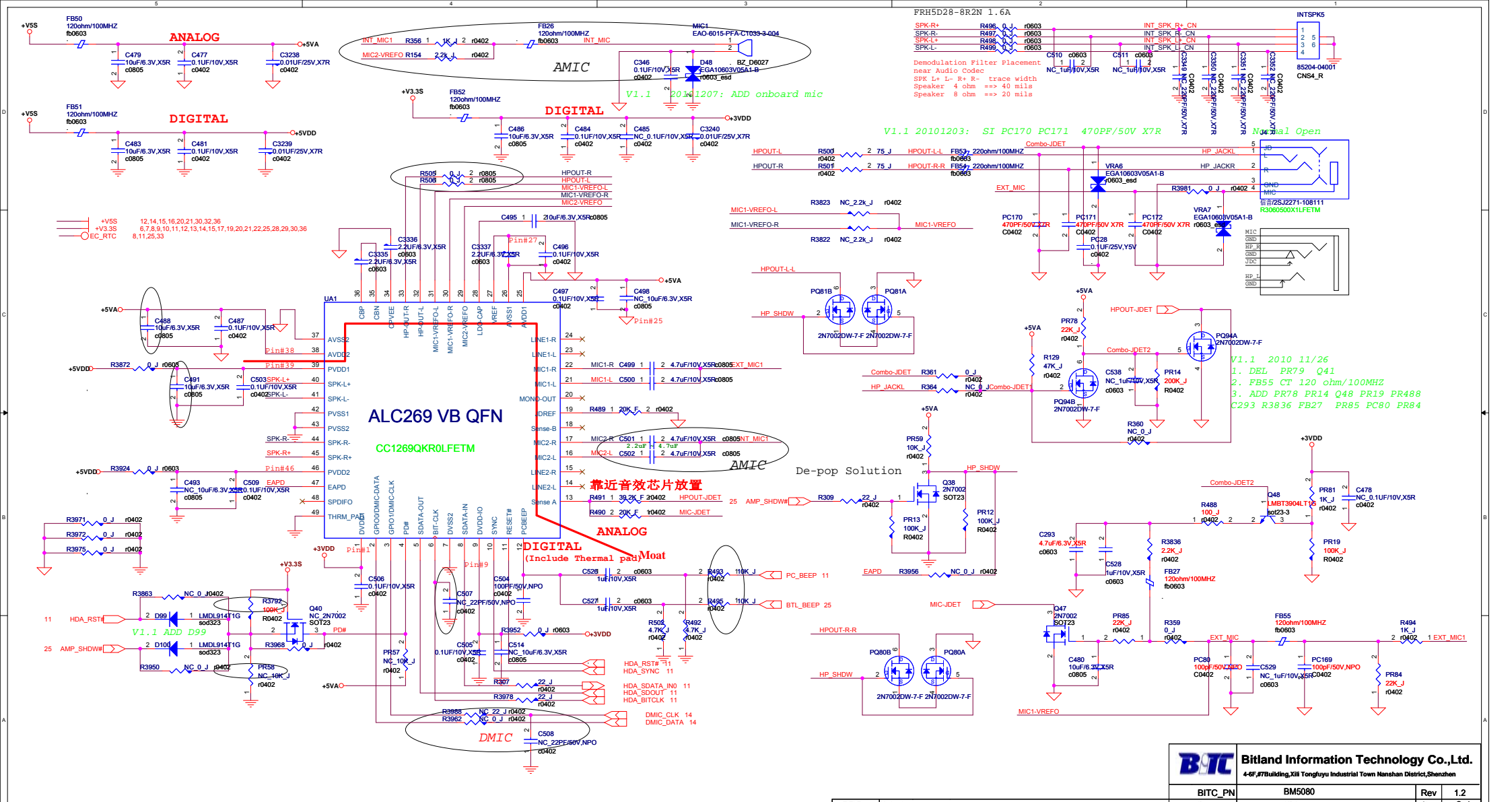


V1.1 20101203: SI DEL R9 CT C9 22PF

BITC Bitland Information Technology Co.,Ltd.
4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen

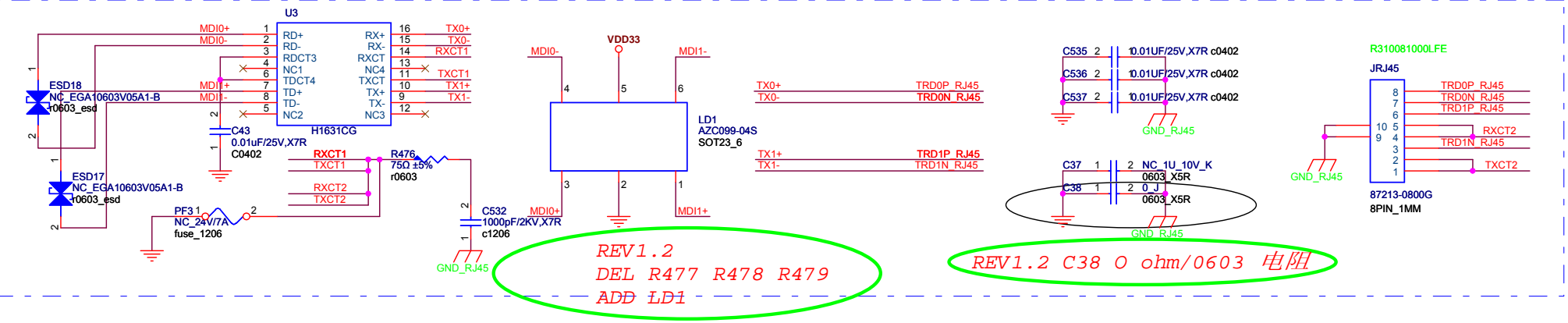
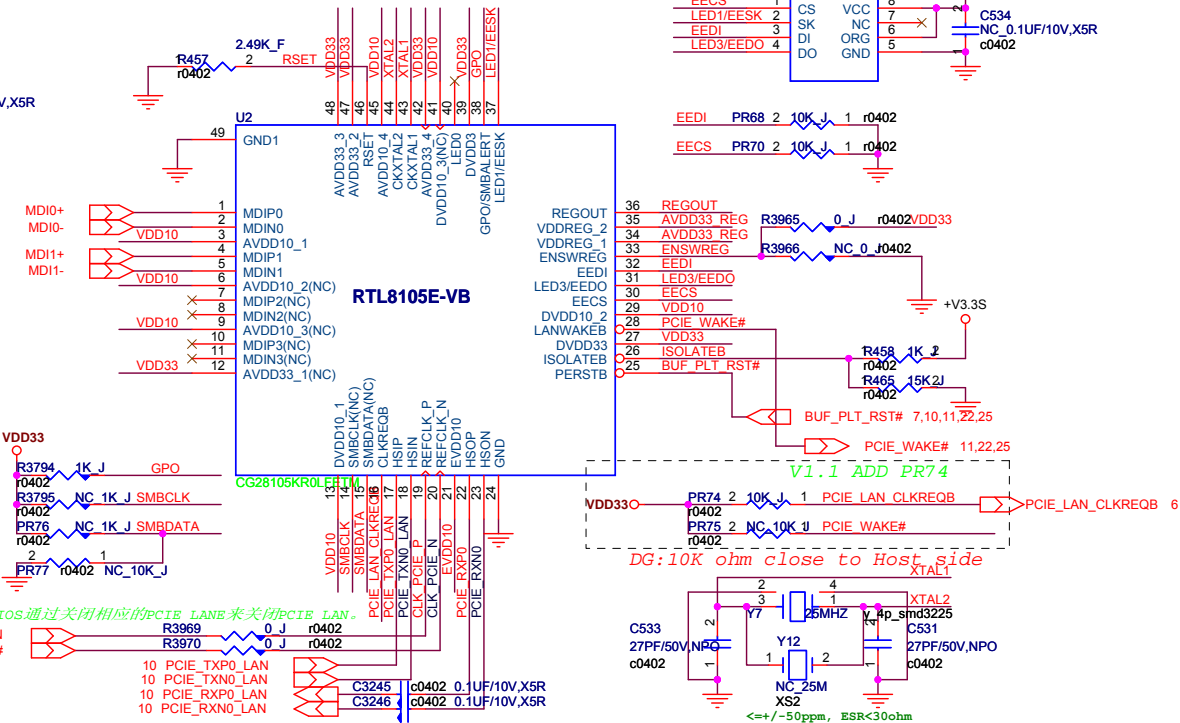
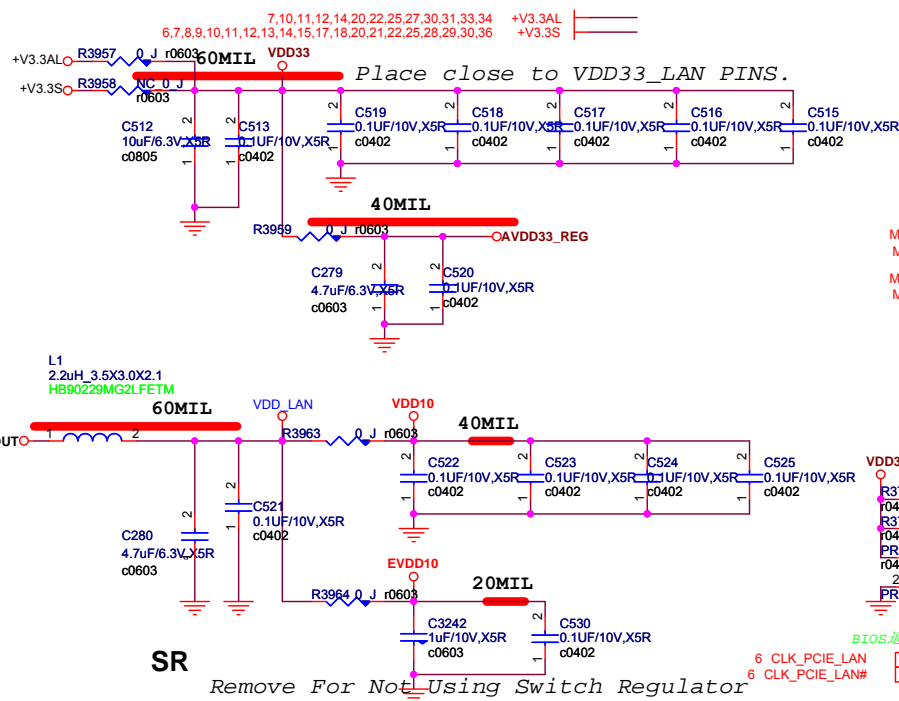
BITC_PN	BM5080	Rev	1.2
ID	CARDREADER	Size	A
Date		Sheet	17 of 42

TITLE	Netbook
PAGE DETAIL	<Doc>

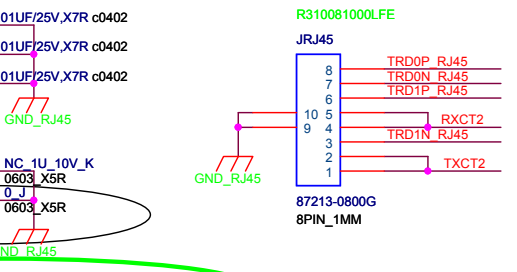
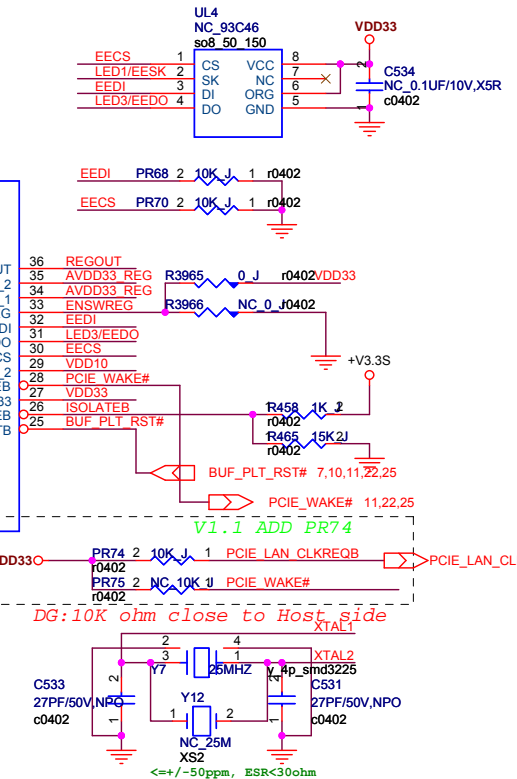


BITC **Bitland Information Technology Co.,Ltd.**
 4-6F, #7Building, Xili Tongfuyuan Industrial Town Nanshan District, Shenzhen

TITLE		Netbook	
ID	BM5080	Rev	1.2
DATE	HDA	Size	Custom
PAGE DETAIL	<Doc>	Sheet	18 of 42

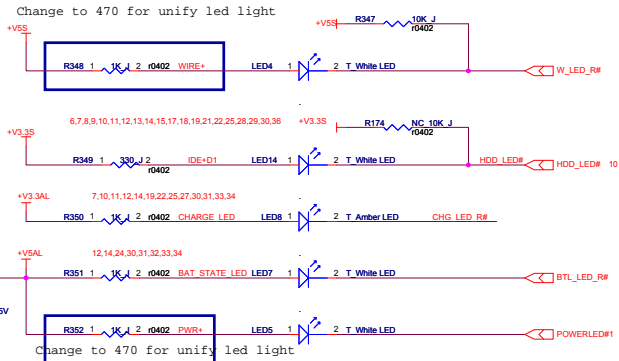


V1.1 20101203: SI
 ADD ESD15 ESD16 ESD17 ESD18
 ADD PF3
 R476 R477 R478 R479 CT 0603

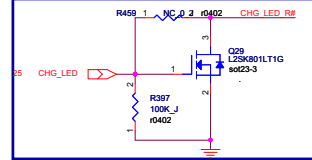


TITLE	Netbook
PAGE DETAIL	<Doc>

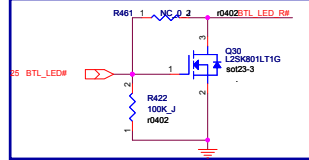
BITC Bitland Information Technology Co.,Ltd.		4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen	
BITC_PN	BM5080	Rev	1.2
ID	LAN	Size	B
Date		Sheet	19 of 42



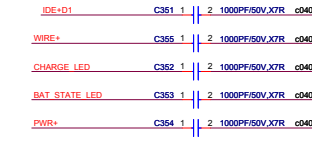
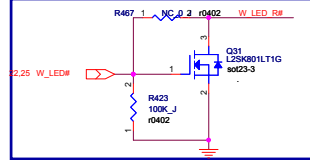
增加MOS, 高电平有效, 解决掉电LED闪烁问题



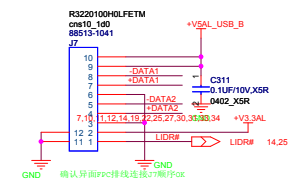
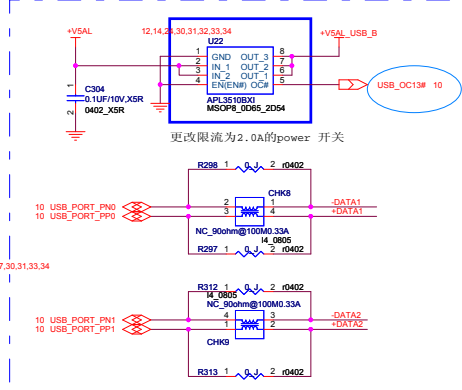
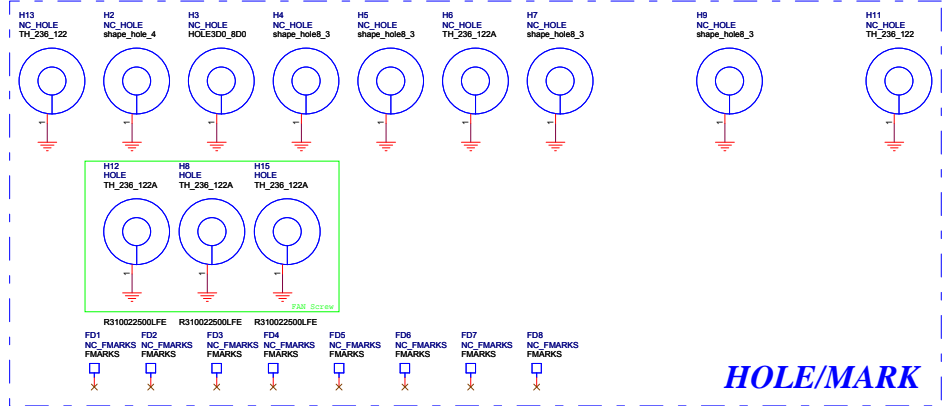
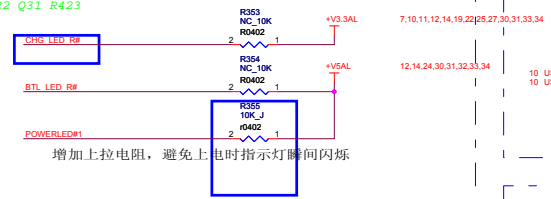
增加MOS, 高电平有效, 解决掉电LED闪烁问题



增加MOS, 高电平有效, 解决掉电LED闪烁问题

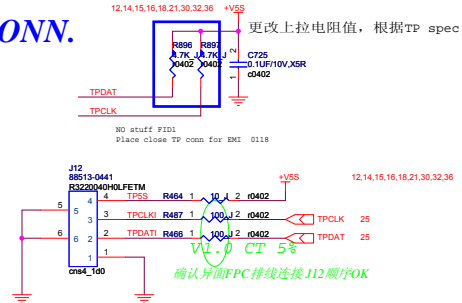


V1.1
DEL R459
ADD Q29 R397 Q30 R422 Q31 R423

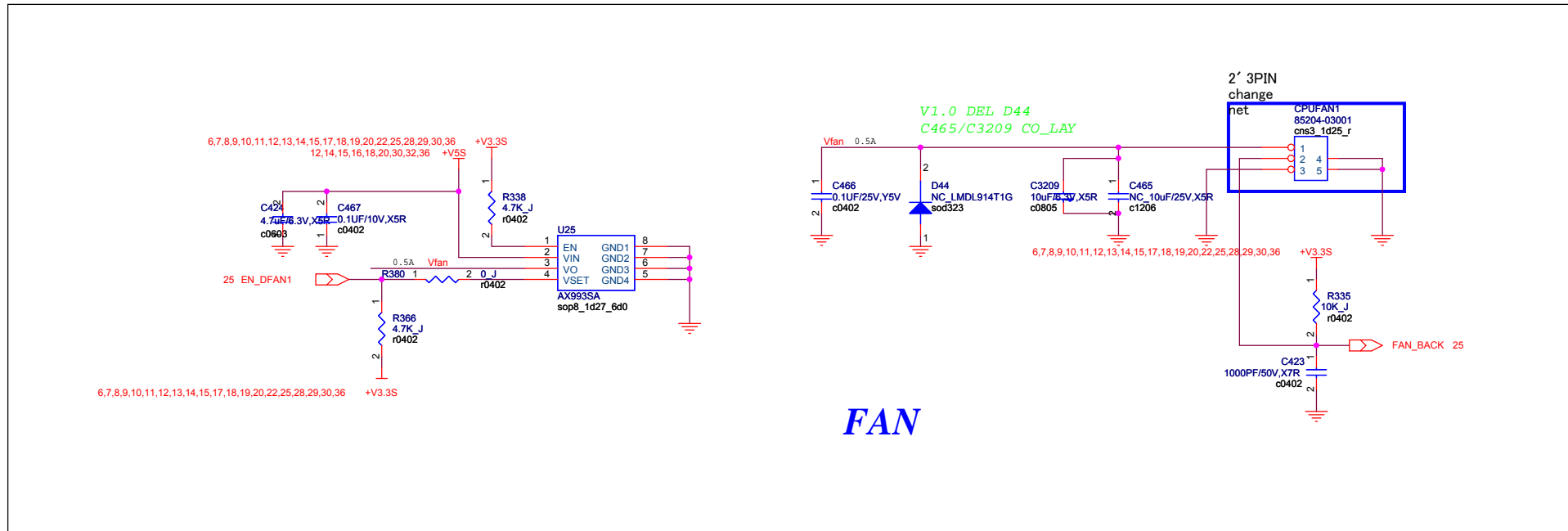



RJ45 DB CONN.

TOUCHPAD CONN.

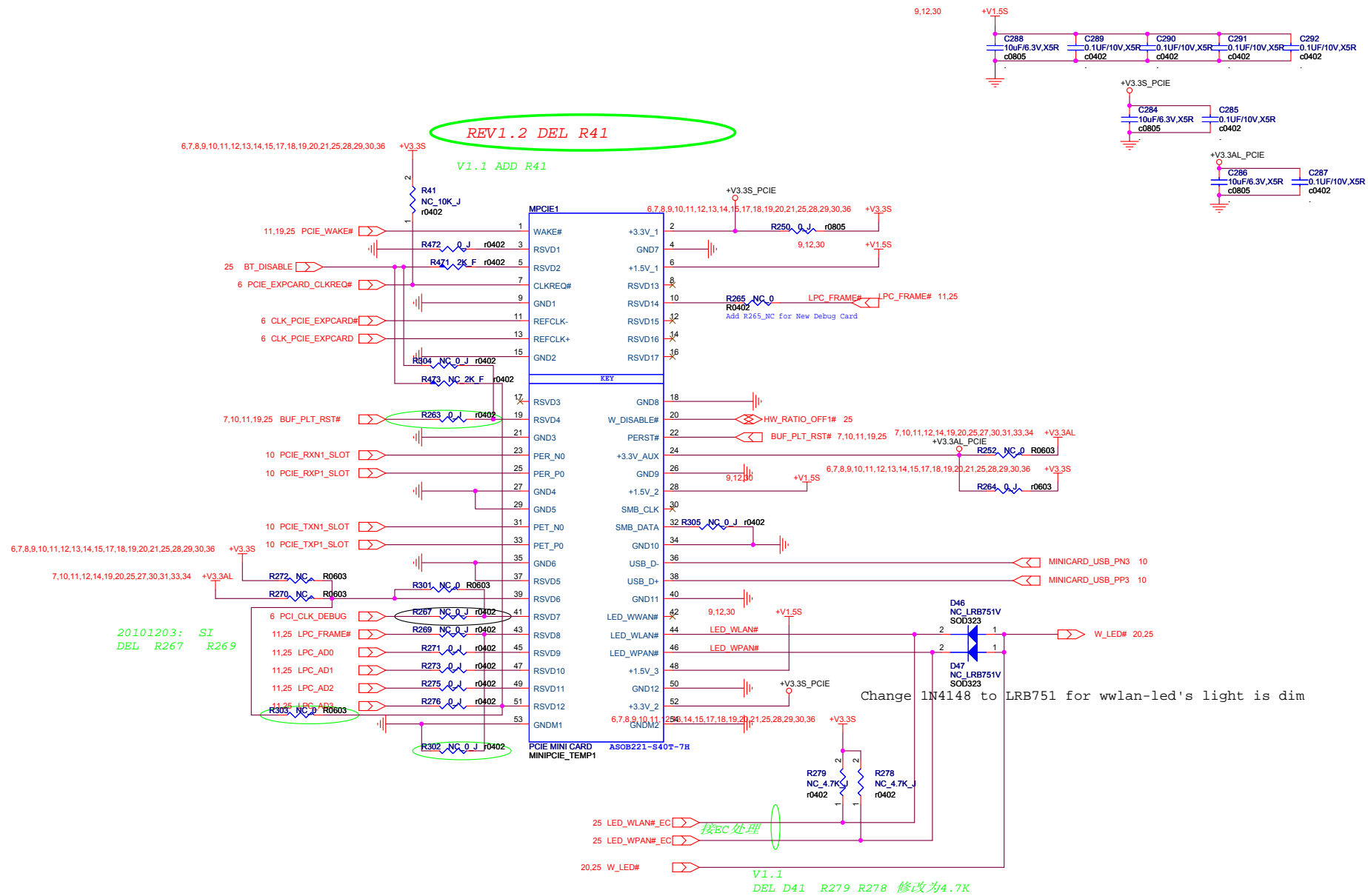


确认异面FPC排线连接J12顺序OK



 Bitland Information Technology Co.,Ltd. 4-6F,#7Building,XIII Tongfuyu Industrial Town Nanshan District,Shenzhen		Rev	1.2
		BITC_PN	BM5080
TITLE	Netbook	ID	BT&FAN
PAGE DETAIL	<Doc>	Date	Sheet 21 of 42

TITLE	Netbook
PAGE DETAIL	<Doc>



BITC		Bitland Information Technology Co.,Ltd.	
4-F, #7 Building, XIII Tongfuyu Industrial Town Nanshan District, Shenzhen			
BITC_PN	BM5080	Rev	1.2
ID	MINI_PCIE_SLOT1	Size	Custom
Date		Sheet	22 of 42

5

4

3

2

1

D

D

C

C

B

B

A

A



Bitland Information Technology Co.,Ltd.
4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen

TITLE Netbook
PAGE DETAIL <Doc>

BITC_PN	BM5080	Rev	1.2
ID	MINI_PCIE_SLOT2	Size	B
Date		Sheet	23 of 42

5

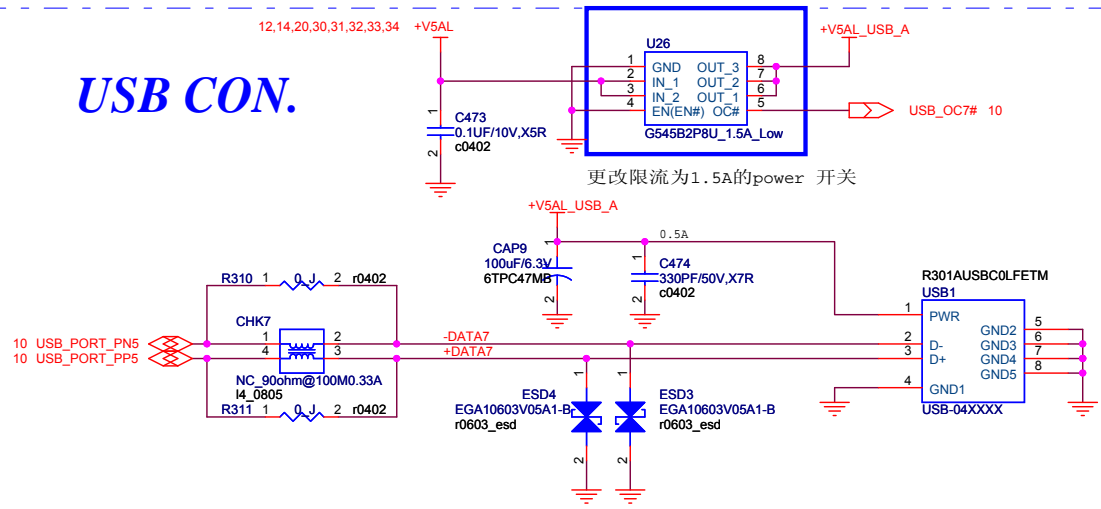
4

3

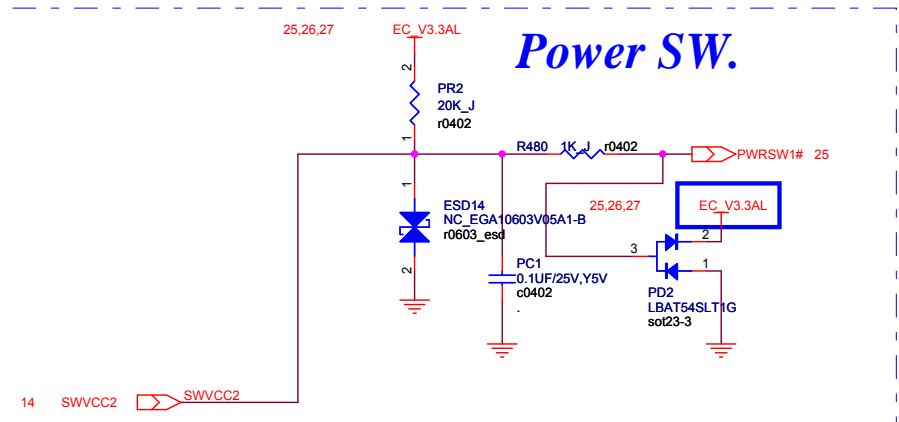
2

1

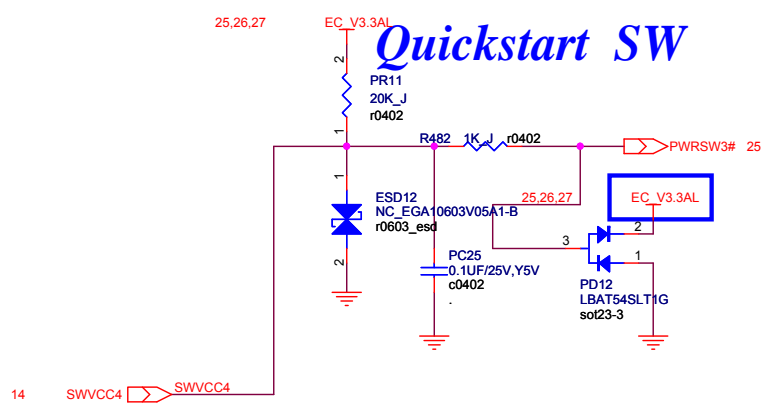
USB CON.



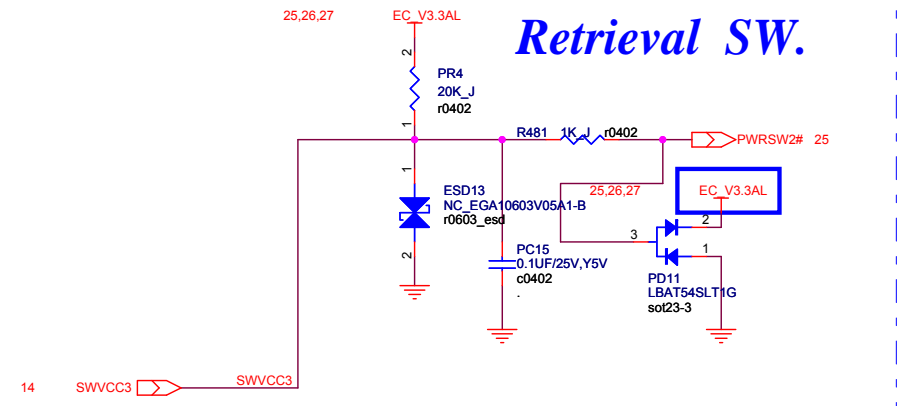
Power SW.



Quickstart SW

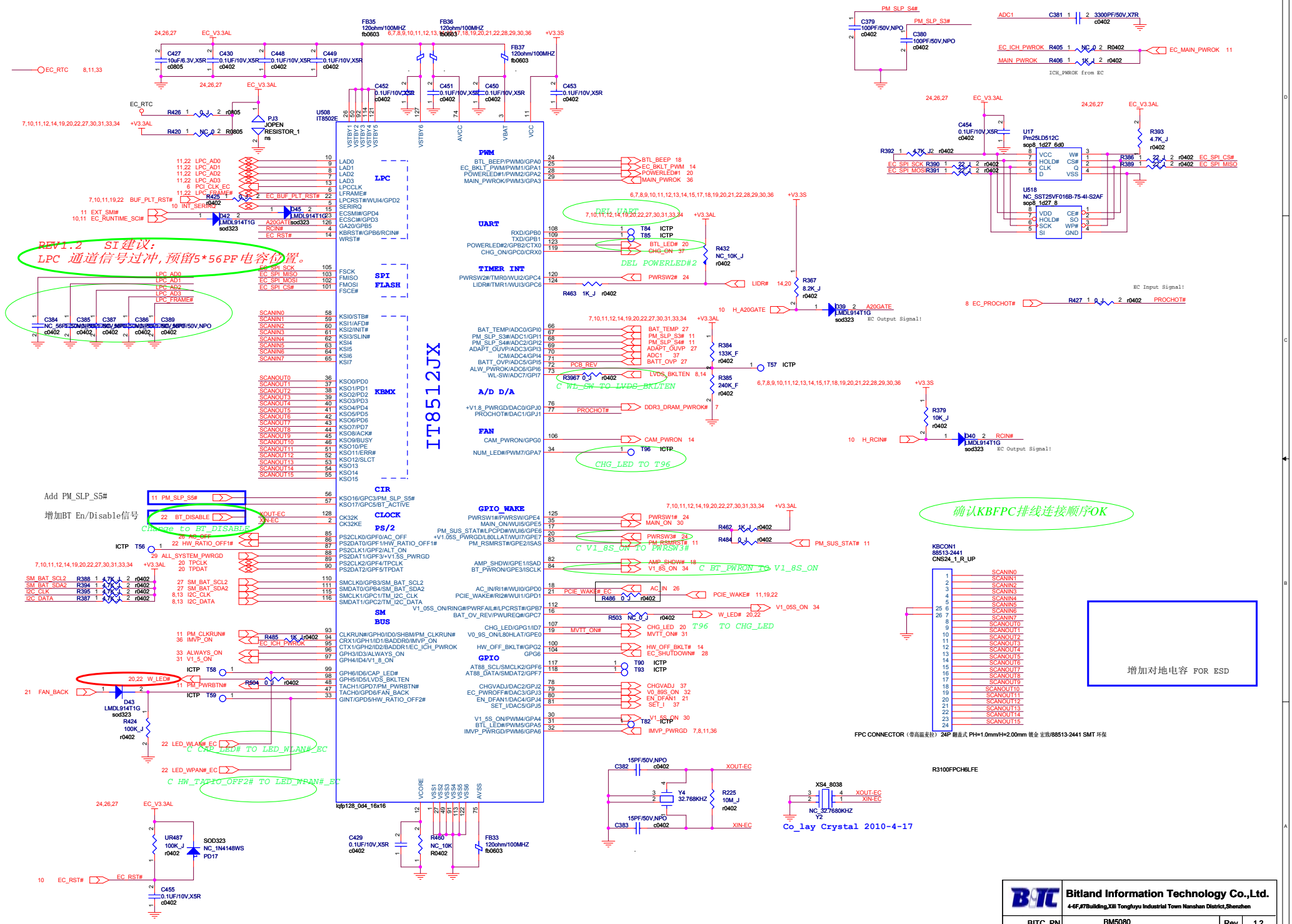


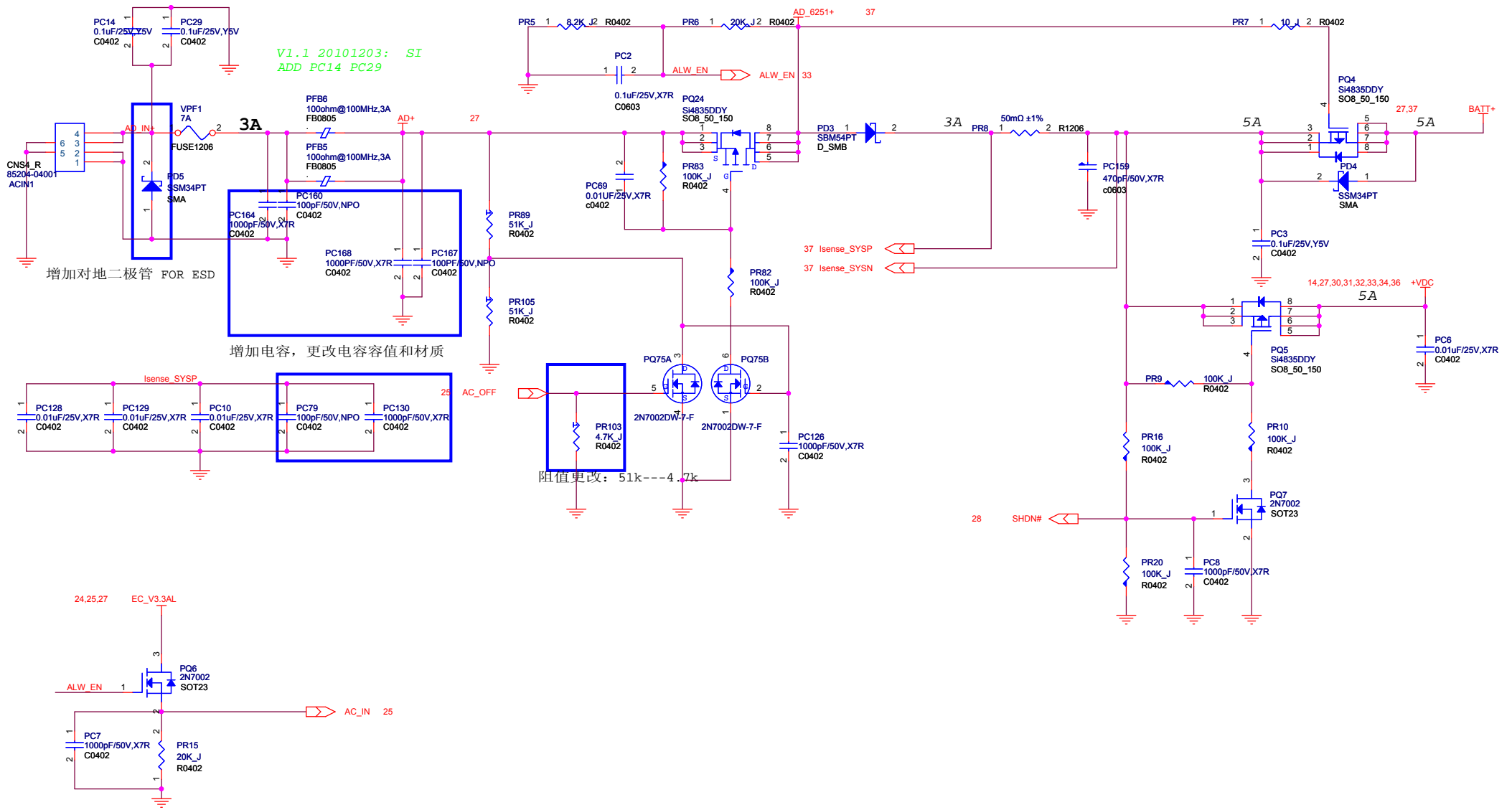
Retrieval SW.



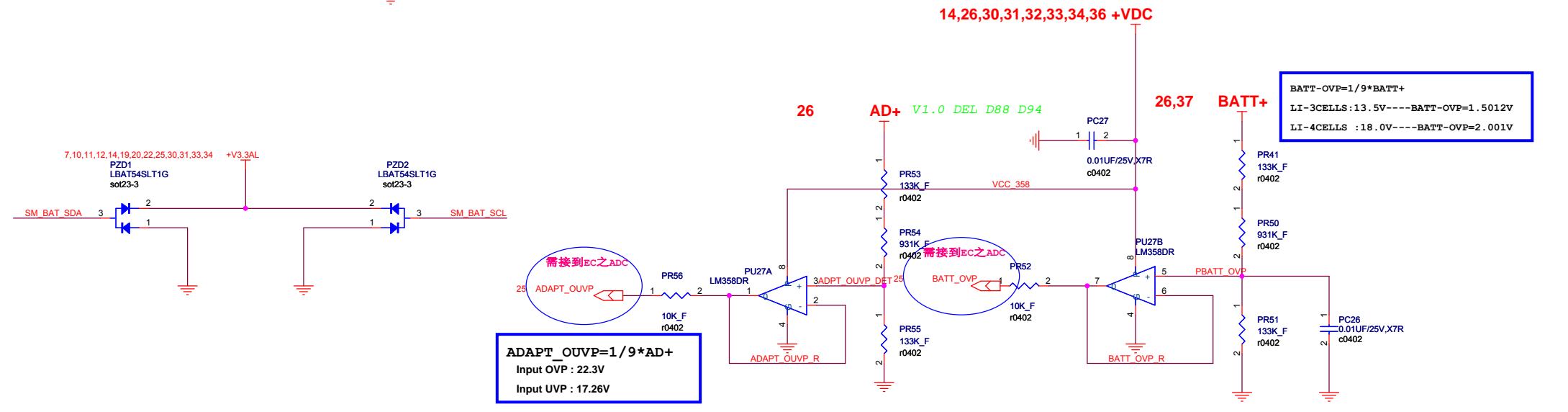
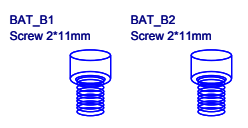
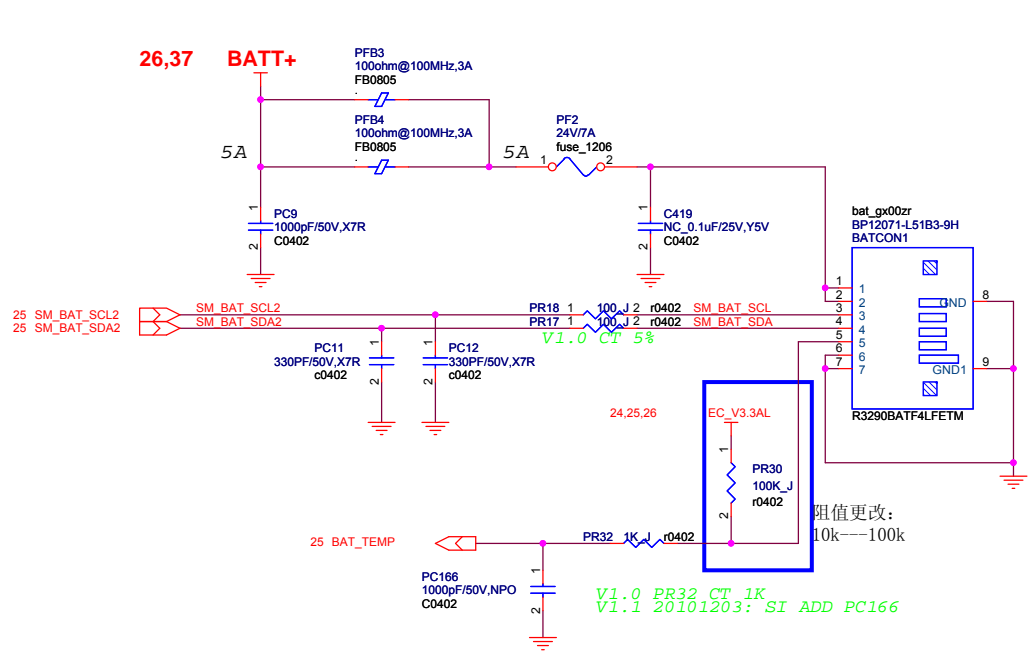
BITC		Bitland Information Technology Co.,Ltd.	
4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen			
BITC_PN	BM5080	Rev	1.2
ID	USB,LID,BWRBTN	Size	B
Date		Sheet	24 of 42

TITLE	Netbook
PAGE DETAIL	<Doc>



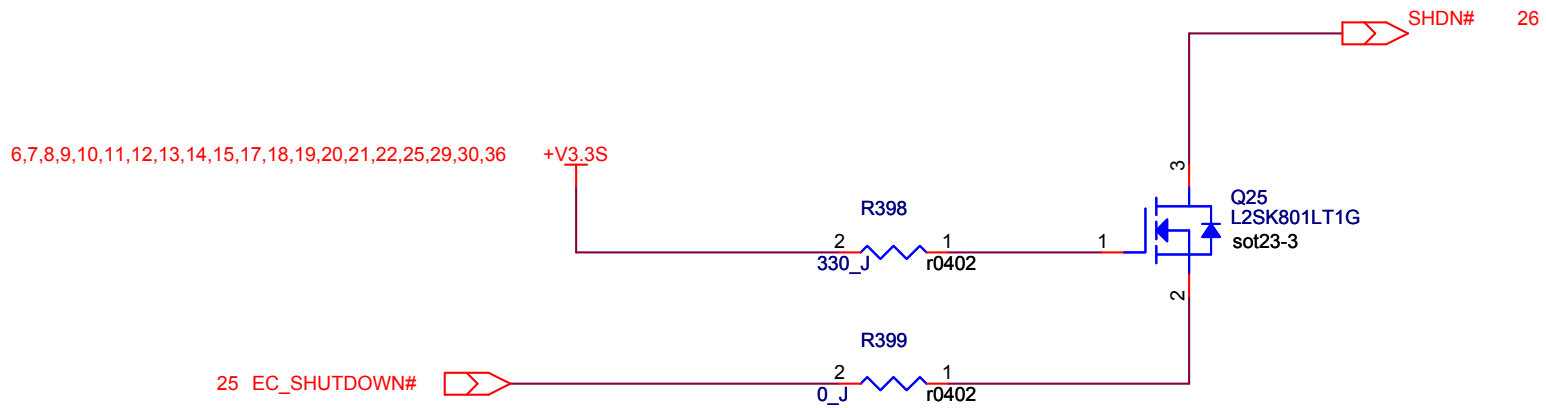


TITLE	Netbook	BITC_PN	BM5080	Rev	1.2
PAGE DETAIL	<Doc>	ID	ADAPTER	Size	A3
		Date		Sheet	26 of 42



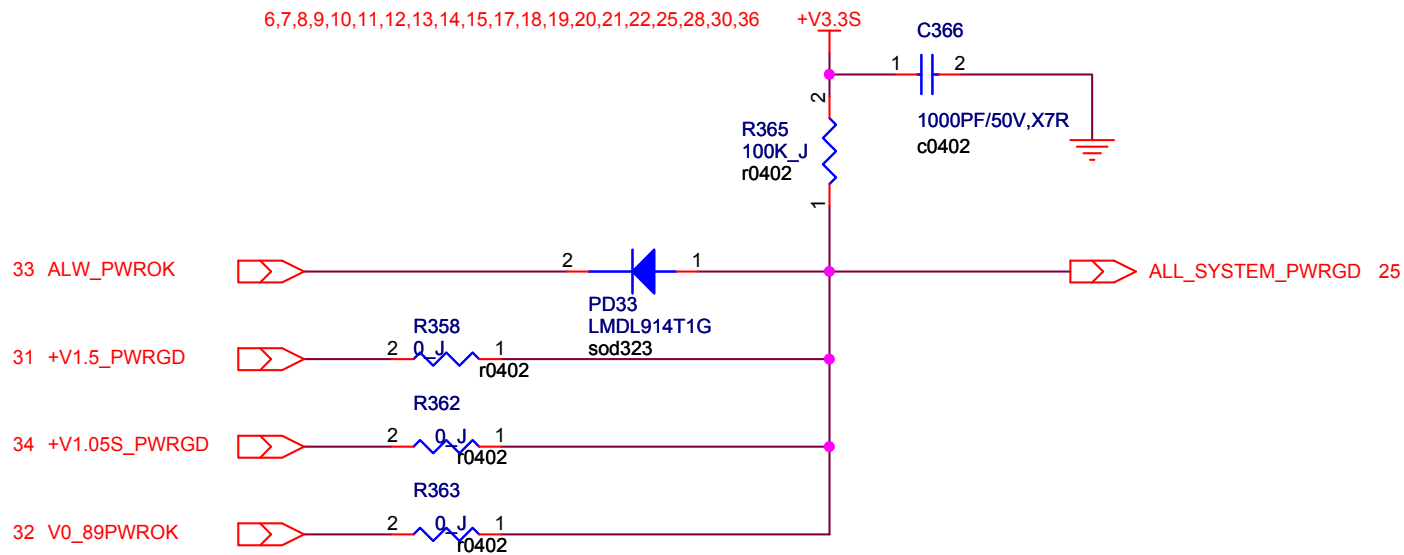
		Bitland Information Technology Co.,Ltd. 4-6F,#7Building,XIII Tongfuyu Industrial Town Nanshan District,Shenzhen	
		BITC_PN	BM5080
ID	BATTERY	Size	A3
Date		Sheet	27 of 42


TITLE	Netbook
PAGE DETAIL	<Doc>



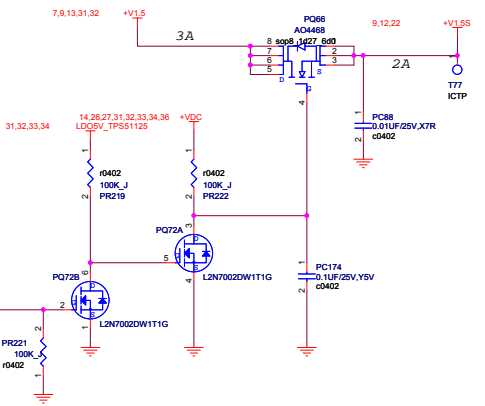
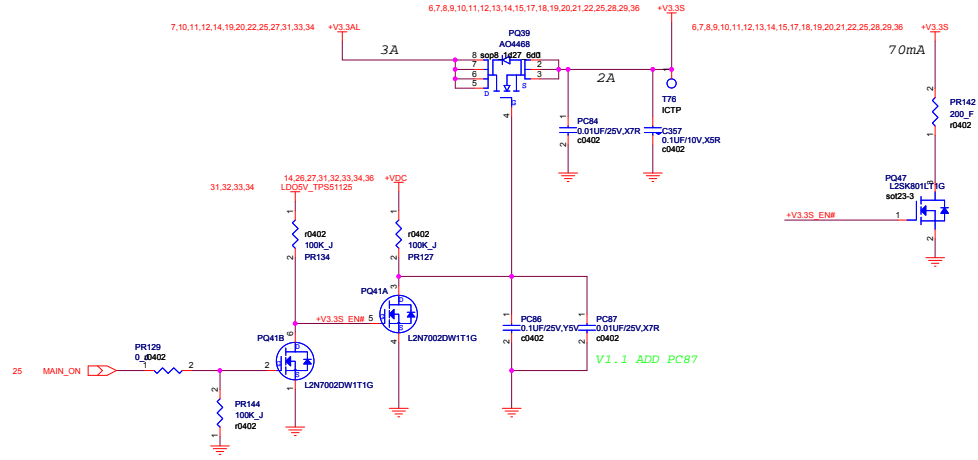
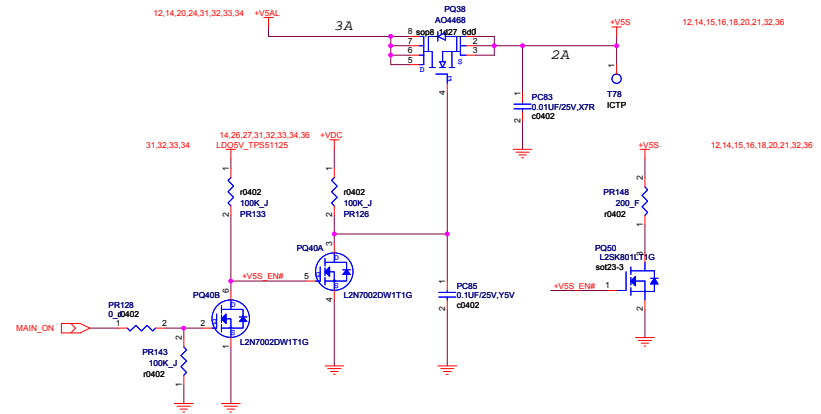
	Bitland Information Technology Co.,Ltd. 4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen		
	BITC_PN	BM5080	Rev 1.2
	ID	THERMAL PROTECT	Size A
	Date		Sheet 28 of 42

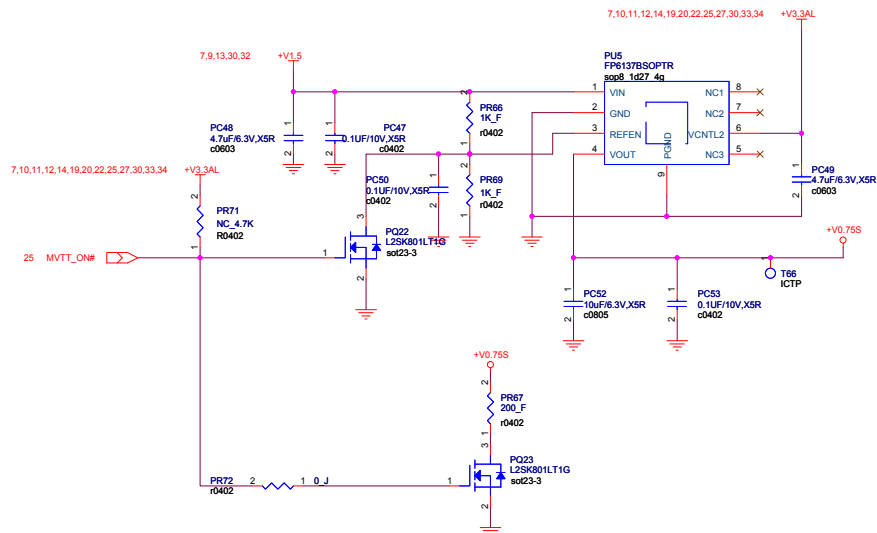
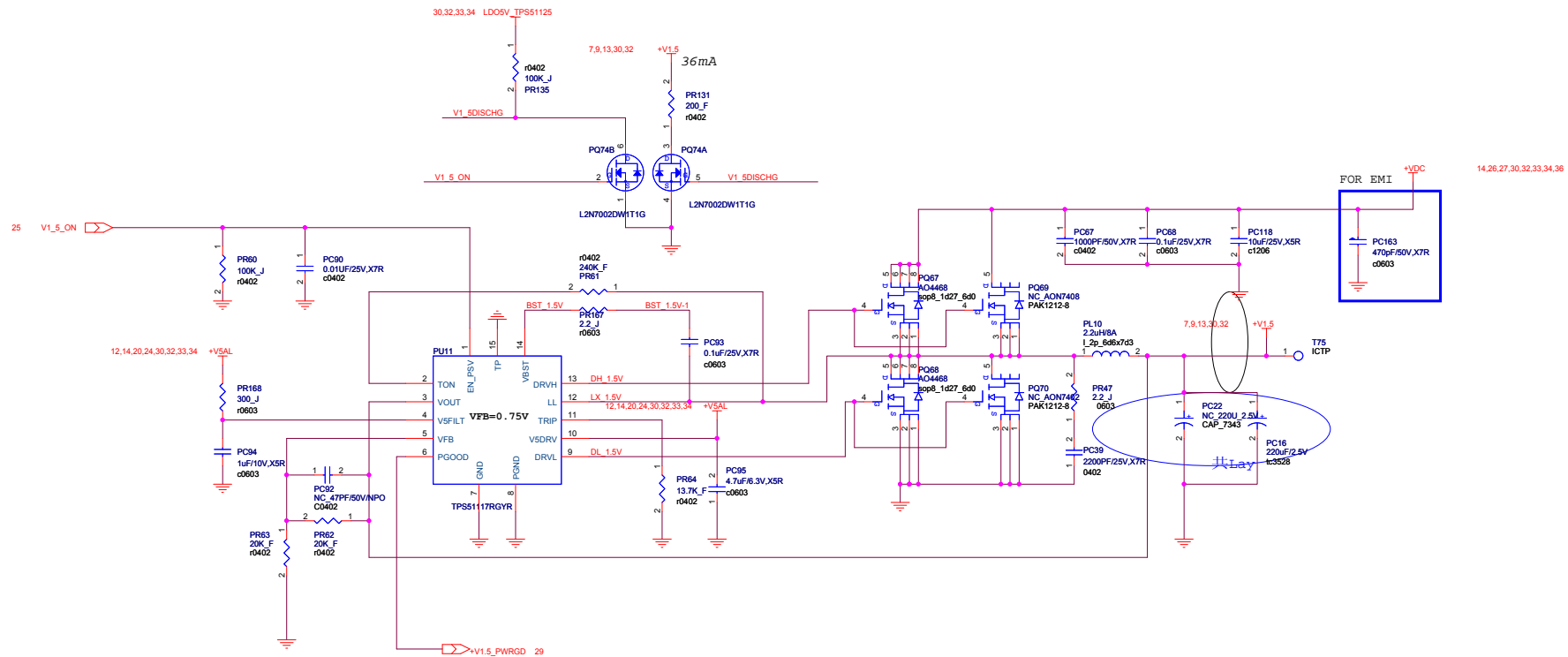
TITLE	Netbook
PAGE DETAIL	<Doc>



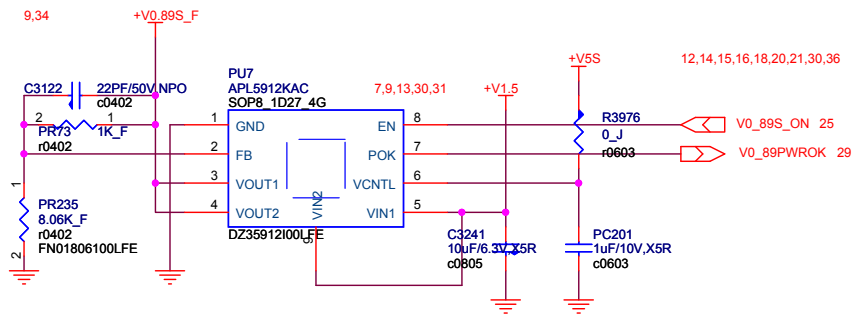
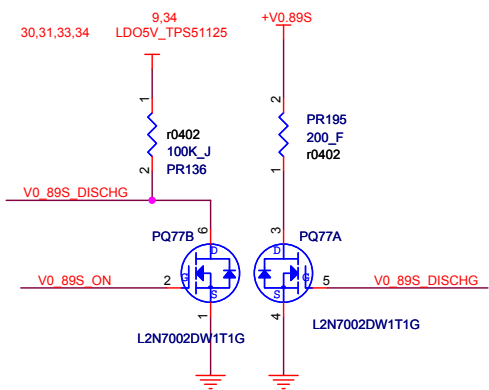
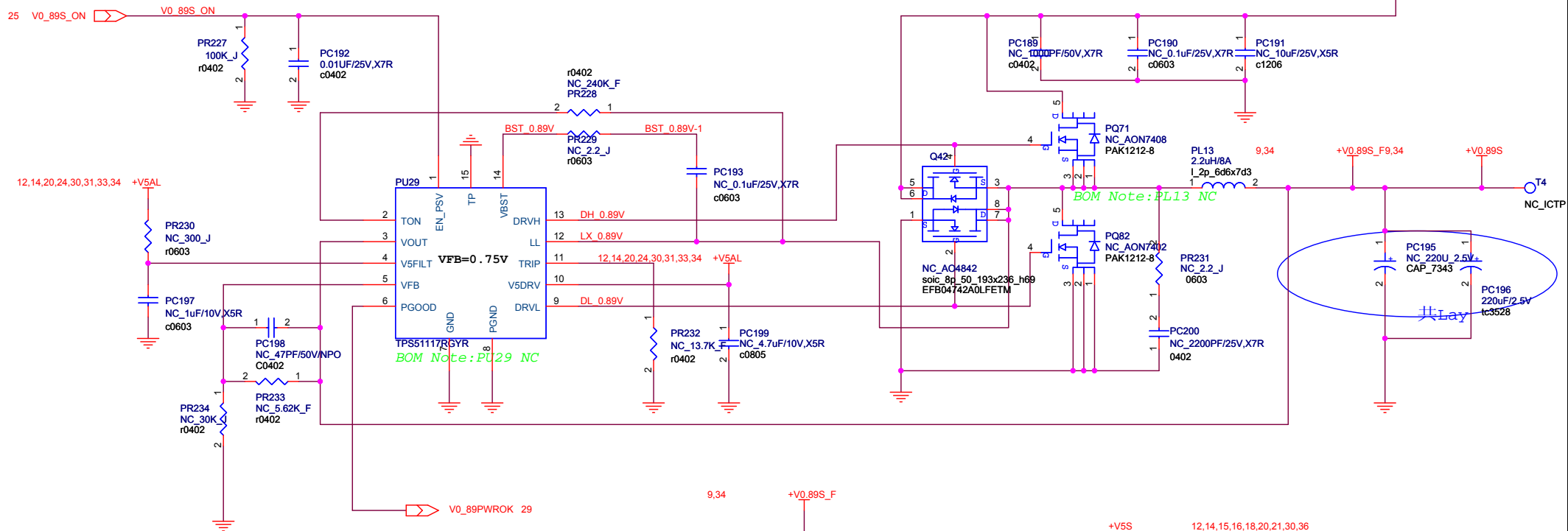
	Bitland Information Technology Co.,Ltd. 4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen		
	BITC_PN	BM5080	Rev 1.2
	ID	POWER OVP	Size A
	Date		Sheet 29 of 42

TITLE	Netbook
PAGE DETAIL	<Doc>





BITC Bitland Information Technology Co.,Ltd.		4-6F, #7Building, XII Tongfuyu Industrial Town Nanshan District, Shenzhen	
BITC_PN	BM5080	Rev	1.2
ID	DDR POWER	Size	C
Date		Sheet	1 of 42

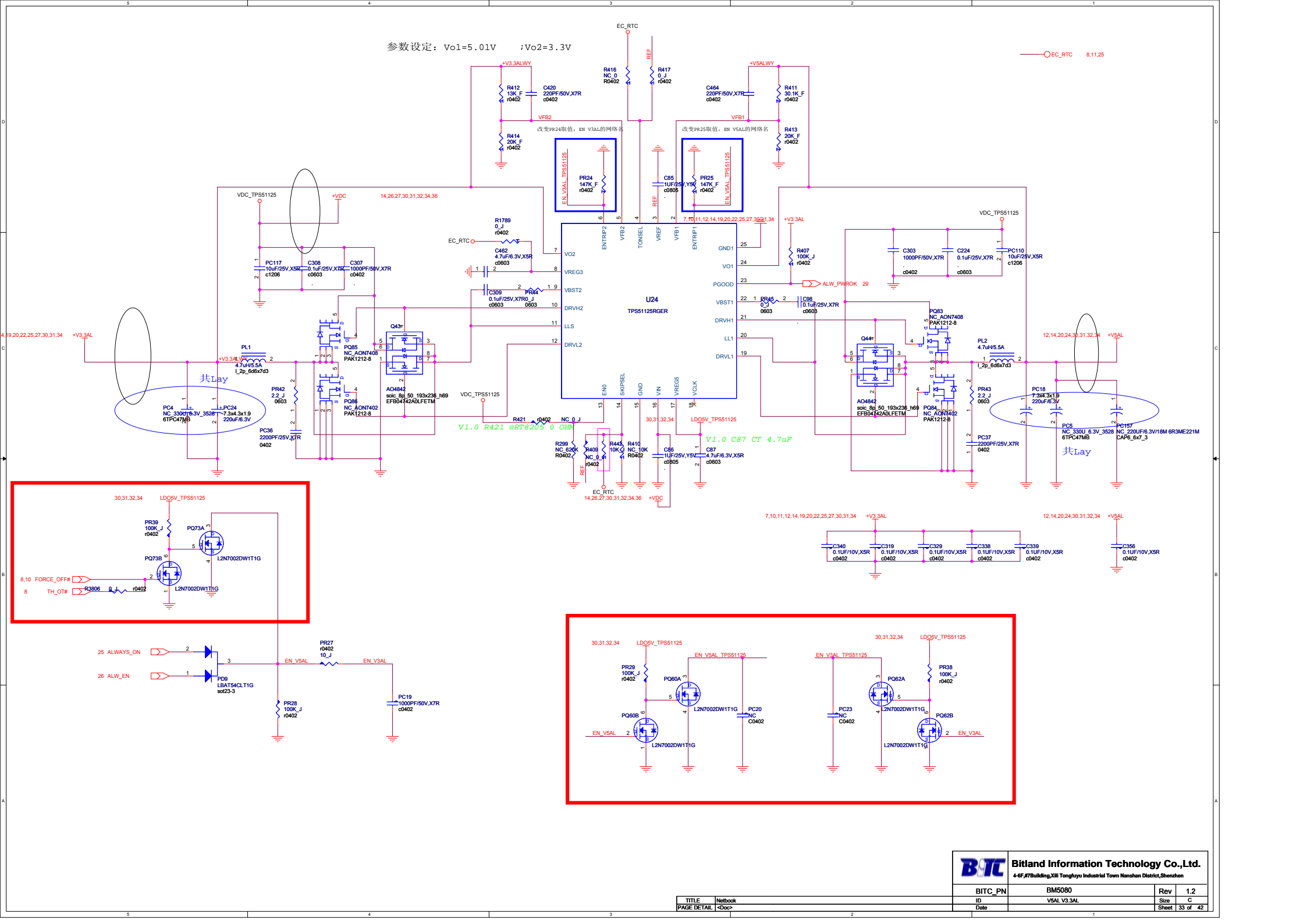


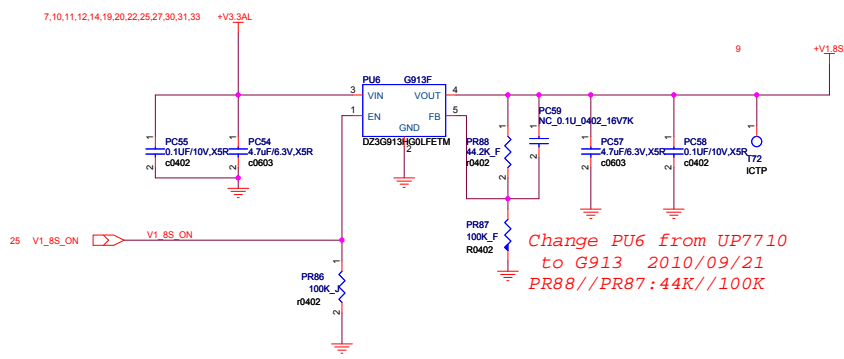
- ==== +V3.3AL 7,10,11,12,14,19,20,22,25,27,30,31,33,34
- ==== +VDC 14,26,27,30,31,33,34,36
- ==== +V0.89S 9,34
- ==== +V5S 12,14,15,16,18,20,21,30,36
- ==== +V3.3S 6,7,8,9,10,11,12,13,14,15,17,18,19,20,21,22,25,28,29,30,36

BIT		Bitland Information Technology Co.,Ltd	
Page Name		+V0.89S/+V0.9S DDR(Ti)	
Size B	Project Name	BM5080	Rev 1.2
Date:	Sheet 32 of 42		
PROPERTY NOTE: this document contains information confidential and property to Bitland Technology Co.,Ltd. and shall not be reproduced or transferred to other documents or disclosed to others or used for any purpose other than that for which it was obtained with the expressed written consent of Bitland			

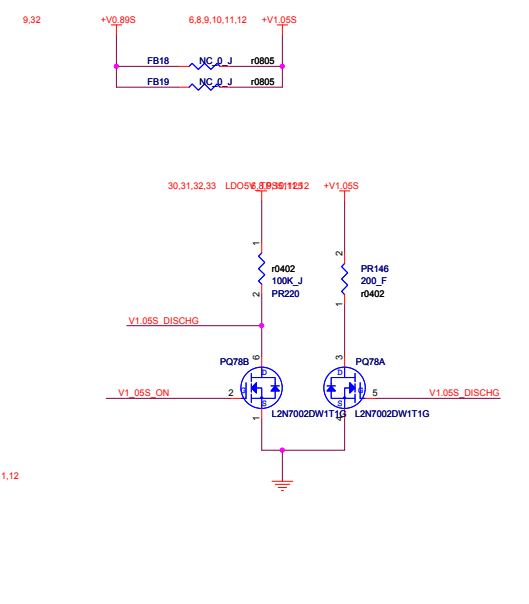
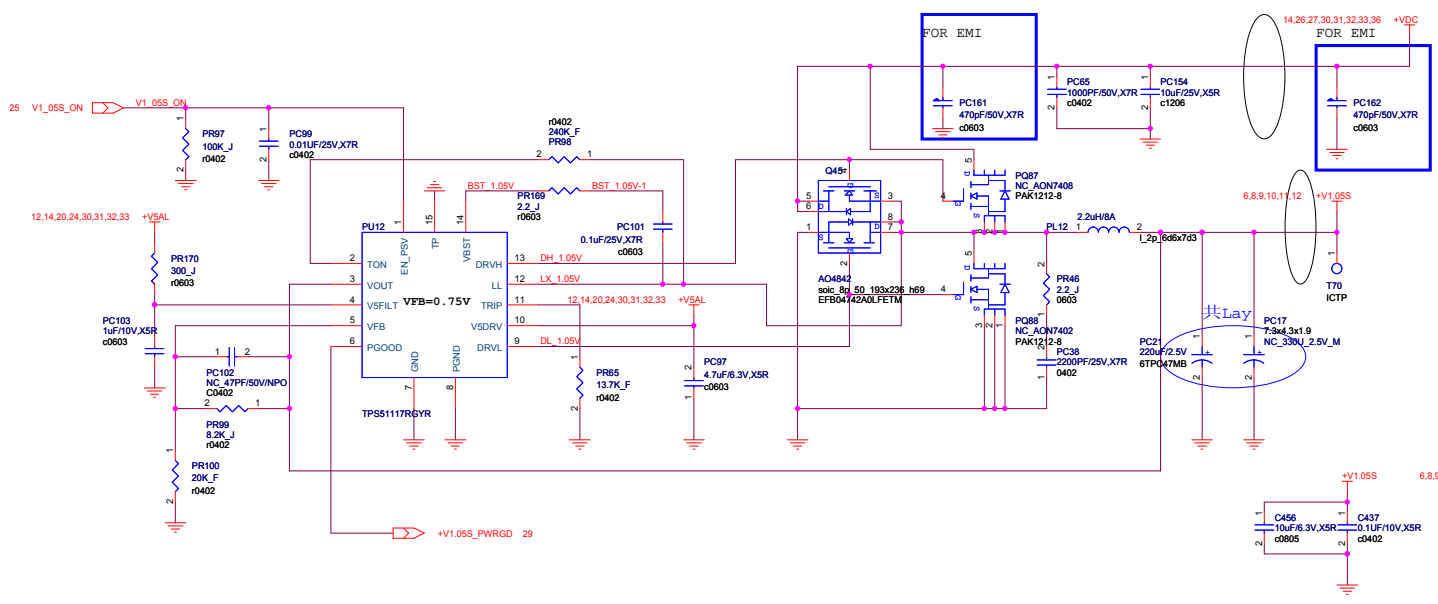
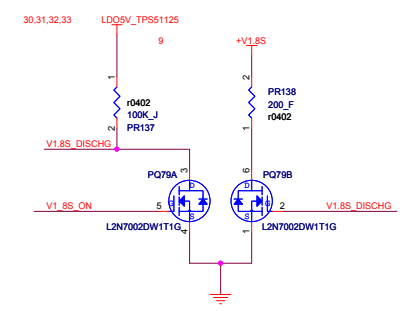
参数设定: Vo1=5.01V ;Vo2=3.3V

EC_RTC 8.11.25





Change PU6 from UP7710 to G913 2010/09/21
PR88//PR87:44K//100K



BITC		Bitland Information Technology Co.,Ltd.	
4-FF,#7Building,XIII Tongfuyu Industrial Town Nanshan District, Shenzhen			
BITC_PN	BM5080	Rev	1.2
ID	V1.8S V1.05S	Size	C
Date		Sheet	34 of 42

5

4

3

2

1

D

D

C


C

B

B

A

A

	Bitland Information Technology Co.,Ltd.		
	<small>4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen</small>		
	BITC_PN	BM5080	Rev
ID	V2.5S	Size	A4
Date		Sheet	35 of 42

TITLE	Netbook
PAGE DETAIL	<Doc>

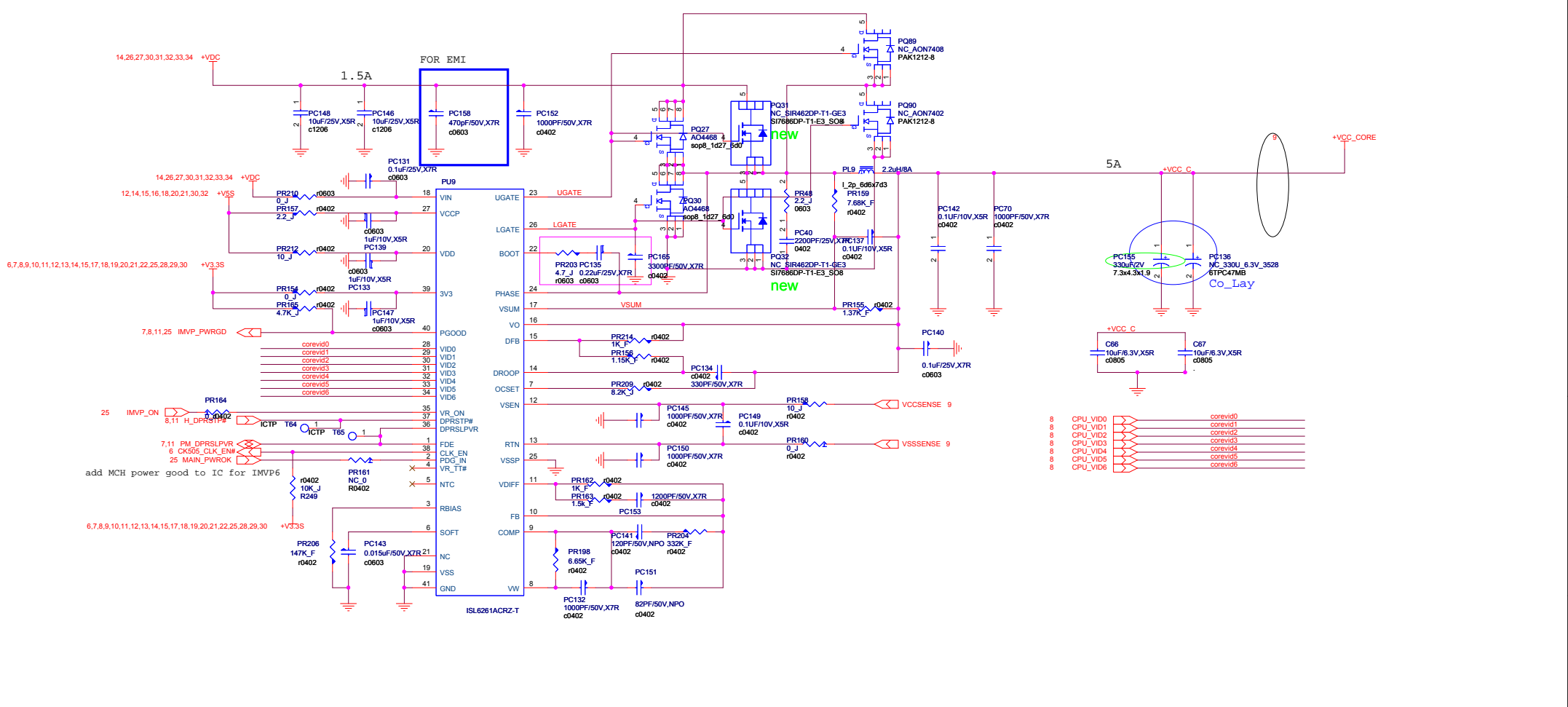
5

4

3

2

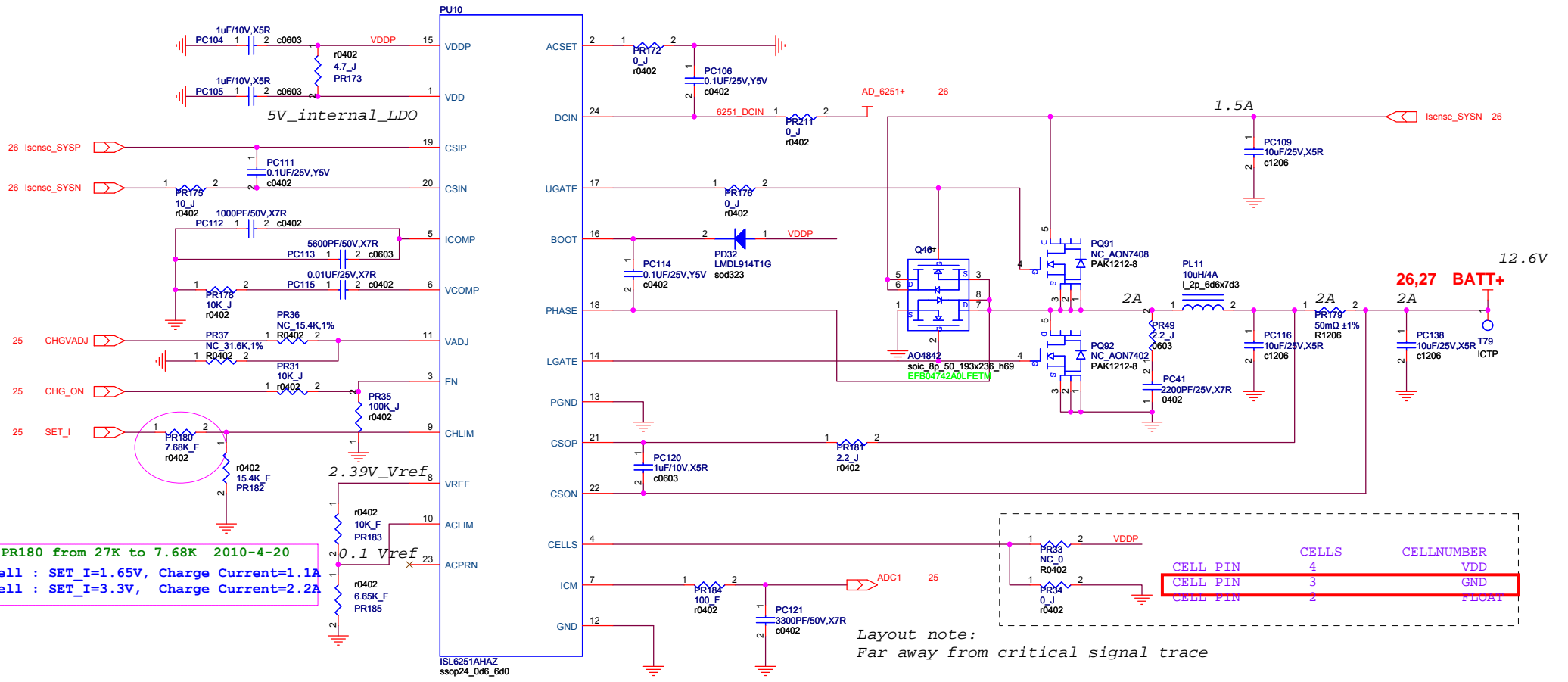
1



- 8 CPU_VID0 >>> corevid0
- 8 CPU_VID1 >>> corevid1
- 8 CPU_VID2 >>> corevid2
- 8 CPU_VID3 >>> corevid3
- 8 CPU_VID4 >>> corevid4
- 8 CPU_VID5 >>> corevid5
- 8 CPU_VID6 >>> corevid6

BITC Bitland Information Technology Co.,Ltd.
 4-F, #7Building, XH Tongfuyu Industrial Town Nanshan District, Shenzhen

TITLE	Netbook	BITC_PN	BM5080	Rev	1.2
PAGE DETAIL	<Doc>	ID	CPU_VCORE	Size	Custom
		Date		Sheet	36 of 42



Change PR180 from 27K to 7.68K 2010-4-20
 For 3 Cell : SET_I=1.65V, Charge Current=1.1A
 6 Cell : SET_I=3.3V, Charge Current=2.2A

CELLS	CELLNUMBER
CELL PIN 4	VDD
CELL PIN 3	GND
CELL PIN 2	FLOAT

Layout note:
 Far away from critical signal trace

设置适配器限流值为
 50mV/25m ohm=2.0A.

$$I_{aclim} = 1/PR8 * (0.05 * V_{aclim} / V_{ref} + 0.05)$$

SET_I 充电电流

0V	0A
0.66V	400mA
3.3V	2A

$$I_{chg} = 165mV / PR179 * (V_{chlim} / 3.3V)$$

20101022_____V1.0

20101126_____V1.1

1. Page6 ADD R3773 R3774 R3772
2. Page11 ADD R42
3. Page14 DEL Q9 R155 R156 PC172
4. Page18 ADD D99
5. Page18 Modify Codec Combo Jack circuit
6. Page 22 ADD R41
7. Page 28 ADD PC87
8. Page14 移动 C346 D48 到LVDS CN附近

20110124_____V1.2

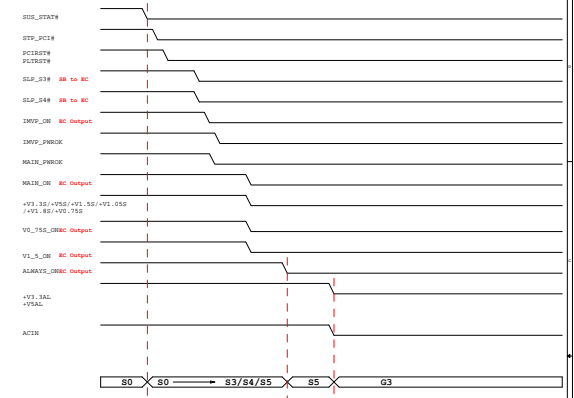
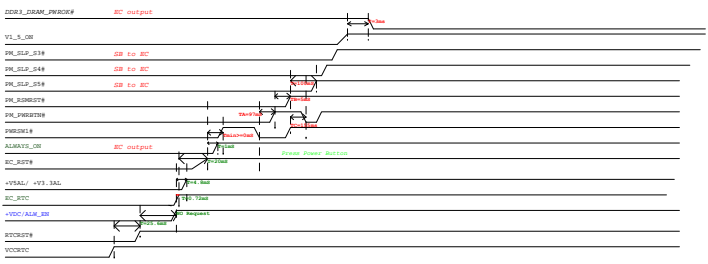
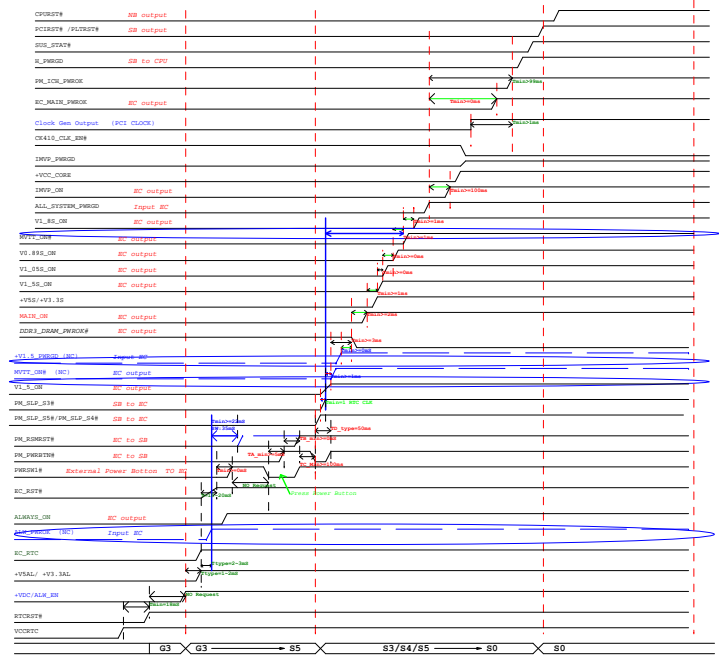
1. Page 6 R3766 CT 10 OHM.
Page 6 DEL R3772 R3774
2. Page14 Del C347 D49
3. Page17 change R11'Footprint from 0603 to 0402 。
4. DEL ALL Power Jumpers
5. Page25 LPC 通道上预留56PF电容位置
6. Page19 DEL R477 R478 R479
增加 C38 位置0603 0 OHM电阻
增加 LD1
7. Page11 DEL R42
8. Page22 DEL R41

	Bitland Information Technology Co.,Ltd.		
	4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen		

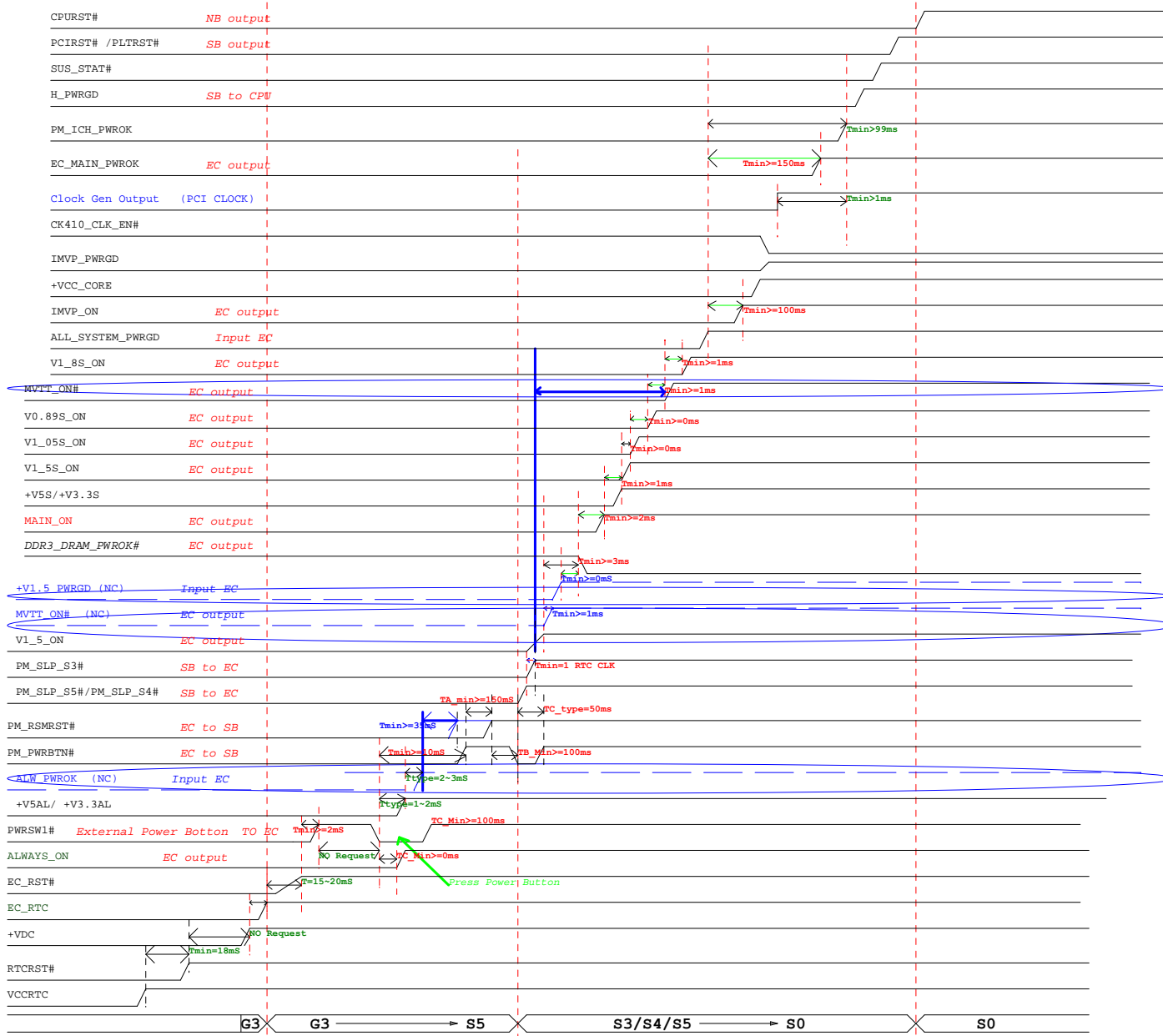
BITC_PN	BM5080	Rev	1.2
ID	History	Size	B
Date		Sheet	38 of 42

TITLE	Netbook
PAGE DETAIL	<Doc>

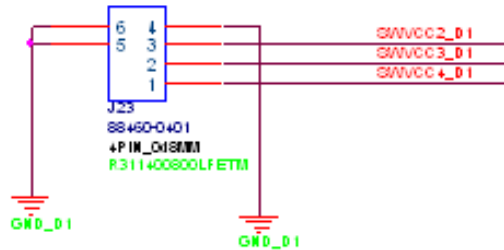
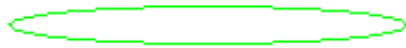
BM5XXX Power On/Off Sequence Specification(Adapter Mode)



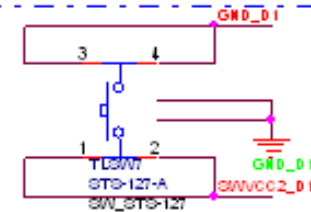
BM5XXX Power On/Off Sequence Specification(Battery Mode)



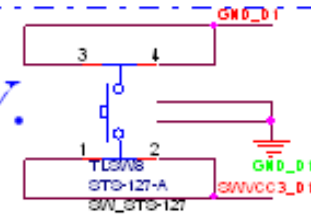
onboard stereo microphone



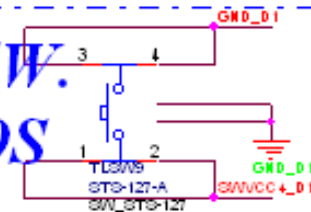
Power SW.



Retrieval SW.



Quickstart SW. For Meego OS



Power Switch DB



Bitland Information Technology Co.,Ltd.

4-6F,#7Building,Xili Tongfuyu Industrial Town Nanshan District,Shenzhen

BITC_PN

BM5080

Rev

1.2

ID

DB LED/MIC

Size

A

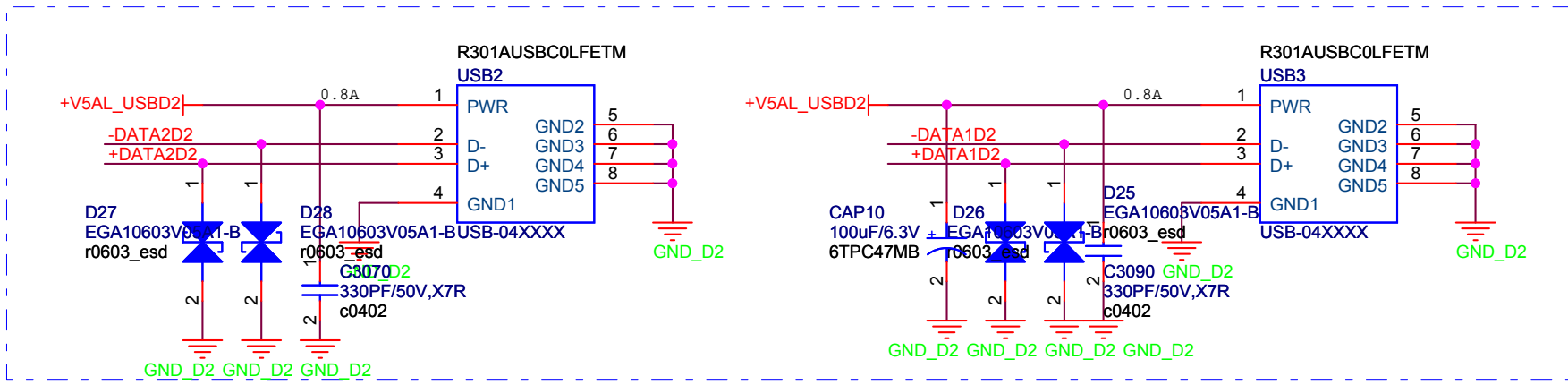
Date

Sheet

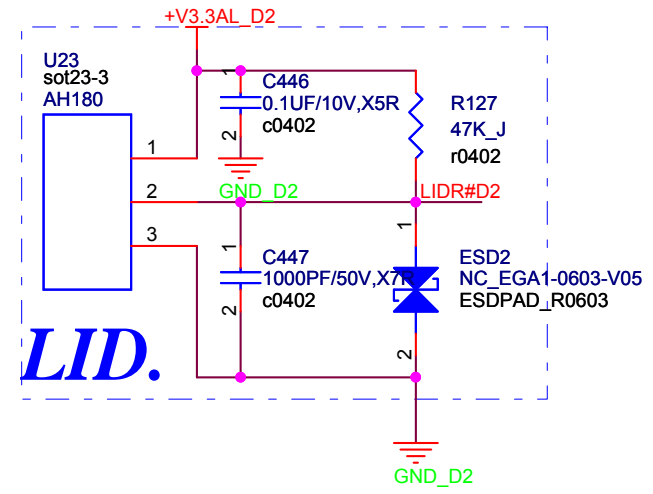
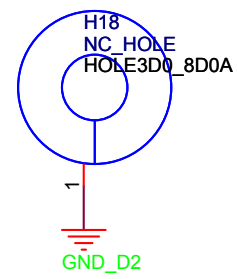
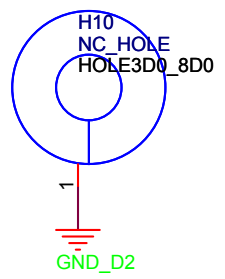
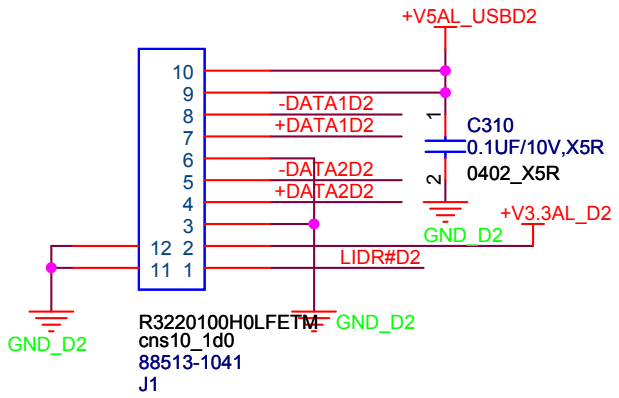
41 of 42

TITLE Netbook

PAGE DETAIL <Doc>



确认异面FPC排线连接J1顺序OK



USB/LID DB

BITC Bitland Information Technology Co.,Ltd.
 4-6F, #7Building, Xili Tongfuyu Industrial Town Nanshan District, Shenzhen

BITC_PN	BM5080	Rev	1.2
ID	DB USB/WL-SW	Size	A
Date		Sheet	42 of 42

TITLE	Netbook
PAGE DETAIL	<Doc>