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RYU2-13 CALPELLA UMA Schematics

Intel ULV CPU-Arrandale SFF

Intel Ibex Peak-M

2010-09-28

REV : A00

DY : Nopop Component

<Core Design>

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Title: Cover Page

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RYU2 CALPELLA Block Diagram

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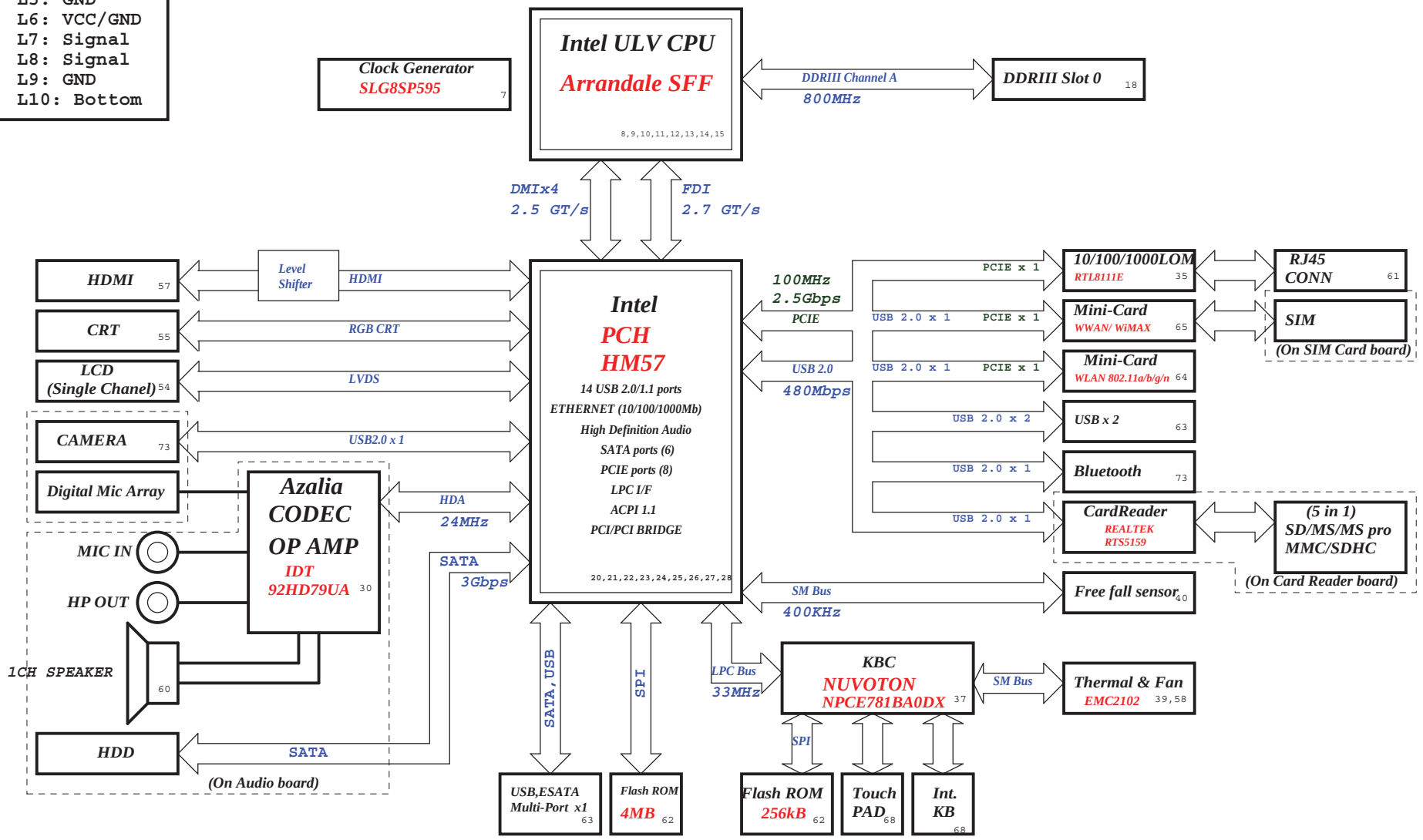
Project code	:	91.4M101.001
Part Number	:	48.4M101.0SB
PCB P/N	:	10251
Revision	:	SB

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: GND
L6: VCC/GND
L7: Signal
L8: Signal
L9: GND
L10: Bottom



CPU DC/DC RT8152DGQW-GP 47

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51123RGER 46

INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC RT8207LGQW-GP-U 50

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC ADP3211 53

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

CHARGER BQ24745 45

INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51218 49

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8209PGQW 49

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_PCH

SYSTEM DC/DC TPS51311RGTR 51

INPUTS	OUTPUTS
+3.3V_RUN	+1.8V_RUN

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Title: Block Diagram

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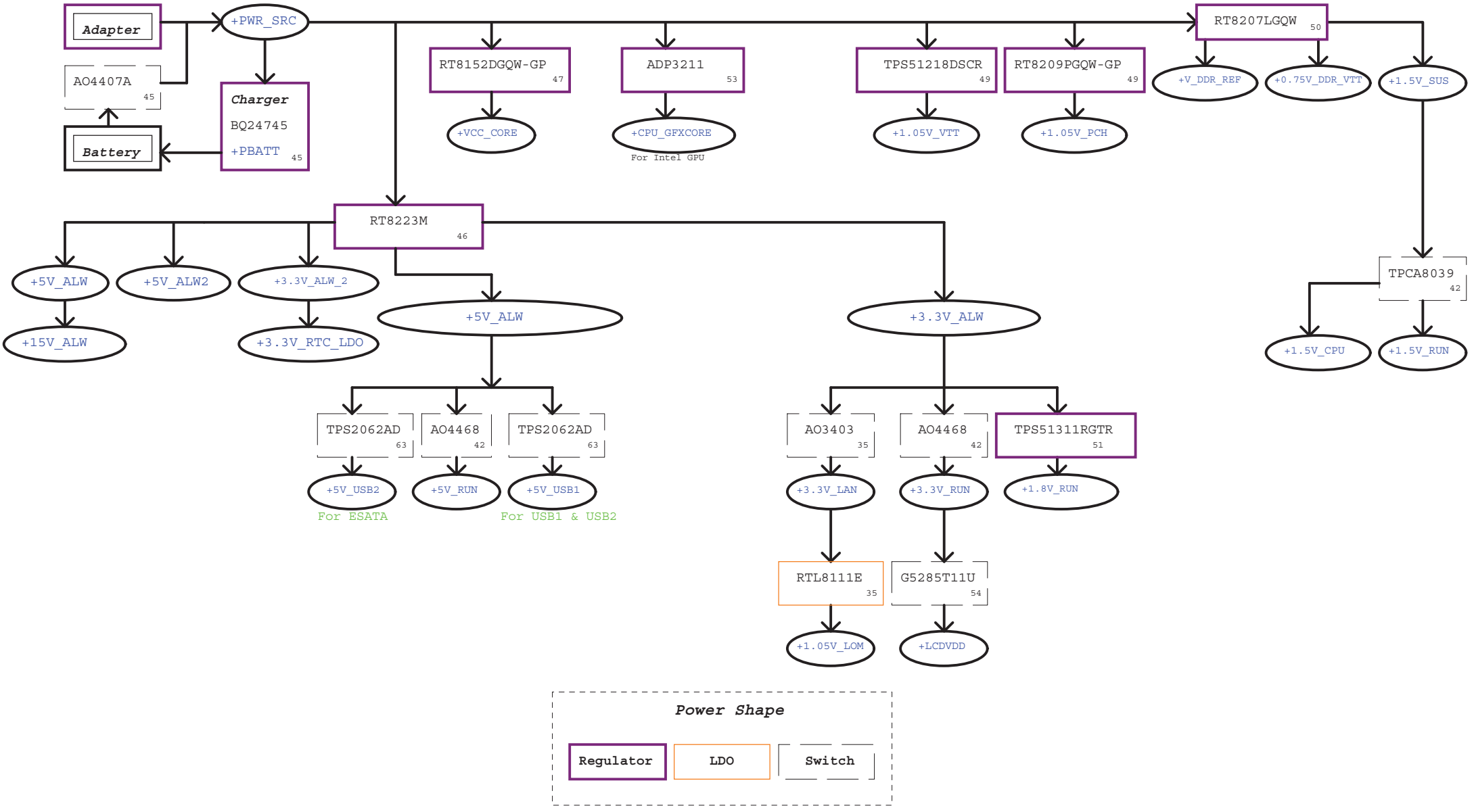

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Title: Power Block Diagram

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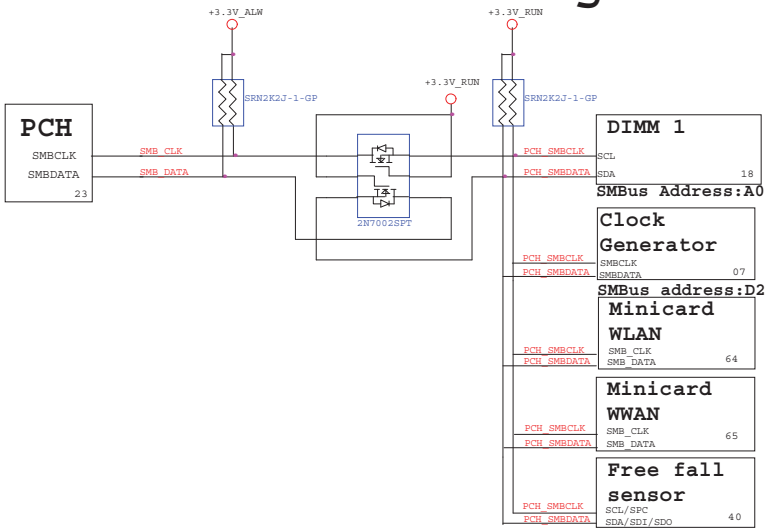
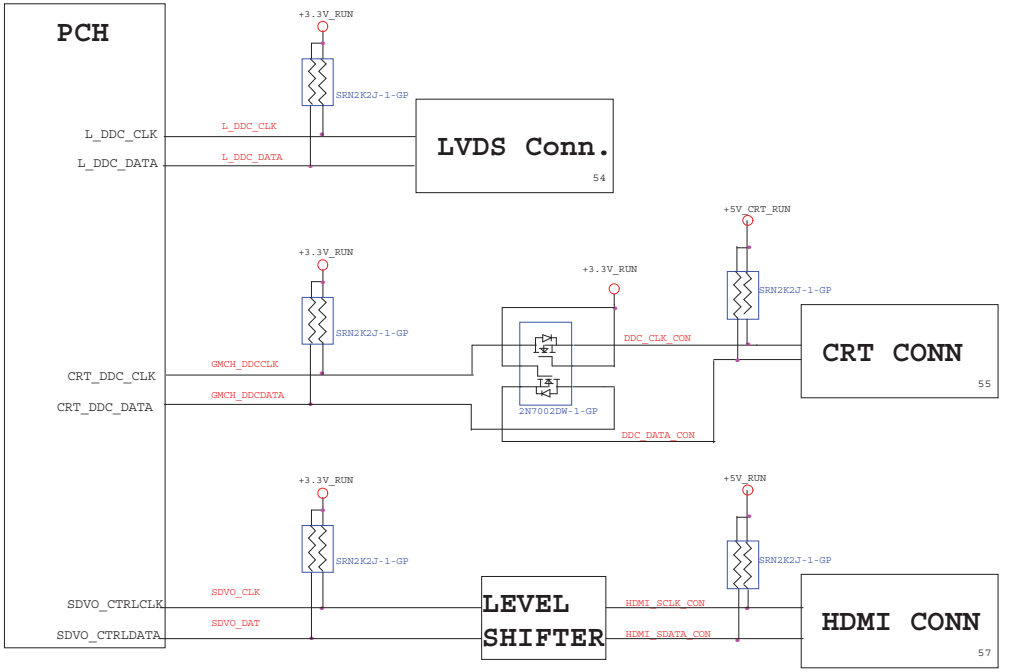
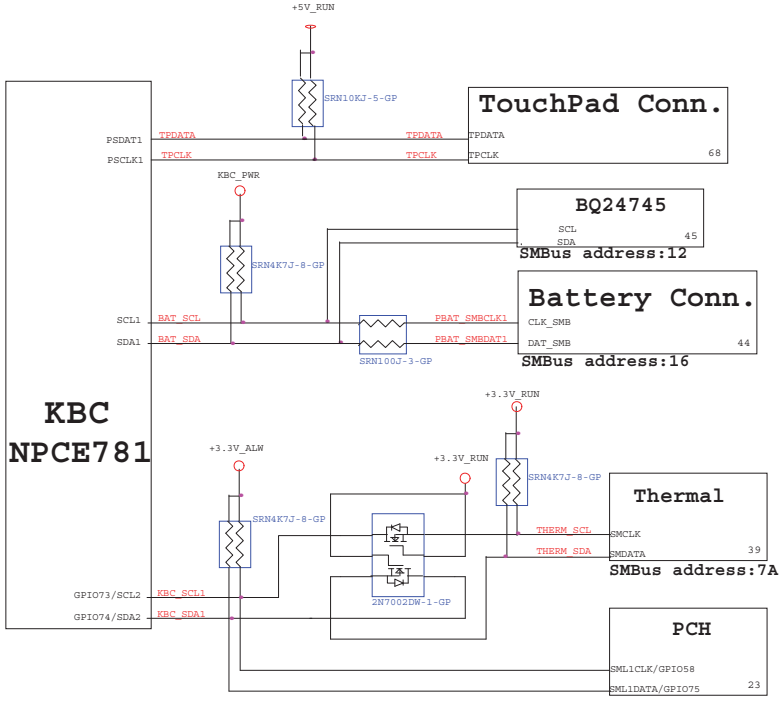
PCH SMBus Block Diagram



Graphic SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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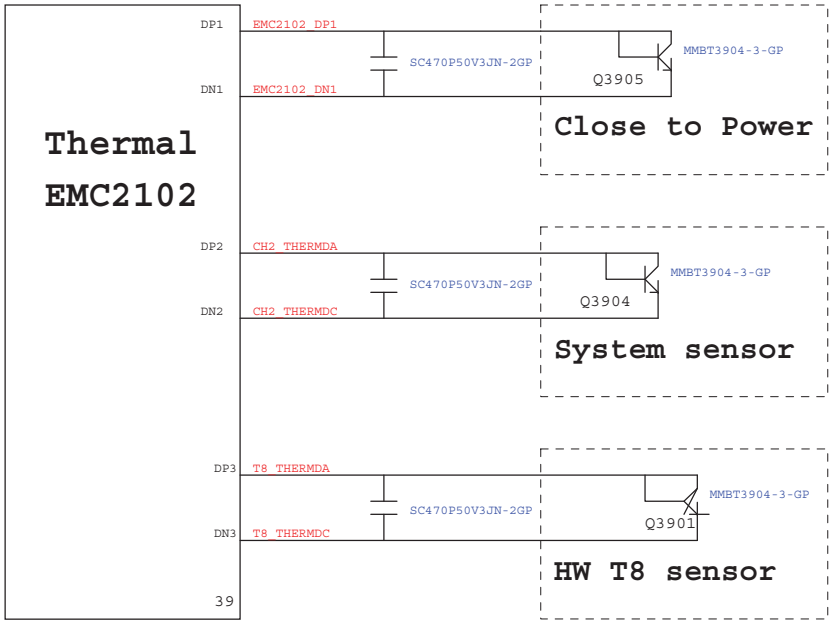
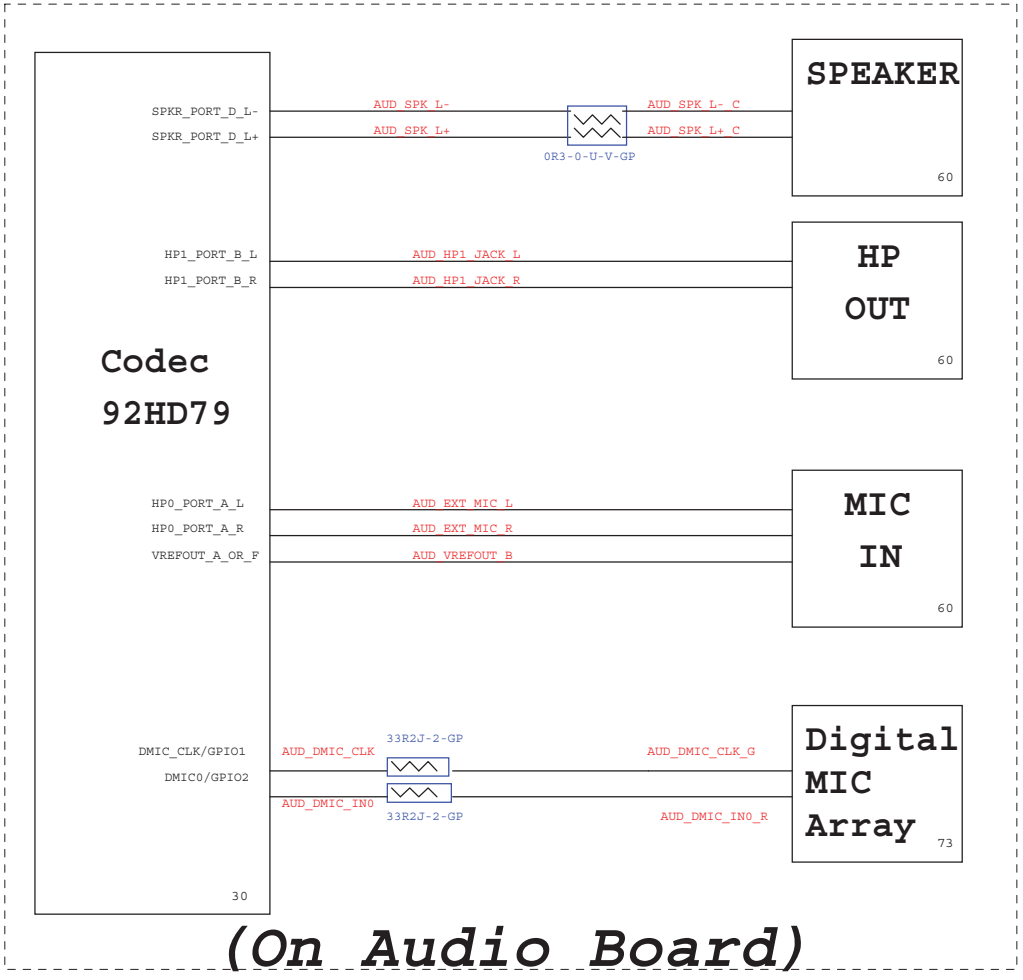
Thermal Block Diagram



Audio Block Diagram



(On Audio Board)

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Title	Thermal/Audio Block Diagram	
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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:** Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:** Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:** Leave floating (internal pull-down
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0)-** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1)-:** Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:** CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	**Low (0)-** Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **High (1)-:** Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality **Note:** This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default = Do not connect (floating). Internal pull-up.** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	1:Disabled - No Physical Di splay Port attached to Embedded DisplayPort 0:Enabled - An external DisplayPort device is connected to the Embedded DisplayPort	1
CFG[3]	**PCI-Express Static Lane Reversal**	1:Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1	1
CFG[0]	**PCI-Express Configuration Select**	1: Single PCI-Express Graphics 0: Bifurcation enabled	1

PCIE Routing

LANE1	RESERVE
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	RESERVE

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB for ESATA
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BlUETOOTH
9	Card Reader
10	RESERVED
11	CAMERA
12	RESERVED
13	RESERVED

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Title: Table of Content

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SSID = Clock GEN

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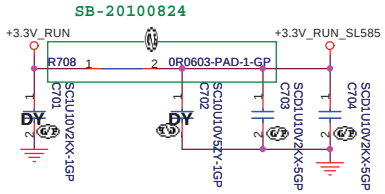

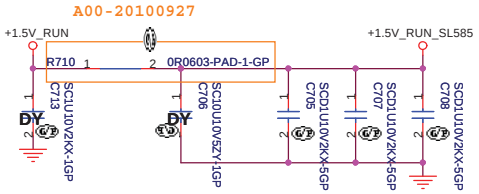

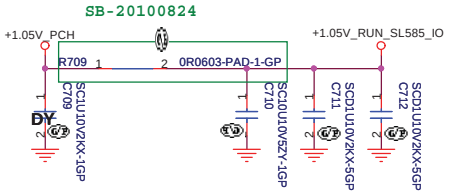

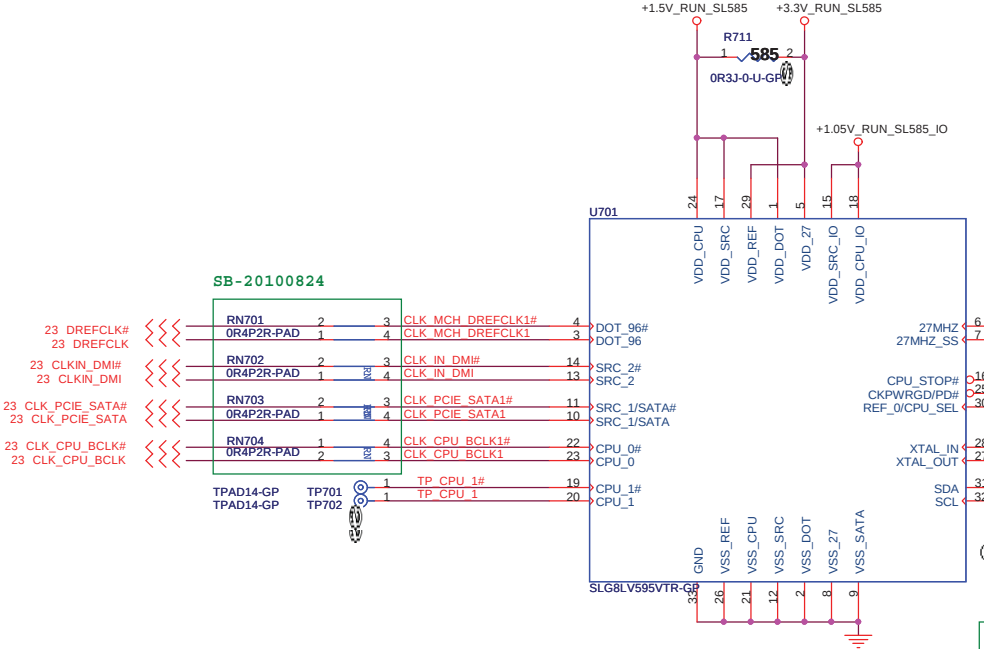

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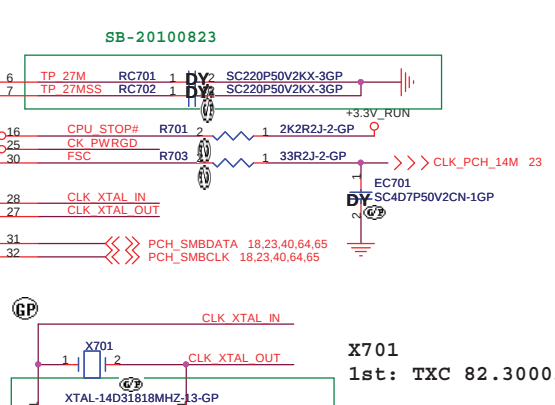
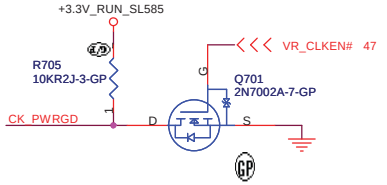
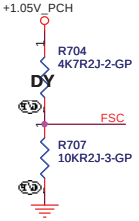
2nd ICS 71.93197.B03



X701
1st: TXC 82.30005.B81





FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator SLG8SP585

Size	Document Number	Rev
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SSID = CPU

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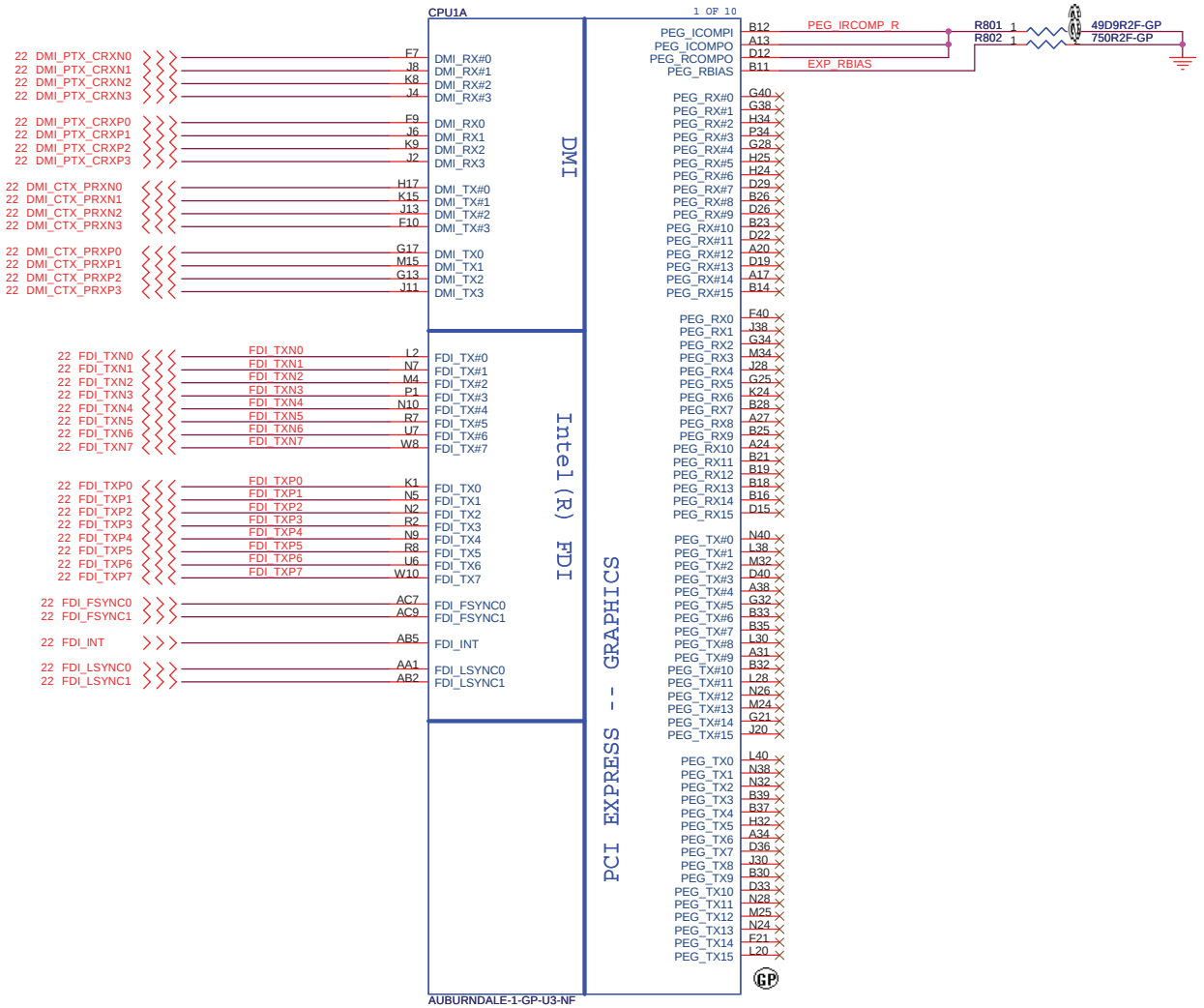

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Title: CPU (PCIE/DMI/FDI)-1/8

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SSID = CPU

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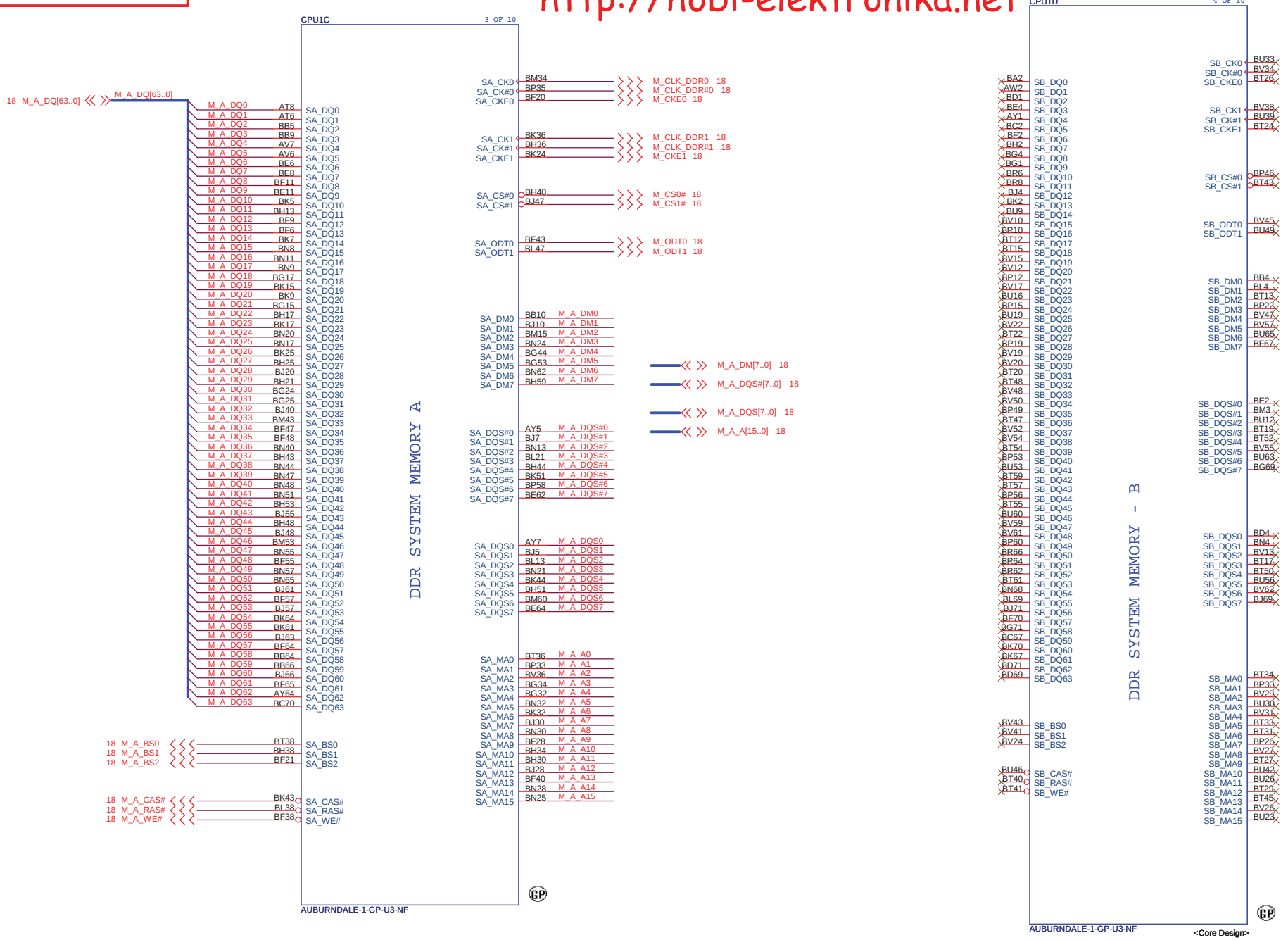

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Title: CPU (DDR)-2/8
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SSID = CPU

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Processor Pullups

Processor Compensation Signals

Misc

Clocks

Thermal

DDR3 Misc

Power Management

JTAG & MBP

SB-20100825

SB-20100824

SB-20100823

DDR3 Compensation Signals

Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details Revision 0.1

Normal

	R919	R920	R977
ARD	1.27k	3k	1.6k(DY)

S3 Power Reduction circuit

	R919	R920	R977
ARD	1.1k(DY)	0.75k	1.6k

XDP Connector

+1.05V_VCCP use Decoupling Capacitor close
ITP connector 100 mil (max)

CPU — TCK(PIN AN28) — XDP_Connector — TCK(PIN 57)

JTAG MAPPING

Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

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Title: CPU (THERMAL/CLOCK/PM)-3/8

Size | Document Number: RYU2 13 UMA | Rev: A00

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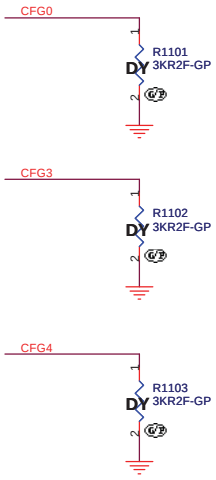
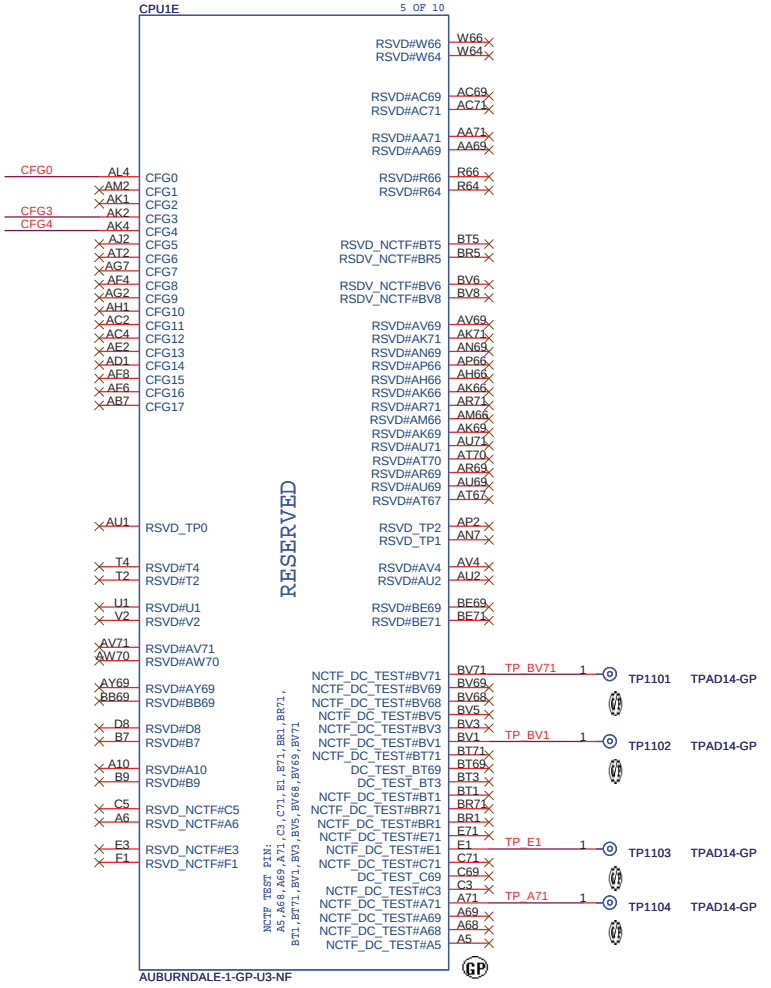


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Embedded DisplayPort Presence	
CFG4	1:Disabled - No Physical Di splay Port attached to Embedded DisplayPort 0:Enabled - An external DisplayPort device is connected to the Embedded DisplayPort



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Title		
CPU (RESERVED)-4/8		
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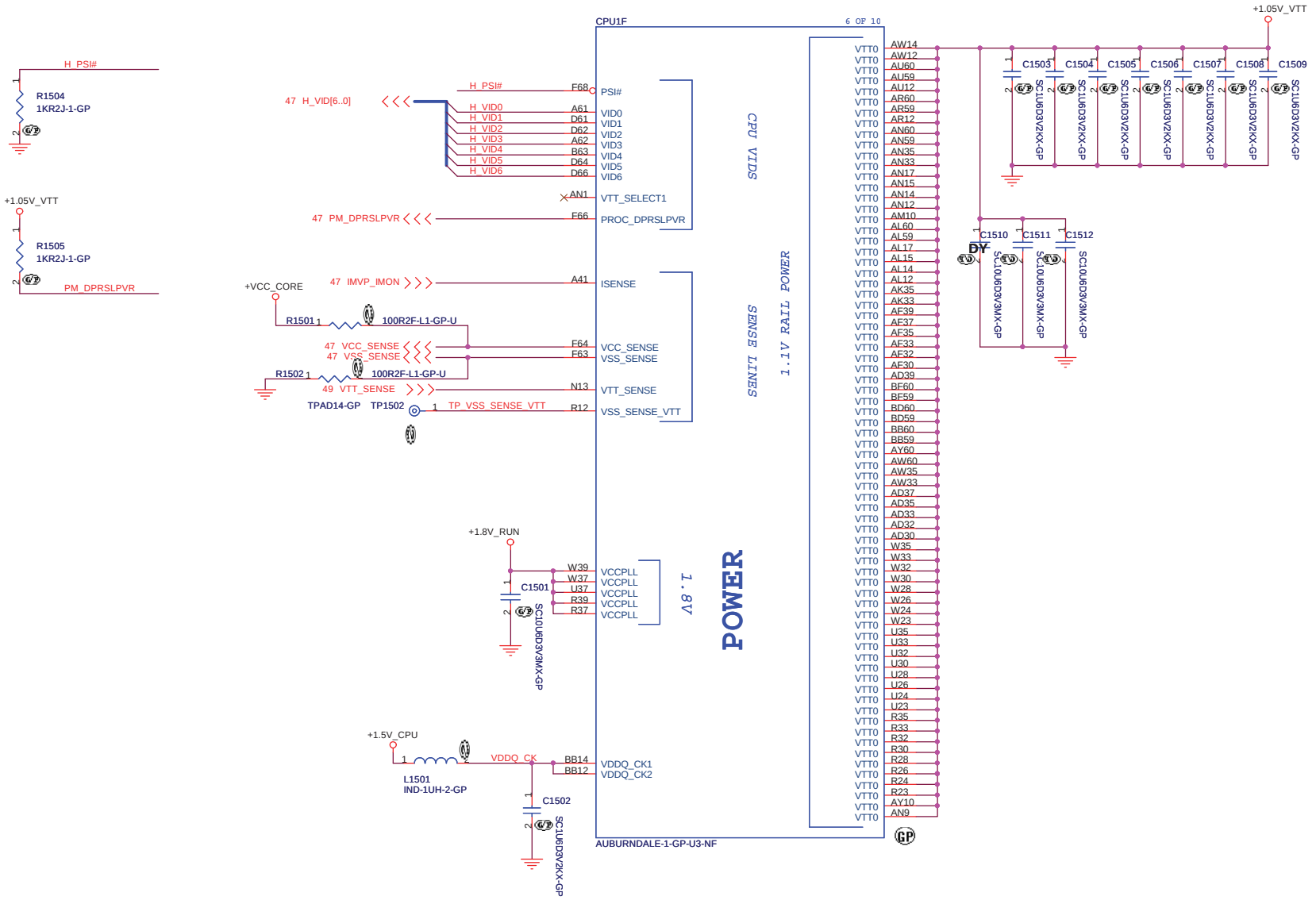

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Title	CPU SFF PWR/VTT-5/8	
Size A3	Document Number RYU2 13 UMA	Rev A00
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SSID = CPU

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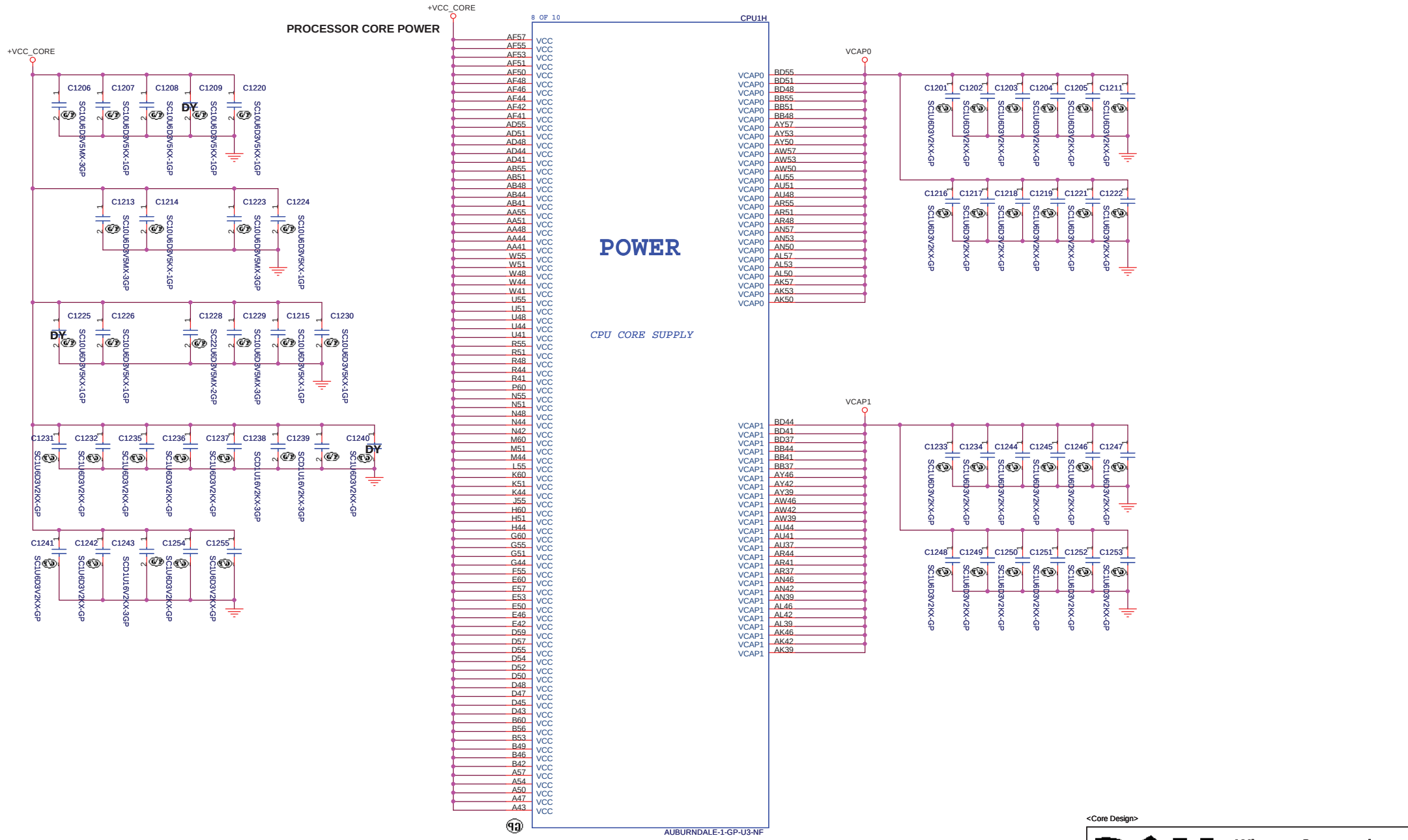

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Title: CPU (VCC_CORE)-6/8

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SSID = CPU

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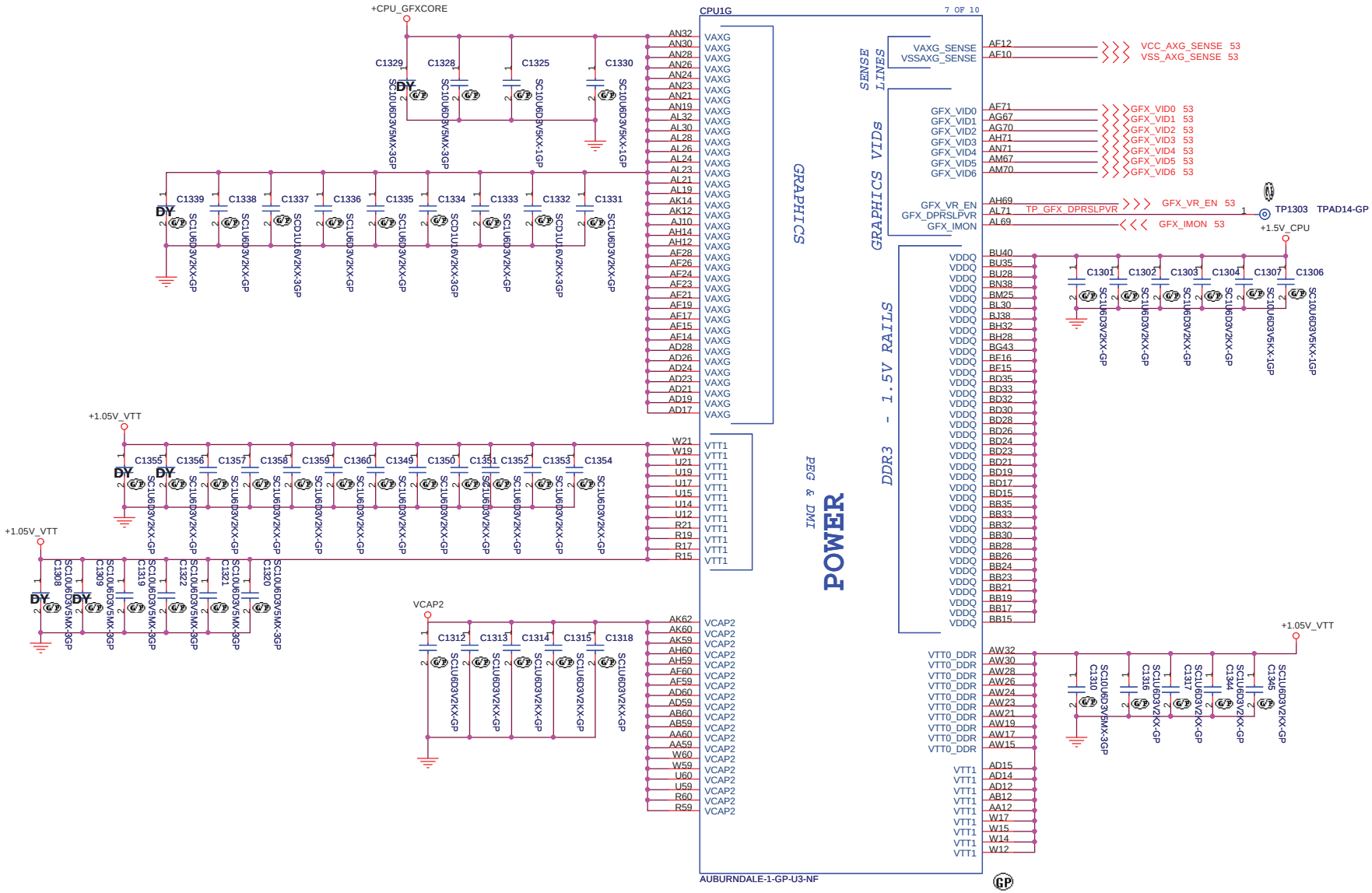

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Title	CPU (VCC_GFXCORE)-7/8	
Size	Document Number: RYU2 13 UMA	Rev: A00
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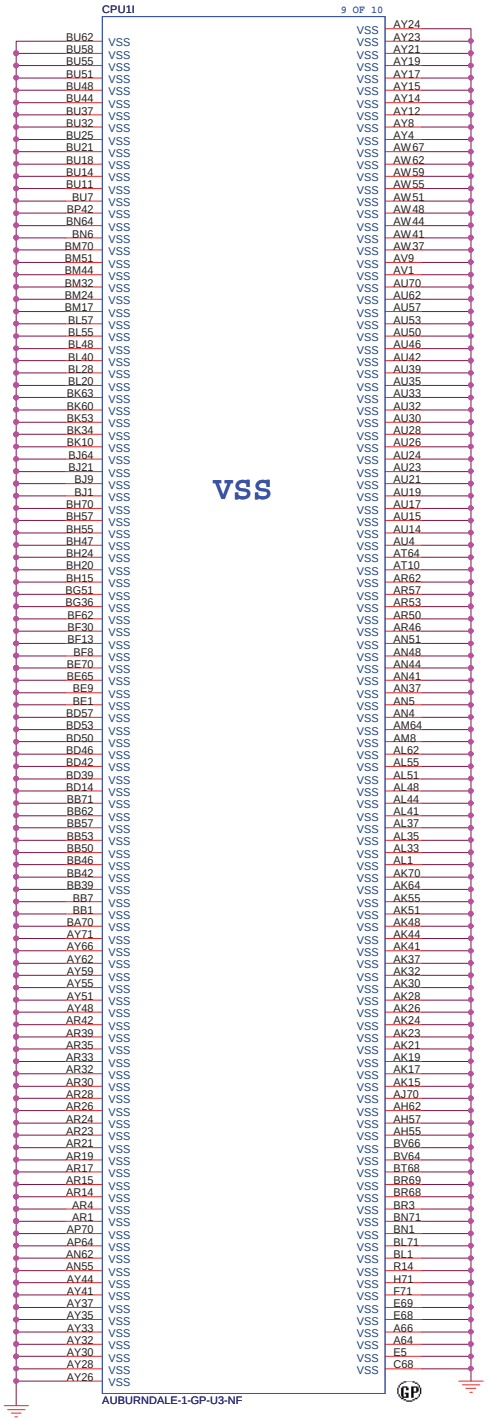

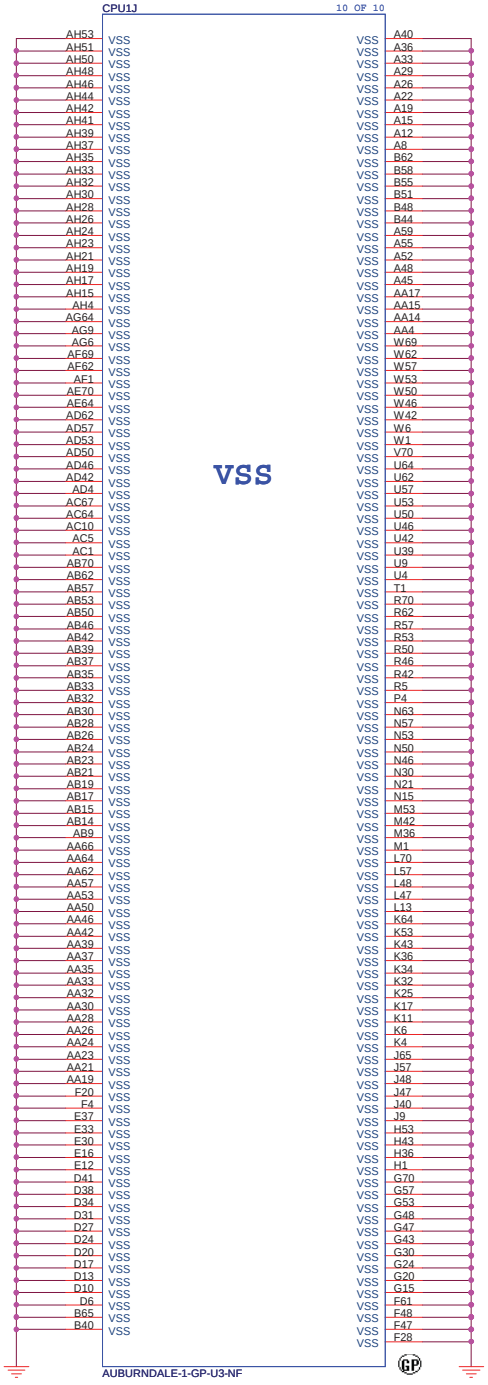

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Title: CPU (VSS)-8/8

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Title

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Title

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SSID = MEMORY

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9 M_A_DQS#[7..0]
9 M_A_DQ[63..0]
9 M_A_DM[7..0]
9 M_A_DQS[7..0]
9 M_A_A[15..0]

Layout Note:
Place near DM1

+1.5V_SUS

C1803 SC10U6D3V5KX-1GP
C1804 SC10U6D3V5KX-1GP
C1812 SC22U6D3V5MX-2GP
C1802 SC10U6D3V5MX-3GP
C1811 SC22U6D3V5MX-2GP
C1816 SC22U6D3V5MX-2GP
EC1801 SCD1U50V3KX-GP
TC1803 ST330U2D5VBM-1-GP
DY

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT

C1801 SC1U6D3V2KX-GP
C1813 SC1U6D3V2KX-GP
C1814 SC1U6D3V2KX-GP
C1815 SC1U6D3V2KX-GP
C1823 SC10U6D3V5MX-3GP

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9. pdf" document.

+1.5V_SUS

C1872 SCD1U16V2KX-3GP
C1873 SCD1U16V2KX-3GP
C1874 SCD1U16V2KX-3GP
C1875 SCD1U16V2KX-3GP

+V_DDR_REF

C1810 SCD1U10V2KX-5GP
C1809 SC2D2U6D3V3KX-GP

+V_DDR_REF

C1817 SCD1U10V2KX-5GP
C1805 SC2D2U6D3V3KX-GP

+0.75V_DDR_VTT

10 DDR3_DRAMRST#

DM1

M_A_A0	97	A0	
M_A_A1	96	A1	
M_A_A2	95	A2	
M_A_A3	92	A3	
M_A_A4	91	A4	
M_A_A5	90	A5	
M_A_A6	86	A6	
M_A_A7	89	A7	
M_A_A8	85	A8	
M_A_A9	107	A9	
M_A_A10	84	A10/AP	
M_A_A11	83	A11	
M_A_A12	119	A12	
M_A_A13	80	A13	
M_A_A14	78	A14	
M_A_A15	79	A15	
9 M_A_BS2		A16/BA2	
M_A_BS0	109	BA0	
M_A_BS1	108	BA1	
M_A_DQ0	5	DQ0	
M_A_DQ1	7	DQ1	
M_A_DQ2	15	DQ2	
M_A_DQ3	17	DQ3	
M_A_DQ4	4	DQ4	
M_A_DQ5	6	DQ5	
M_A_DQ6	16	DQ6	
M_A_DQ7	18	DQ7	
M_A_DQ8	21	DQ8	
M_A_DQ9	23	DQ9	
M_A_DQ10	33	DQ10	
M_A_DQ11	35	DQ11	
M_A_DQ12	22	DQ12	
M_A_DQ13	24	DQ13	
M_A_DQ14	34	DQ14	
M_A_DQ15	36	DQ15	
M_A_DQ16	39	DQ16	
M_A_DQ17	41	DQ17	
M_A_DQ18	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ20	40	DQ20	
M_A_DQ21	42	DQ21	
M_A_DQ22	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ24	57	DQ24	
M_A_DQ25	59	DQ25	
M_A_DQ26	67	DQ26	
M_A_DQ27	69	DQ27	
M_A_DQ28	56	DQ28	
M_A_DQ29	58	DQ29	
M_A_DQ30	68	DQ30	
M_A_DQ31	70	DQ31	
M_A_DQ32	129	DQ32	
M_A_DQ33	131	DQ33	
M_A_DQ34	141	DQ34	
M_A_DQ35	143	DQ35	
M_A_DQ36	130	DQ36	
M_A_DQ37	132	DQ37	
M_A_DQ38	140	DQ38	
M_A_DQ39	142	DQ39	
M_A_DQ40	147	DQ40	
M_A_DQ41	149	DQ41	
M_A_DQ42	157	DQ42	
M_A_DQ43	159	DQ43	
M_A_DQ44	146	DQ44	
M_A_DQ45	148	DQ45	
M_A_DQ46	158	DQ46	
M_A_DQ47	160	DQ47	
M_A_DQ48	163	DQ48	
M_A_DQ49	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ51	177	DQ51	
M_A_DQ52	164	DQ52	
M_A_DQ53	166	DQ53	
M_A_DQ54	174	DQ54	
M_A_DQ55	176	DQ55	
M_A_DQ56	181	DQ56	
M_A_DQ57	183	DQ57	
M_A_DQ58	191	DQ58	
M_A_DQ59	193	DQ59	
M_A_DQ60	180	DQ60	
M_A_DQ61	182	DQ61	
M_A_DQ62	192	DQ62	
M_A_DQ63	194	DQ63	
M_A_DQS#0	10	DQS0#	
M_A_DQS#1	27	DQS1#	
M_A_DQS#2	45	DQS2#	
M_A_DQS#3	62	DQS3#	
M_A_DQS#4	135	DQS4#	
M_A_DQS#5	152	DQS5#	
M_A_DQS#6	169	DQS6#	
M_A_DQS#7	186	DQS7#	
M_A_DQS0	12	DQS0	
M_A_DQS1	29	DQS1	
M_A_DQS2	47	DQS2	
M_A_DQS3	64	DQS3	
M_A_DQS4	137	DQS4	
M_A_DQS5	154	DQS5	
M_A_DQS6	171	DQS6	
M_A_DQS7	188	DQS7	
9 M_ODT0	116	ODT0	
9 M_ODT1	120	ODT1	
	126	VREF_CA	
	1	VREF_DQ	
	30	RESET#	
	203	VTT1	
	204	VTT2	

NC#1	NP1	
NC#2	NP2	
RAS#	110	M_A_RAS# 9
WE#	113	M_A_WE# 9
CAS#	115	M_A_CAS# 9
CS0#	114	M_CS0# 9
CS1#	121	M_CS1# 9
CKE0	73	M_CKE0 9
CKE1	74	M_CKE1 9
CK0	101	M_CLK_DDR0 9
CK0#	103	M_CLK_DDR#0 9
CK1	102	M_CLK_DDR1 9
CK1#	104	M_CLK_DDR#1 9
DM0	11	M_A_DM0
DM1	28	M_A_DM1
DM2	46	M_A_DM2
DM3	63	M_A_DM3
DM4	136	M_A_DM4
DM5	153	M_A_DM5
DM6	170	M_A_DM6
DM7	187	M_A_DM7
SDA	200	PCH_SMBDATA 7,23,40,64,65
SCL	202	PCH_SMBCLK 7,23,40,64,65
EVENT#	198	
VDDSPD	199	
SA0	197	SA0_DM1
SA1	201	SA1_DM1
NC#1	77	
NC#2	122	
NC#/TEST	125	
VDD1	75	
VDD2	76	
VDD3	81	
VDD4	82	
VDD5	87	
VDD6	88	
VDD7	93	
VDD8	94	
VDD9	99	
VDD10	100	
VDD11	105	
VDD12	106	
VDD13	111	
VDD14	112	
VDD15	117	
VDD16	118	
VDD17	123	
VDD18	124	
VSS	2	
VSS	3	
VSS	8	
VSS	9	
VSS	13	
VSS	14	
VSS	19	
VSS	20	
VSS	25	
VSS	26	
VSS	31	
VSS	32	
VSS	37	
VSS	38	
VSS	43	
VSS	44	
VSS	48	
VSS	49	
VSS	54	
VSS	55	
VSS	60	
VSS	61	
VSS	65	
VSS	66	
VSS	71	
VSS	72	
VSS	127	
VSS	128	
VSS	133	
VSS	134	
VSS	138	
VSS	139	
VSS	144	
VSS	145	
VSS	150	
VSS	151	
VSS	155	
VSS	156	
VSS	161	
VSS	162	
VSS	167	
VSS	168	
VSS	172	
VSS	173	
VSS	178	
VSS	179	
VSS	184	
VSS	185	
VSS	189	
VSS	190	
VSS	195	
VSS	196	
VSS	205	
VSS	206	

DDR3-204P-99-GP-U
62.10017.W01

SA0_DM1
SA1_DM1

R1802 10KR2J-3-GP
R1801 10KR2J-3-GP

SMBUS address:A0

+3.3V_RUN

C1806 SCD1U10V2KX-5GP
C1807 SC2D2U6D3V3KX-GP
DY

+1.5V_SUS

put near connector

M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1

C1821 DUMMY-C2
C1819 DUMMY-C2
C1820 DUMMY-C2
C1818 DUMMY-C2

<Core Design>

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Title: DDRIII-SODIMM SLOT1
Size: Custom
Document Number: RYU2 13 UMA
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Title

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Size	Document Number	Rev
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SSID = PCH

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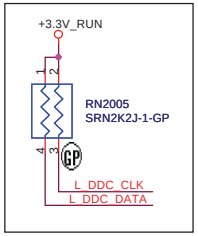
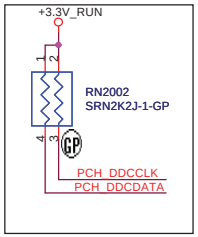
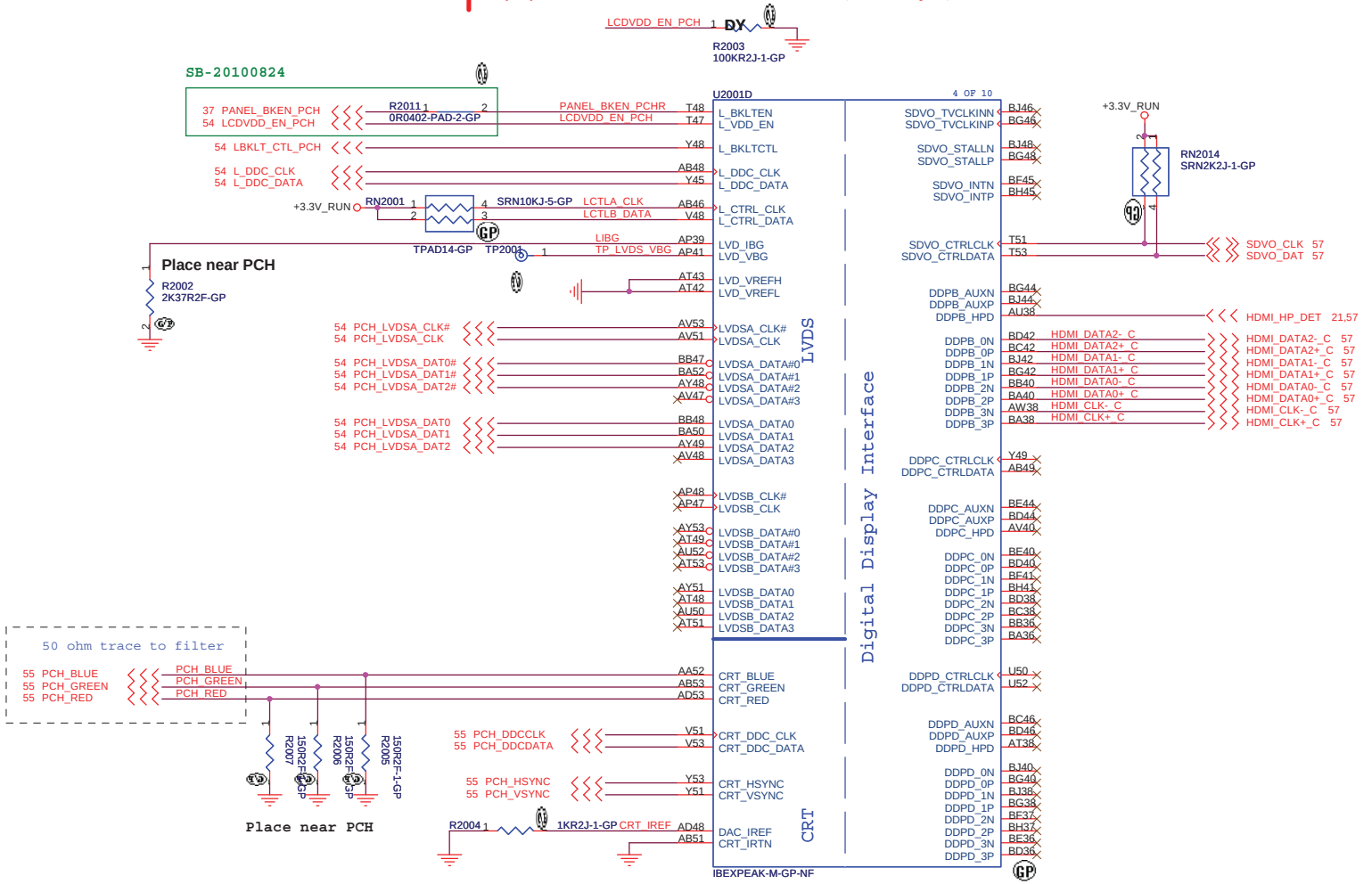
LVDS SMBUS
Close PCH



CRT SMBUS
Close PCH





<Core Design>

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Title: PCH (LVDS/CRT/DDI)

Size | Document Number: RYU2 13 UMA | Rev: A00

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SSID = PCH

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BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high. Low = Default

unused NV_SLE strap

USB	
Pair	Device
0	USB1 debug port
1	USB2
2	USB for ESATA
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Card Reader
10	RESERVED
11	CAMERA
12	RESERVED
13	RESERVED

Calpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

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Title: PCH (PCI/USB/NVRAM)

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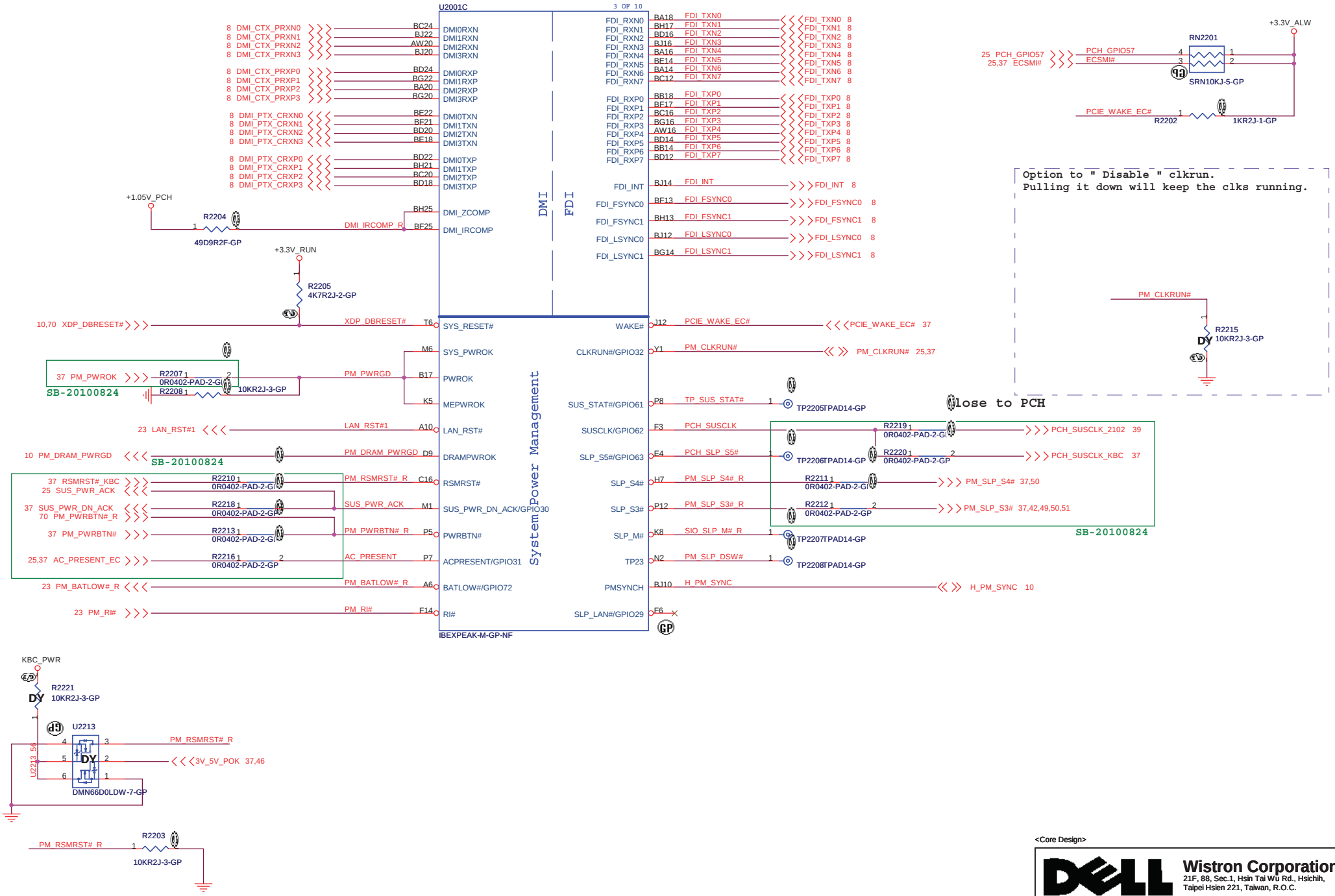

<Core Design>

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Title	PCH (DM I/FDI/PM)	
Size	Document Number: RYU2 13 UMA	Rev: A00
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SSID = PCH

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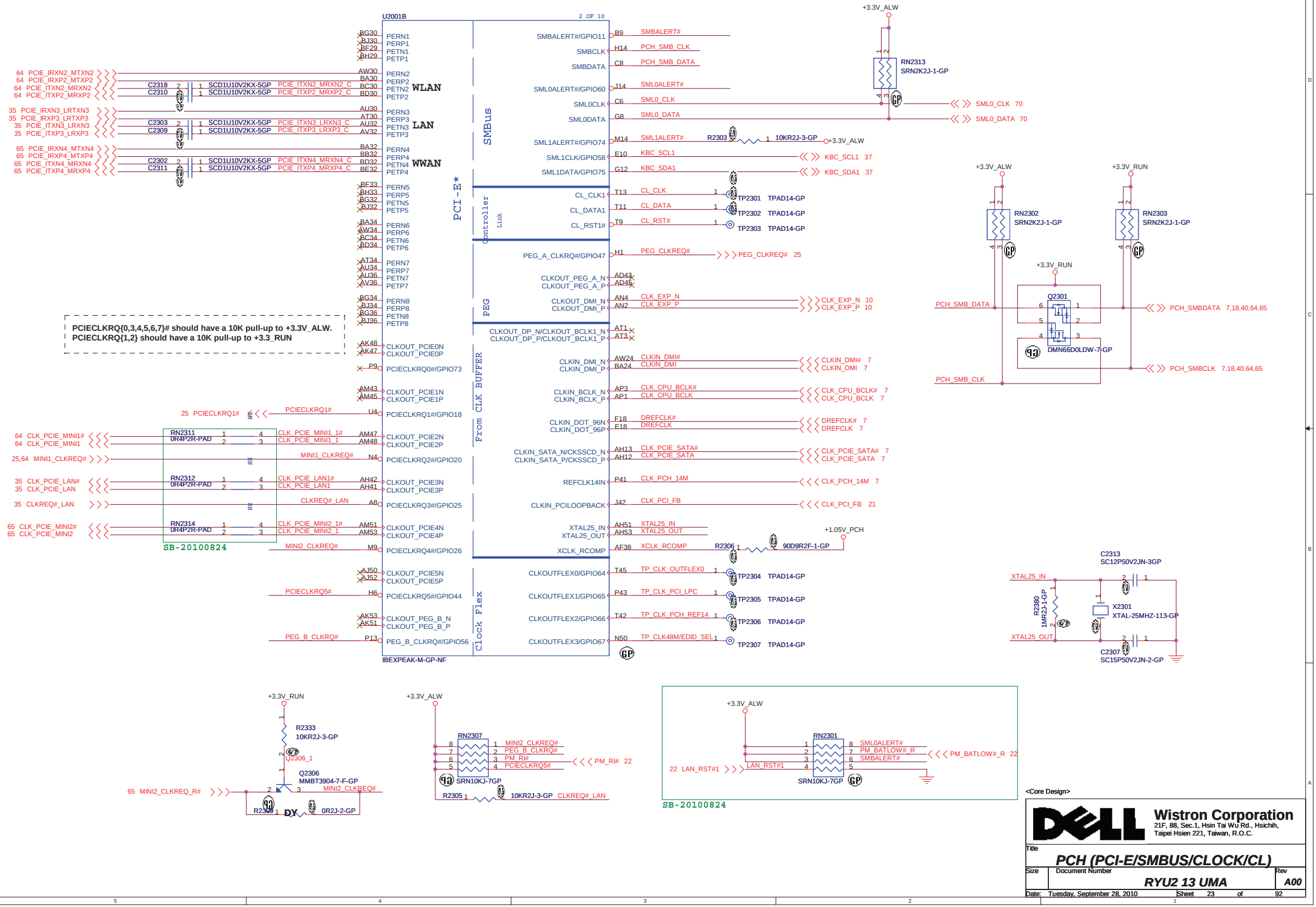

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<core_design>

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: RYU2 13 UMA | Rev: A00

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SSID = PCH

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INTVRMEN: Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

Flash Descriptor Security Override/ ME Debug Mode	
ME_UNLOCK#	This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

U2001A

HDD

ESATA

IBEXPEAK-M-GP-NF

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)

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SSID = PCH

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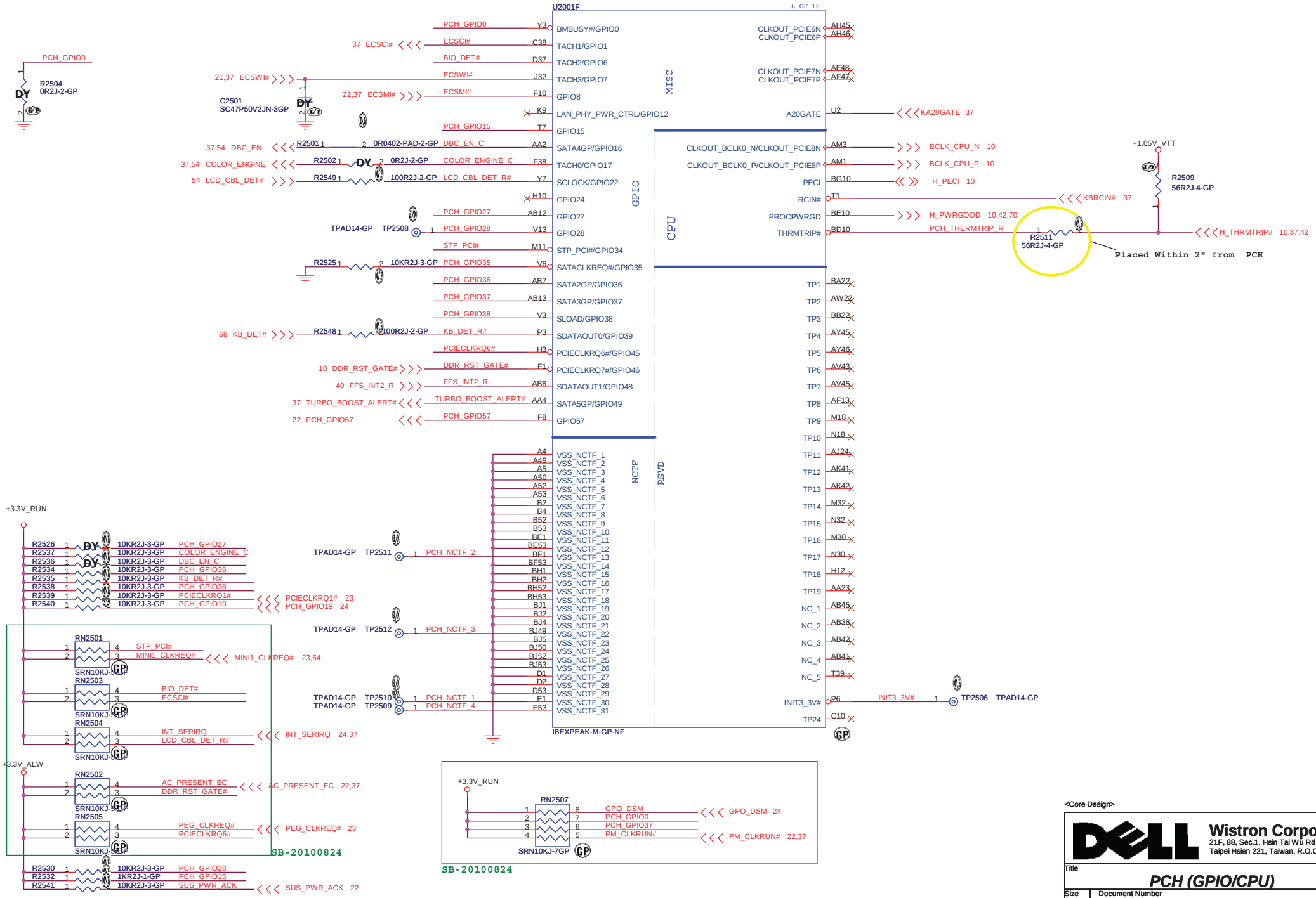

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

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SSID = PCH

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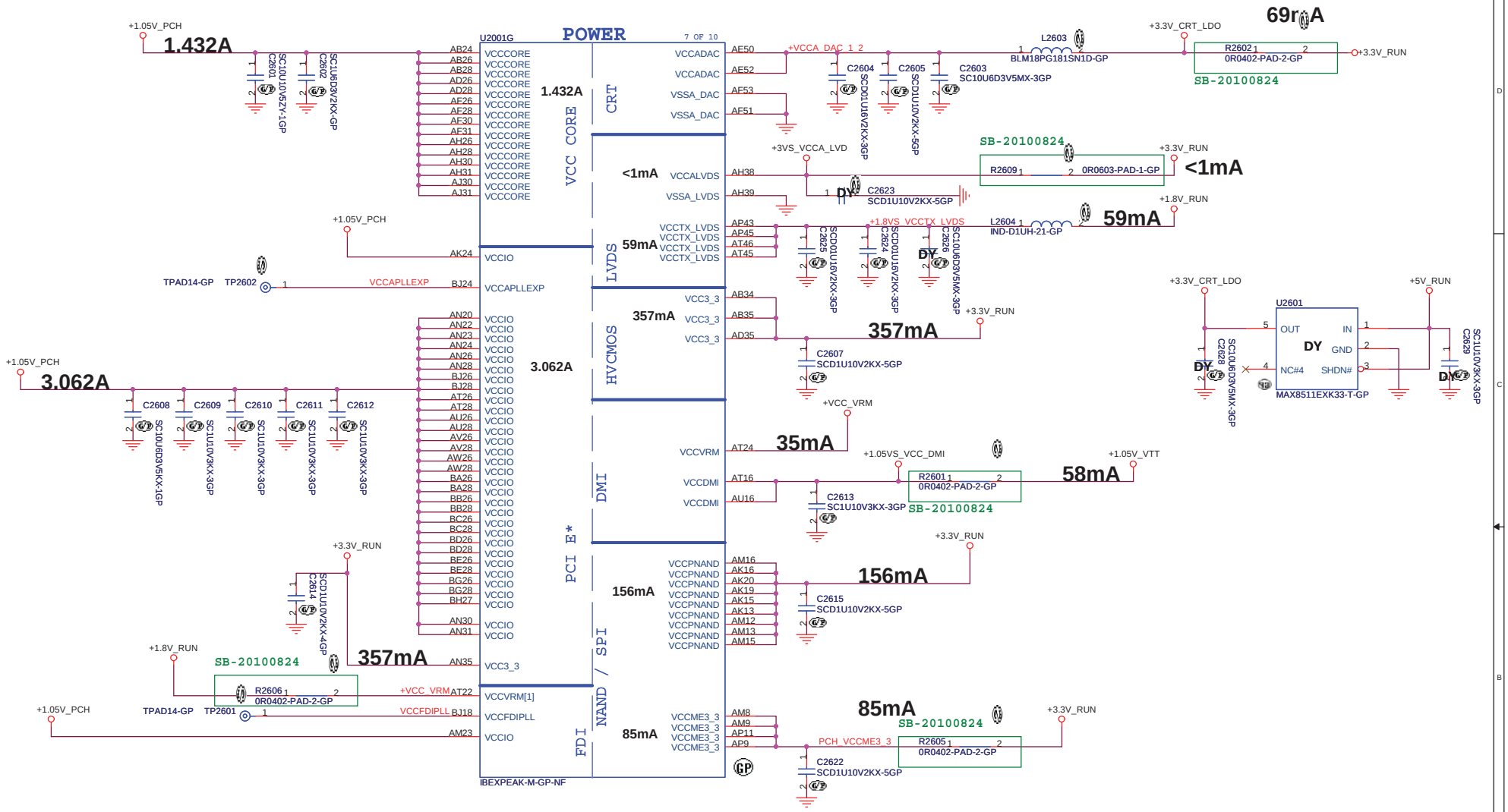

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Title	PCH (POWER1)	
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SSID = PCH

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U2001J POWER 10 OF 10

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | RTC | HDA

TPAD14-GP TP2701 VCCACLK

1.849A

+1.05V_PCH

+3.3V_ALW

+3.3V_RUN

+5V_ALW

+5V_RUN

+1.05VS_VCCA_A_DPL

+1.05VS_VCCA_B_DPL

+VCCRTCEXT

+VCC_VRM

+VCCSST

+1.05VALW_INT_VCCSUS

+1.05V_VTT

+RTC_CELL

+3VS_+1.5VS_HDA_IO

+5VALW_PCH_VCC5REFSUS

+5VS_PCH_VCC5REF

VCCSATAPLL

IBEXPEAK-M-GP-NF

<Core Design>

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Title: PCH (POWER2)

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SSID = PCH

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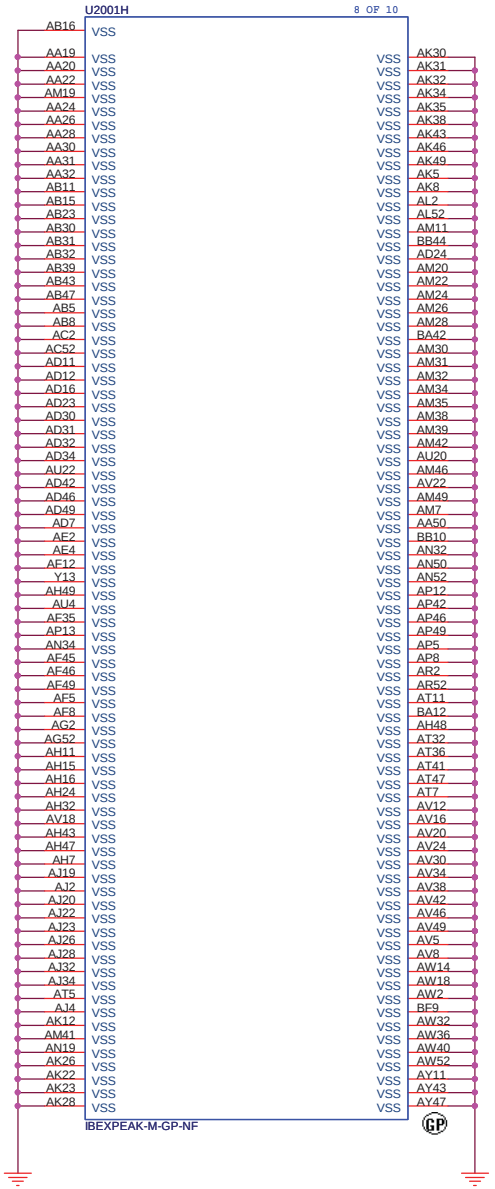

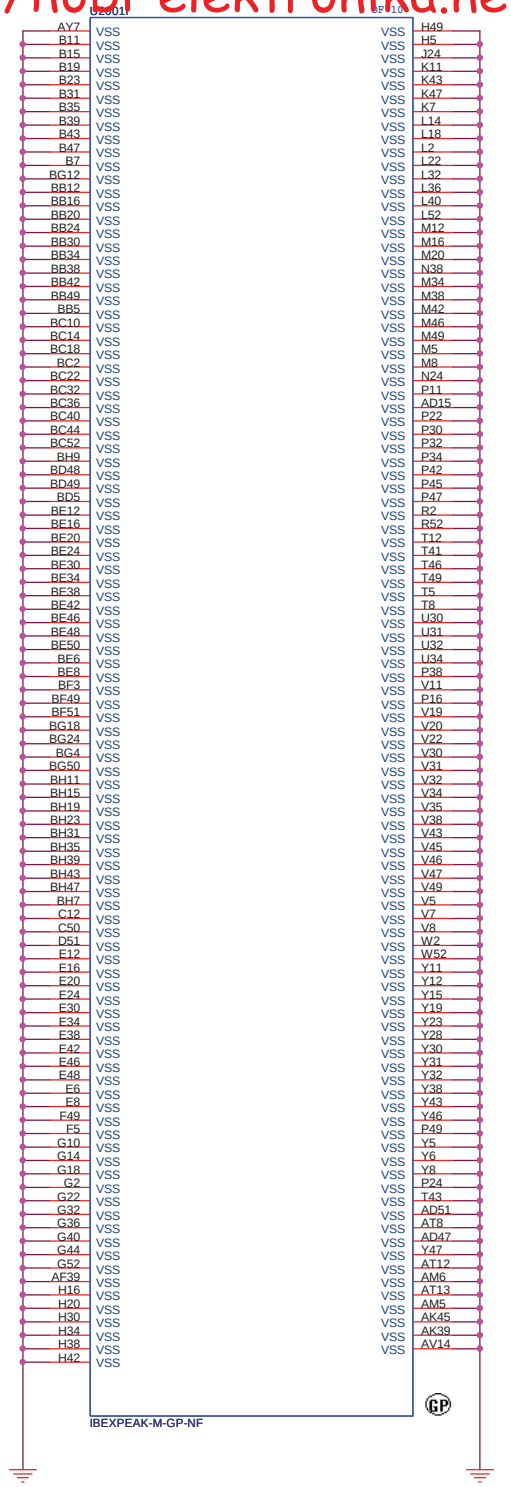

<Core Design>

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Title	PCH (VSS)	
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Title

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Title

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<Core Design>

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Title

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SSID = LOM

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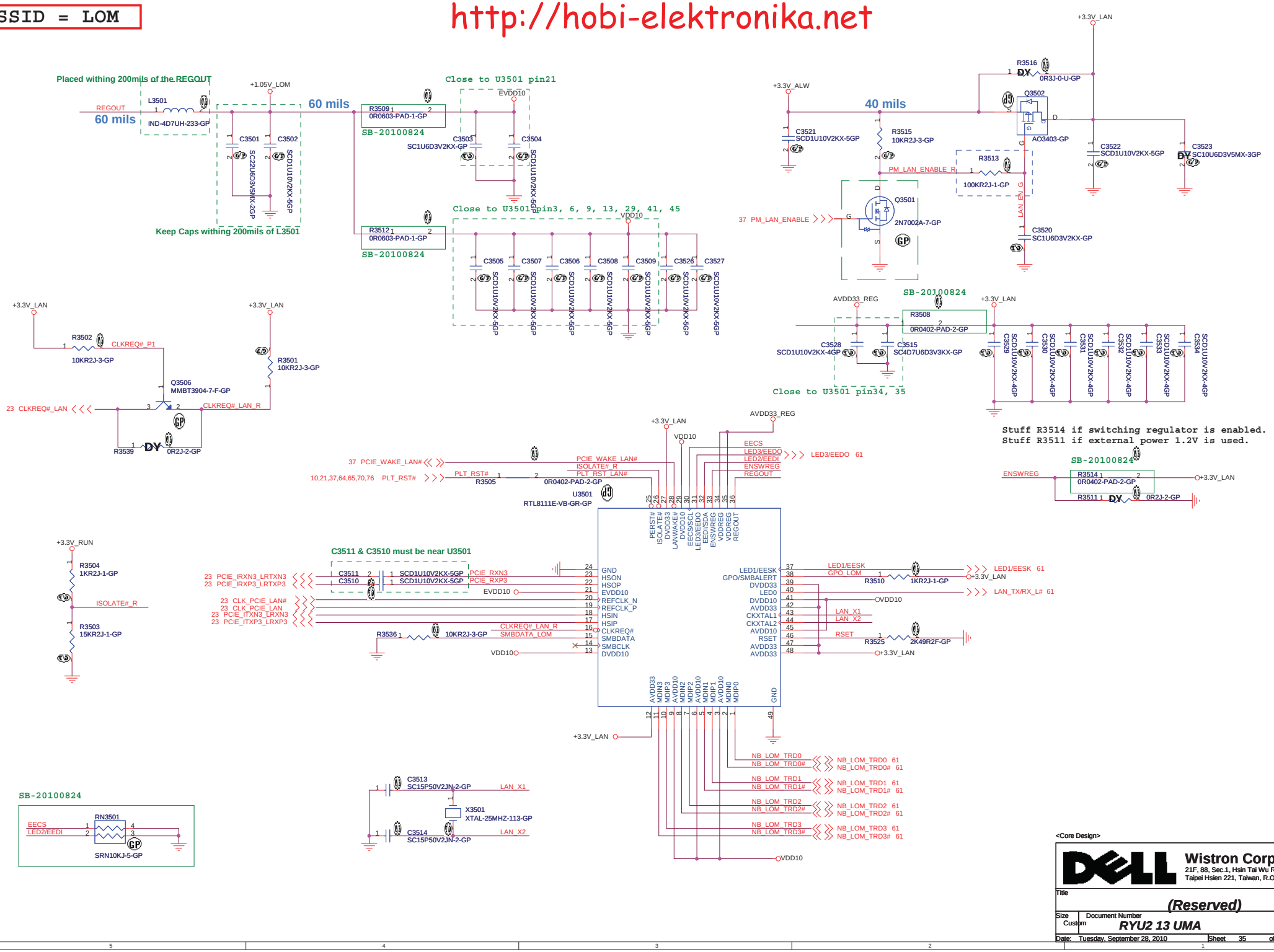

<Core Design>

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Title: (Reserved)

Size	Document Number	Rev
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<Core Design>

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Title
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SSID = KBC

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Put 0.1uF close to VCC-GND pin pair.

Pull High : Discrete
internal Pull Low for UMA

C3710 need place near pin 44.

MB VERSION ID	VER1	VER0
SA	0	0
SB	0	1
SC	1	0
-1	1	1

KBC CLK EMI

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: Custom | Document Number: RYU2 13 UMA | Rev: A00

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Title

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SSID = Thermal

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25mil

25mil

1. CPU CORE POWER

Q3905 must be near CPU Core Power

C3912 must be near Q3905

C3914 must be near EMC2102

Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. System Sensor

C3913 must be near Q3904

C3906 must be near EMC2102

Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.

C3901 must be near Q3901

C3903 must be near EMC2102

3.HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

SB-20100824

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is set 88 deg-C.

32K suspend clock output

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

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SSID = User.Interface

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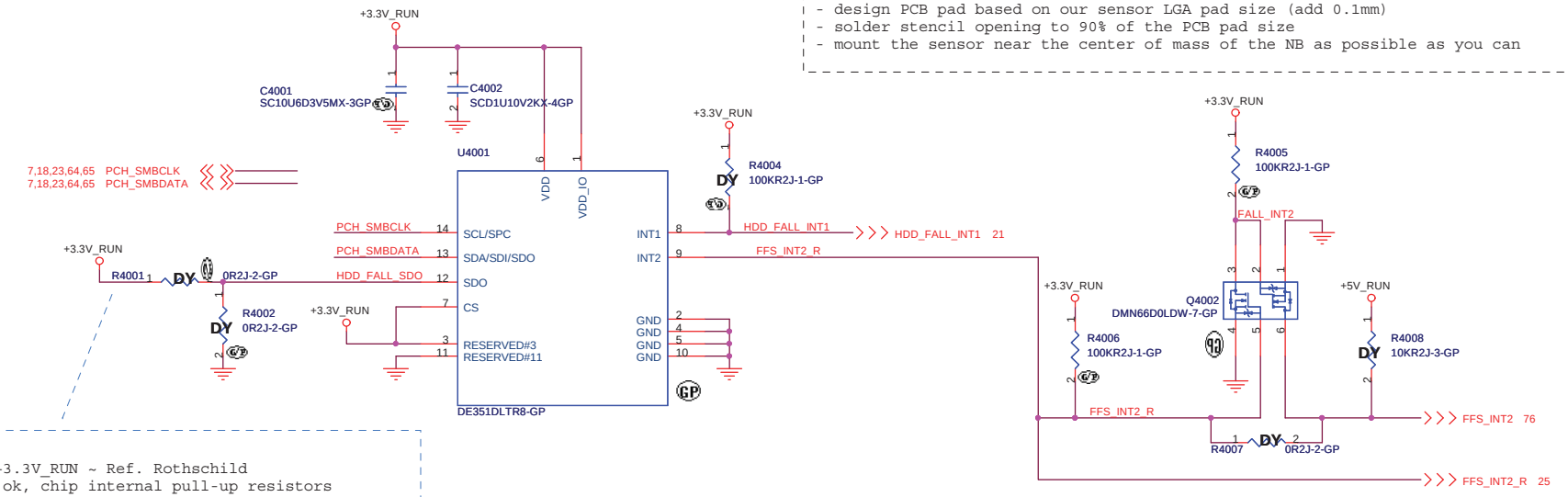
Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title	Free Fall Sensor	
Size A3	Document Number RYU2 13 UMA	Rev A00
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<Core Design>

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Title

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SSID = Reset.Suspend

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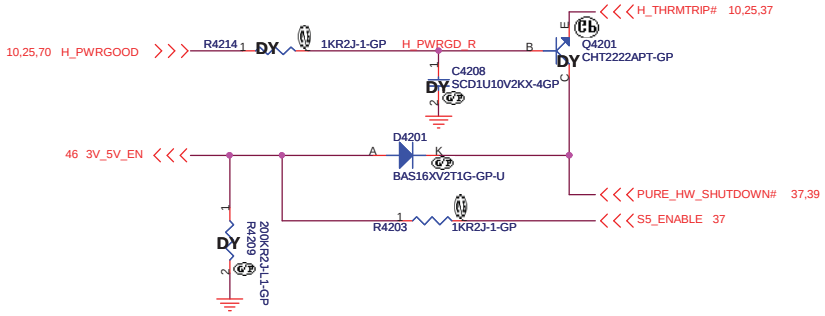

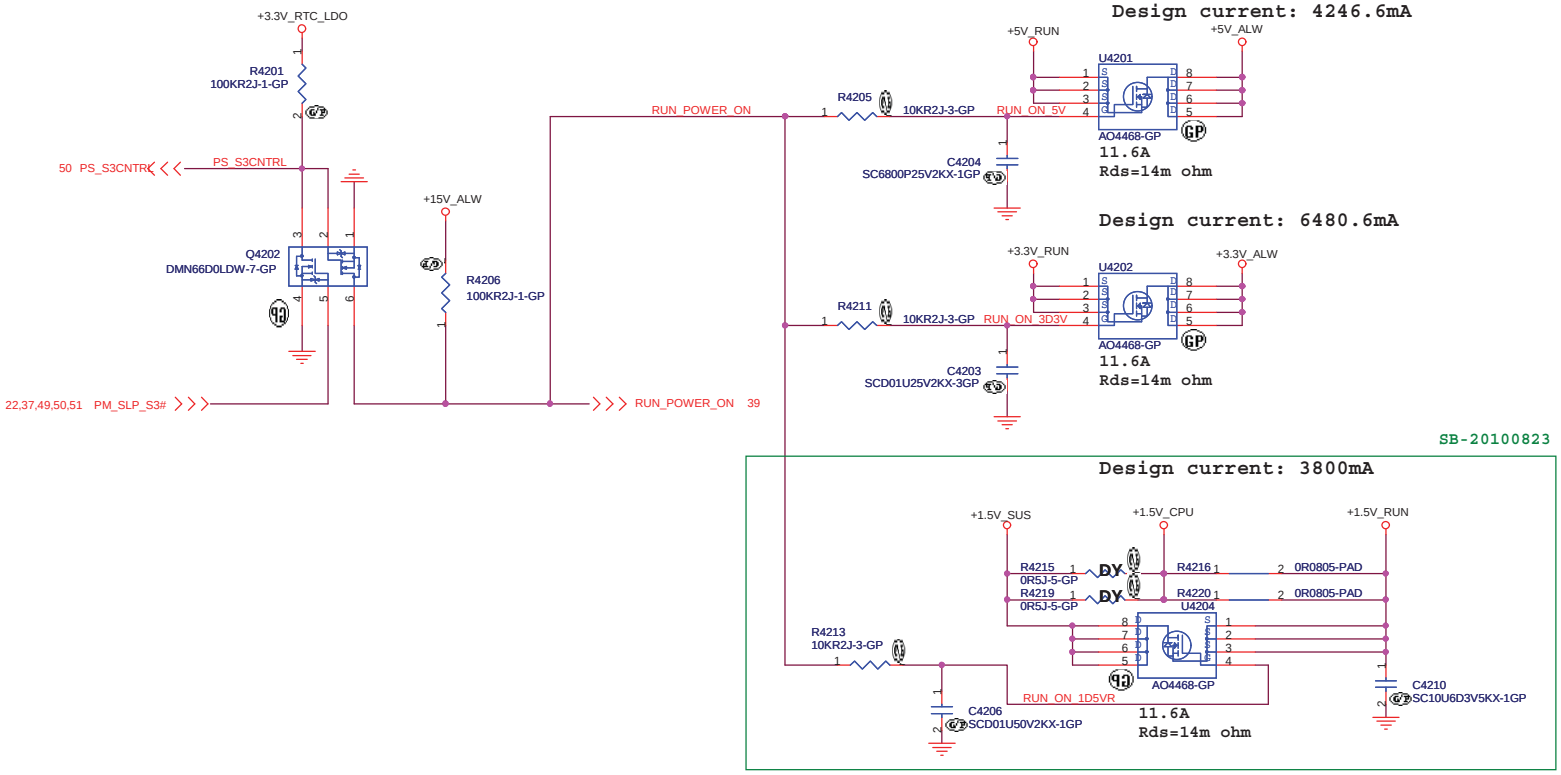

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: Custom | Document Number: RYU2 13 UMA | Rev: A00

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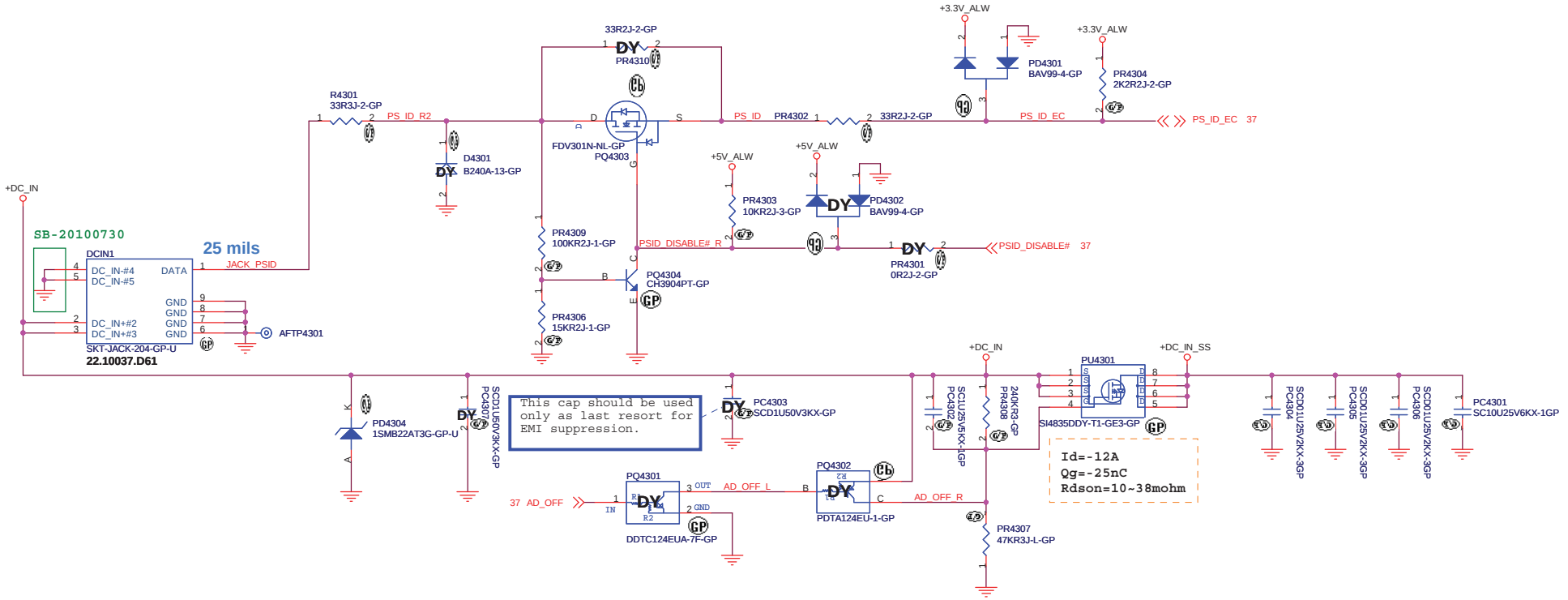
SSID = DCIN

http://hobi-elektronika.net



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	DCIN	
Size: Custom	Document Number: RYU2 13 UMA	Rev: A00
Date: Tuesday, September 28, 2010	Sheet 43 of 92	

SSID = BATT

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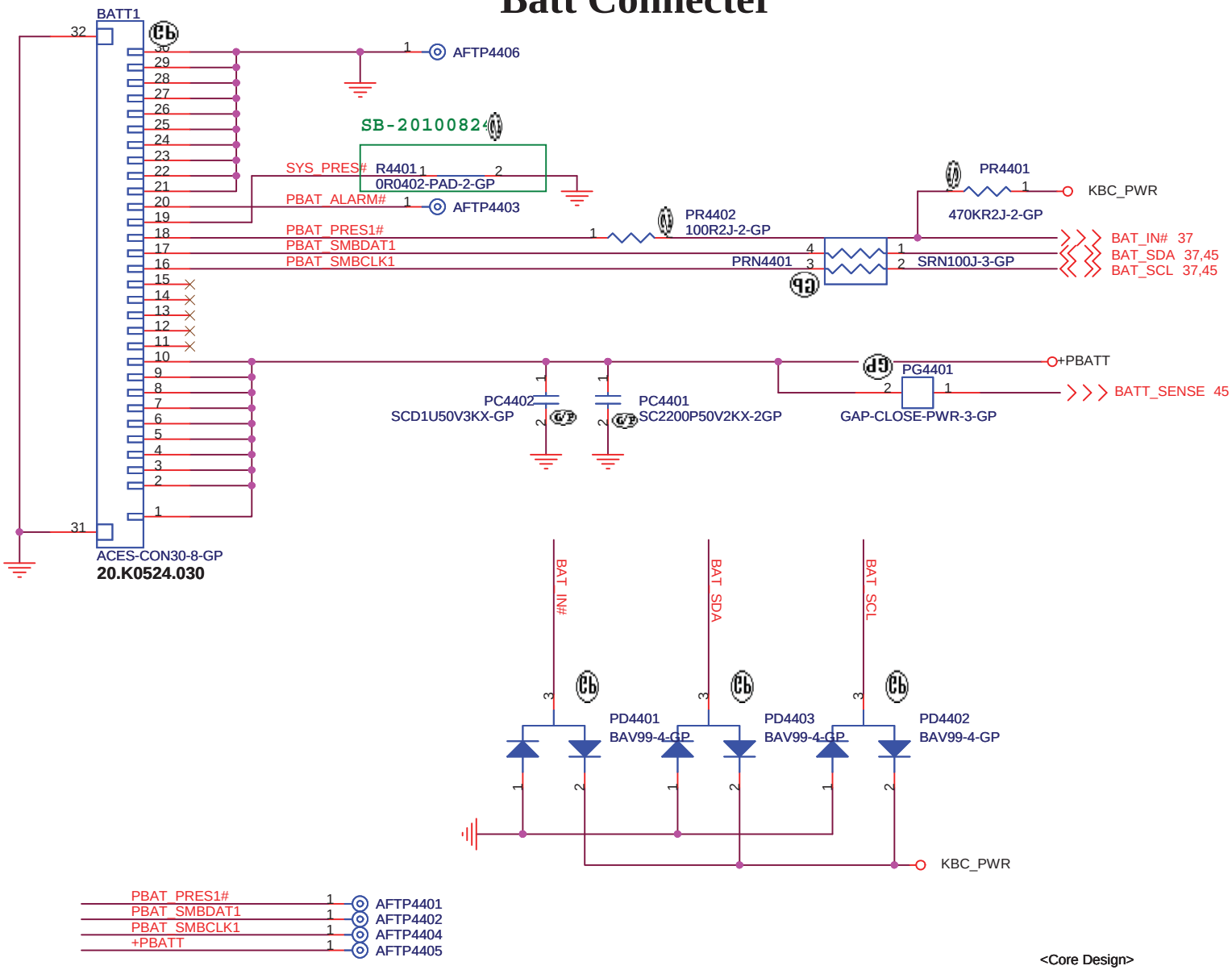
Batt Connecter



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Batt Connecter*		
Size: A4	Document Number: *RYU2 13 UMA*	Rev: *A00*
Date: Tuesday, September 28, 2010	Sheet 44 of 92	

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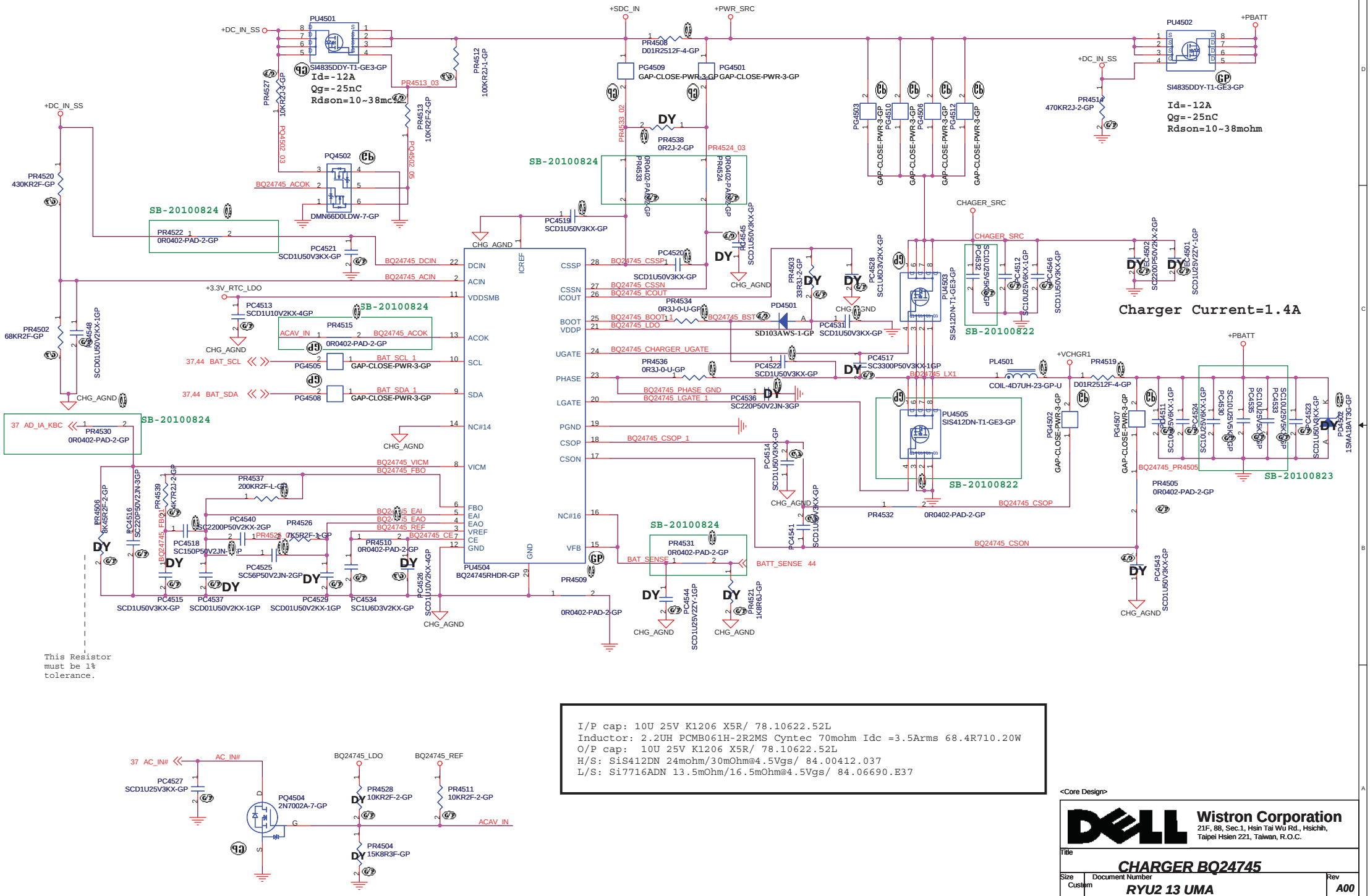
SSID = Charger



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMB061H-2R2MS Cyntec 70mohm Idc =3.5Arms 68.4R710.20W
O/P cap: 10U 25V K1206 X5R/ 78.10622.52L
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745
Size: Custom | Document Number: RYU2 13 UMA | Rev: A00
Date: Tuesday, September 28, 2010 | Sheet 45 of 92

SSID = PWR.Plane.Regulator_3V/5V

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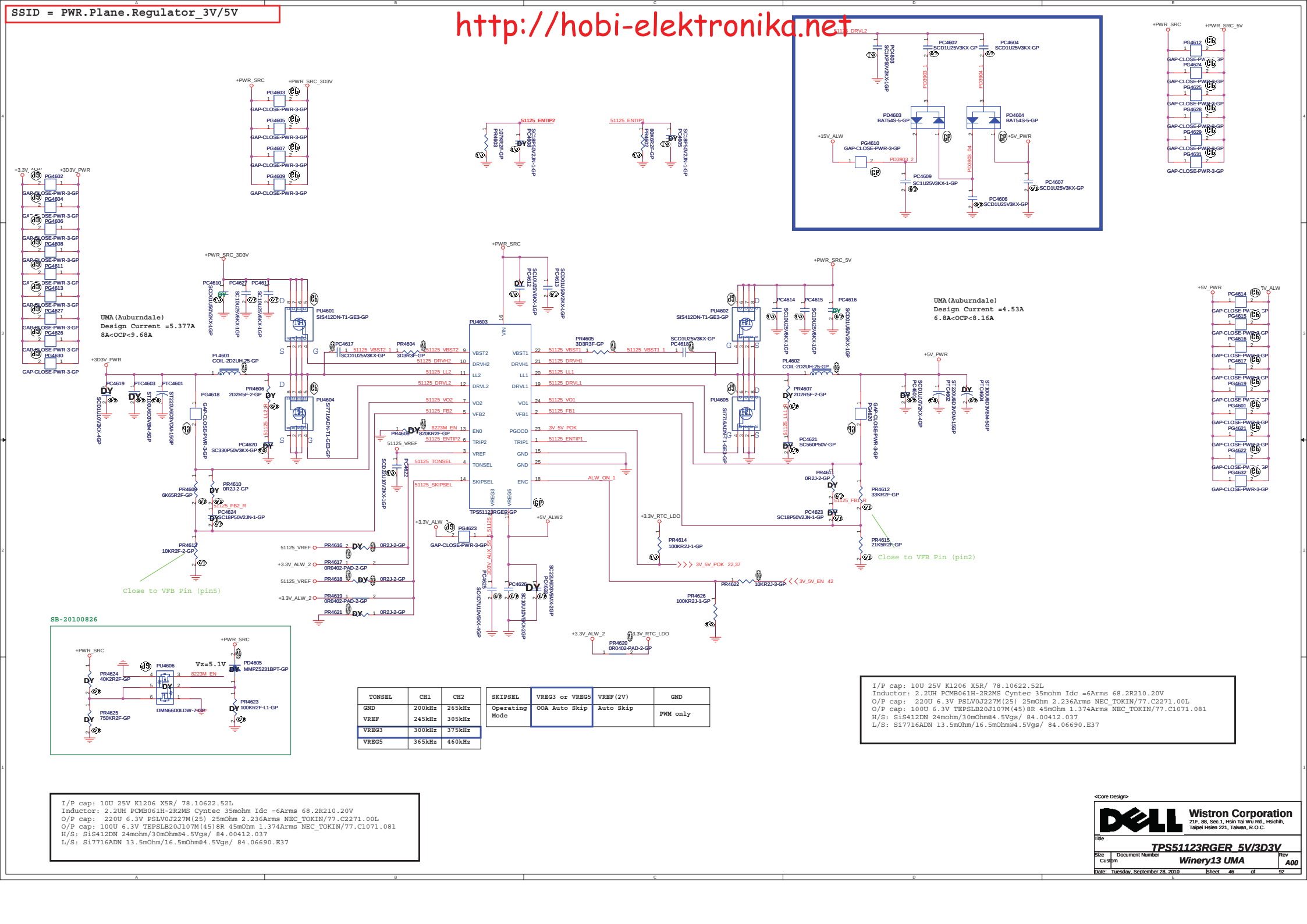

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123RGER_5V/3D3V

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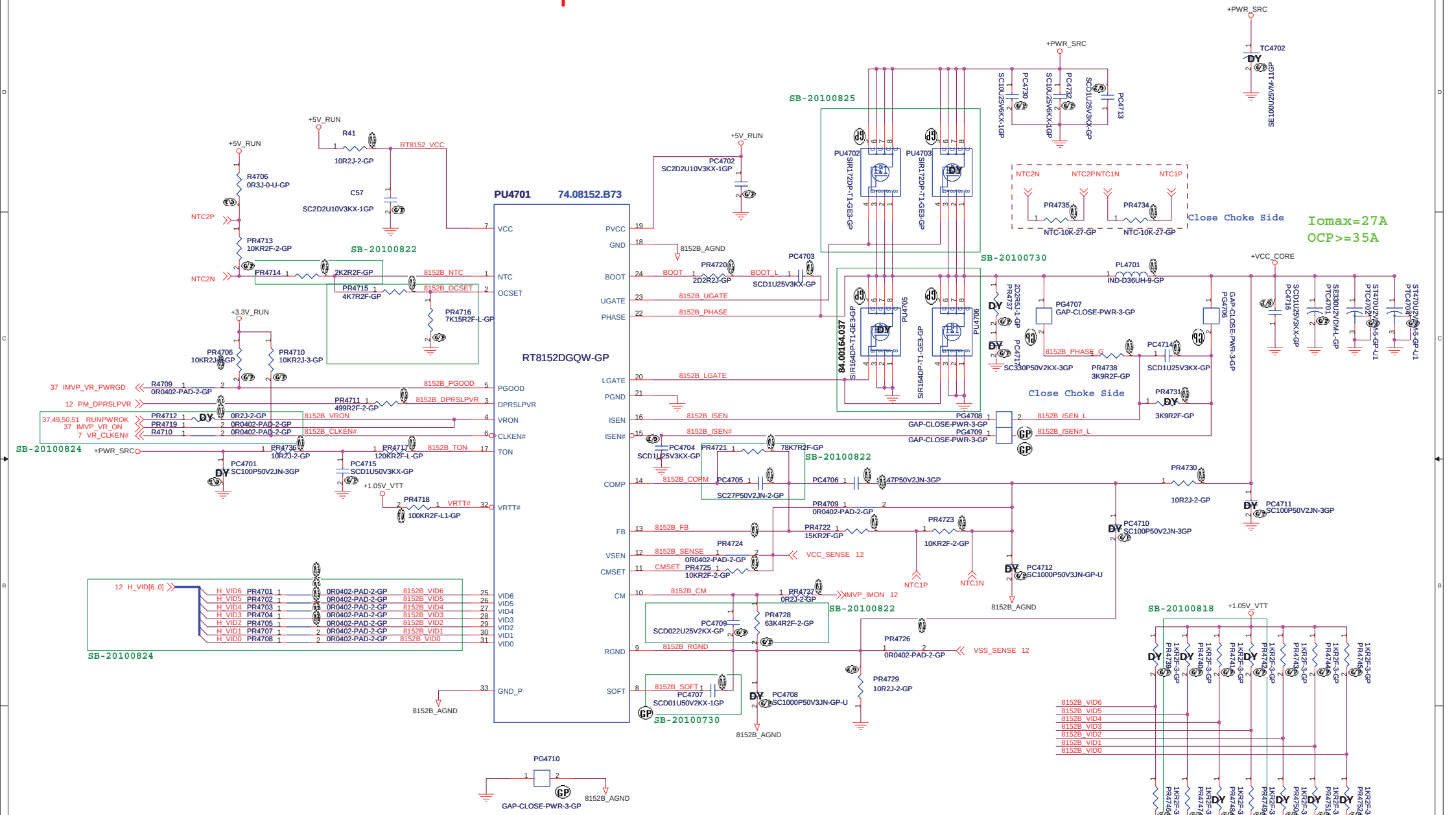

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: CHOKE 0.36UH PCMC104T-R36 Cyntec 1.05mohm Idc =30Arms 68.R3610.20C
O/P cap: EEFLX0D331R EL 330U 2V M 7.3*4.3 6mOhm 3.5Arms PANASONIC 79.33719.2EL
O/P cap: EL330U2V EEFSX0D331ER 9mOhm 3 Arms PANASONIC/79.33719.L01
H/S: SI7686DP 10mohm/14mOhm@4.5Vgs/ 84.07686.A37
L/S: SIR164DP 2.6mOhm/3.2mOhm@4.5Vgs/ 84.00164.037

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Title: RT8152_CPU_CORE

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<Core Design>

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Title: *(Reserved)*

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SSID = PWR.Plane.Regulator_1D05V_VTT

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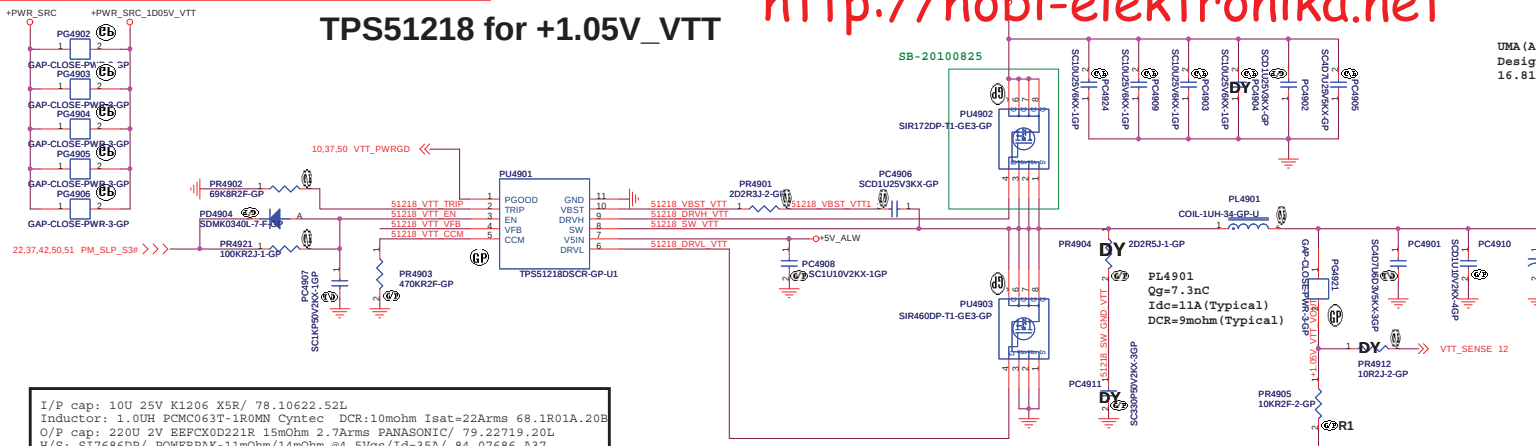
TPS51218 for +1.05V_VTT



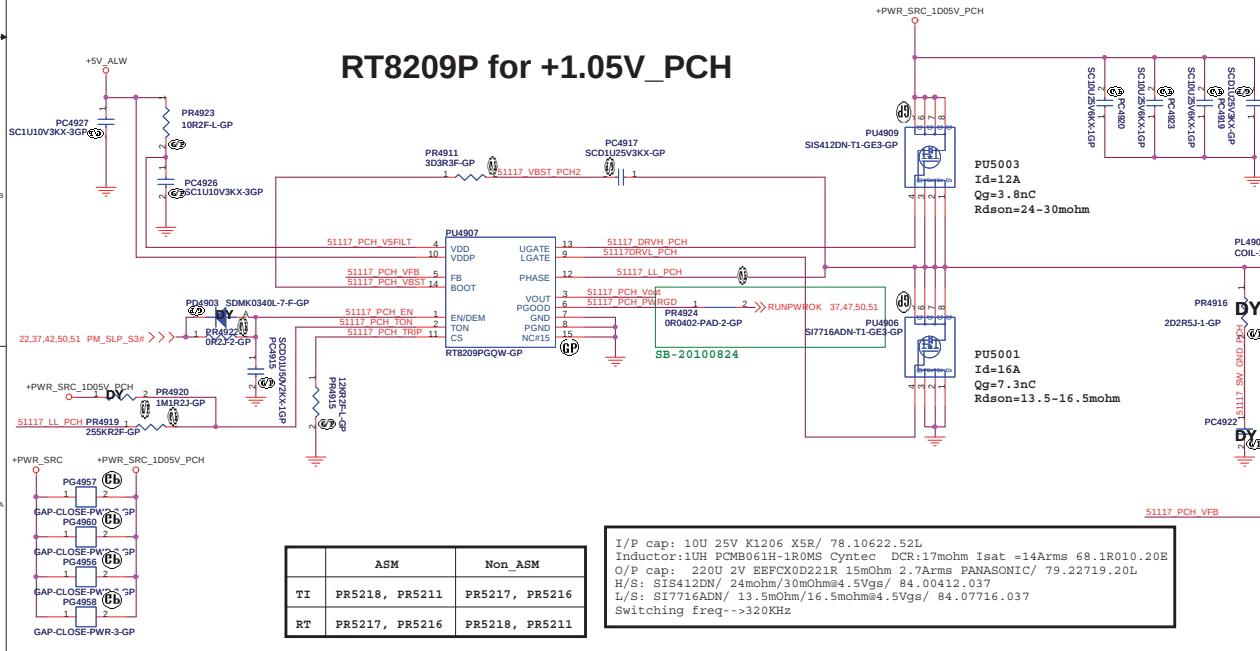
UMA(Arrandale 1.05V_VTT)
Design Current = 11.2A
16.81A<OCP<20.16A

PL4901
Qg=7.3nC
Idc=11A(Typical)
DCR=9mohm(Typical)

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC063T-1R0MN Cyntec DCR:10mohm Isat=22Arms 68.1R01A.20E
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-11mOhm/14mOhm @4.5Vgs/Id=35A/ 84.07686.A37
L/S:SIR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/Id=40A/84.00460.037

Vout=0.704V*(R1+R2)/R2

RT8209P for +1.05V_PCH



PU5003
Id=12A
Qg=3.8nC
Rdson=24~30mohm

PU5001
Id=16A
Qg=7.3nC
Rdson=13.5~16.5mohm

UMA(Arrandale 1.05V_pch)
Design Current = 6.3A
9.45A<OCP<11.34A

	ASM	Non_ASM
TI	PR5218, PR5211	PR5217, PR5216
RT	PR5217, PR5216	PR5218, PR5211

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:1UH PCMB061H-1R0MS Cyntec DCR:17mohm Isat =14Arms 68.1R010.20E
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->320KHz

Vout=0.75V*(R2+R3)/R3

<Core Design>

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Title: TPS51218_+1.05V_VTT
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SSID = PWR.Plane.Regulator_1p5v0p75v

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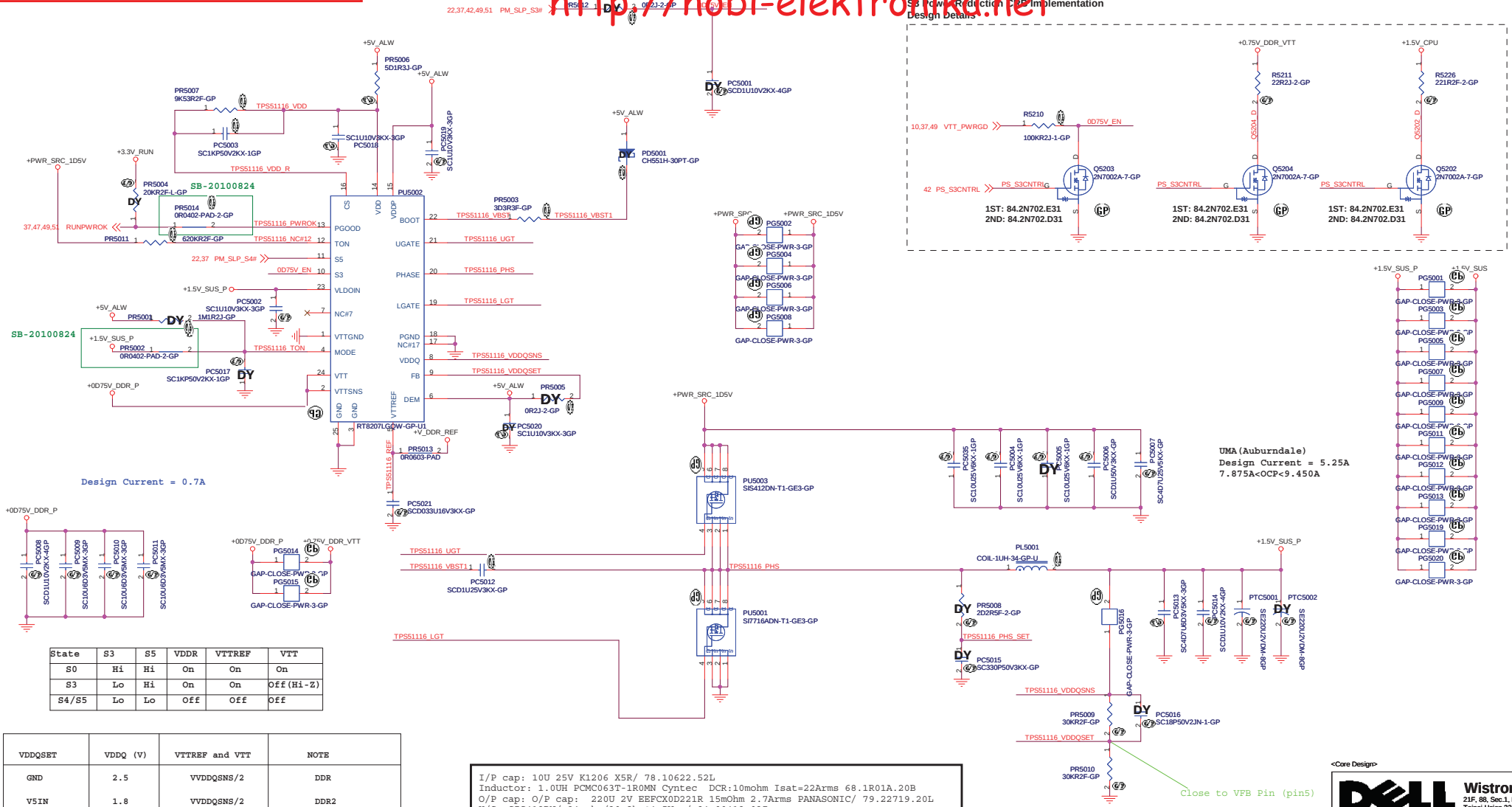
Calpella Platform S3 Power Reduction Platform
S3 Power Reduction DDR Implementation
Design Details



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC063T-1R0MN Cyntec DCR:10mohm Isat=22Arms 68.1R01A.20B
O/P cap: O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->400KHz

<Core Design>

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Title: TPS51116_+1.5V_SUS
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SSID = PWR.Plane.Regulator_1p8v

TPS51311RGTR for +1.8V_RUN

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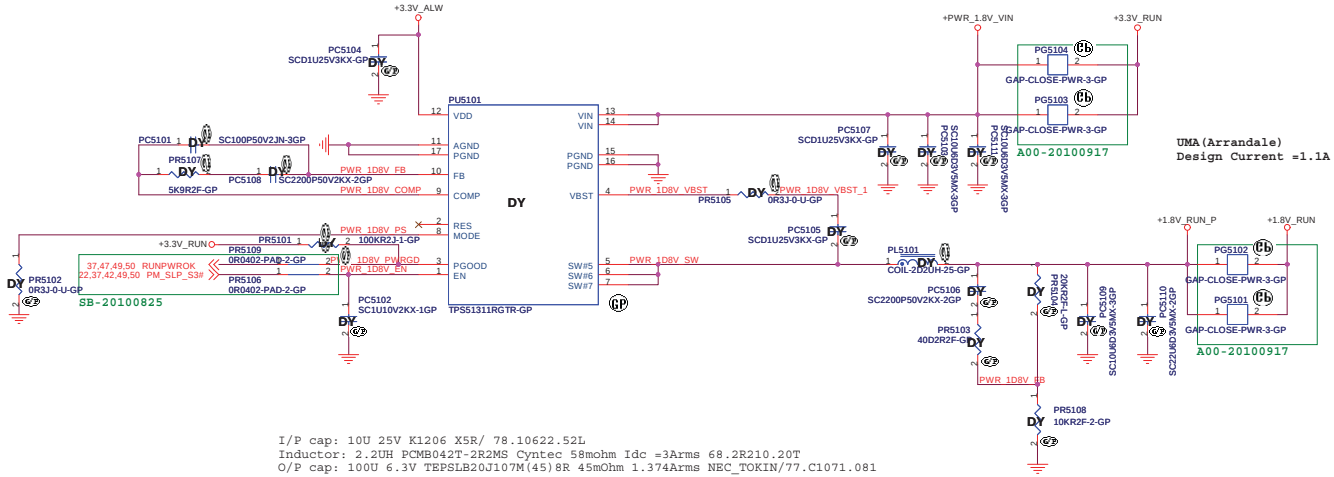
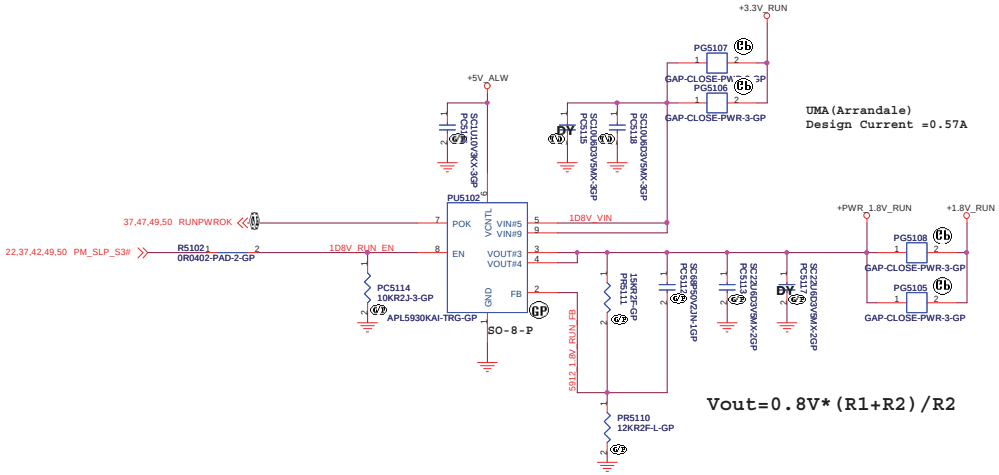


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2UH PCMB042T-2R2MS Cyntec 58mohm Idc =3Arms 68.2R210.20T
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081

SB-20100819

APL5930 for +1.8V_RUN



<Core Design>

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Title: TPS51311 +1.8V_RUN

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<Core Design>

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Title: *(Reserved)*

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SSID = CPU.GFX.Regulator

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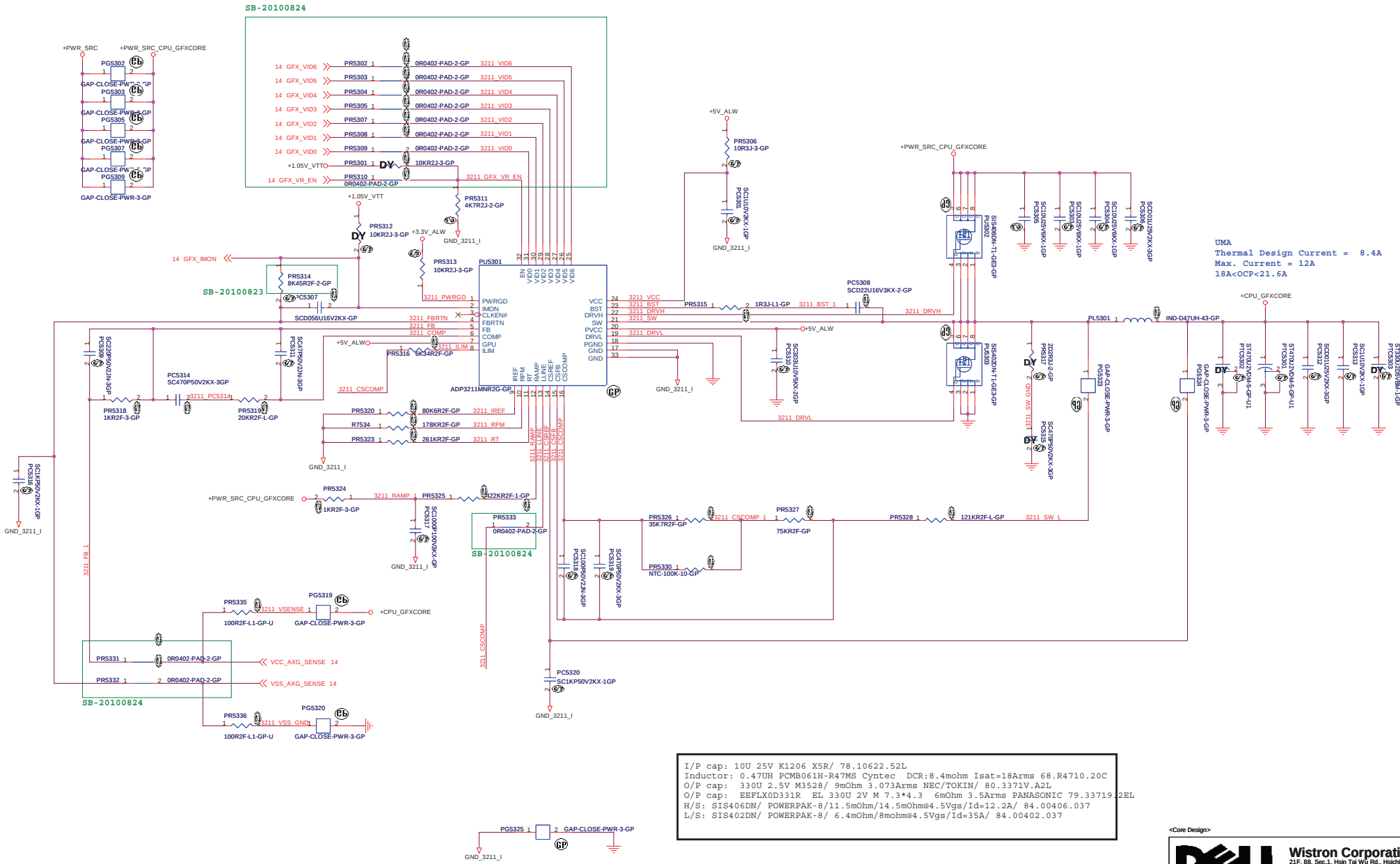

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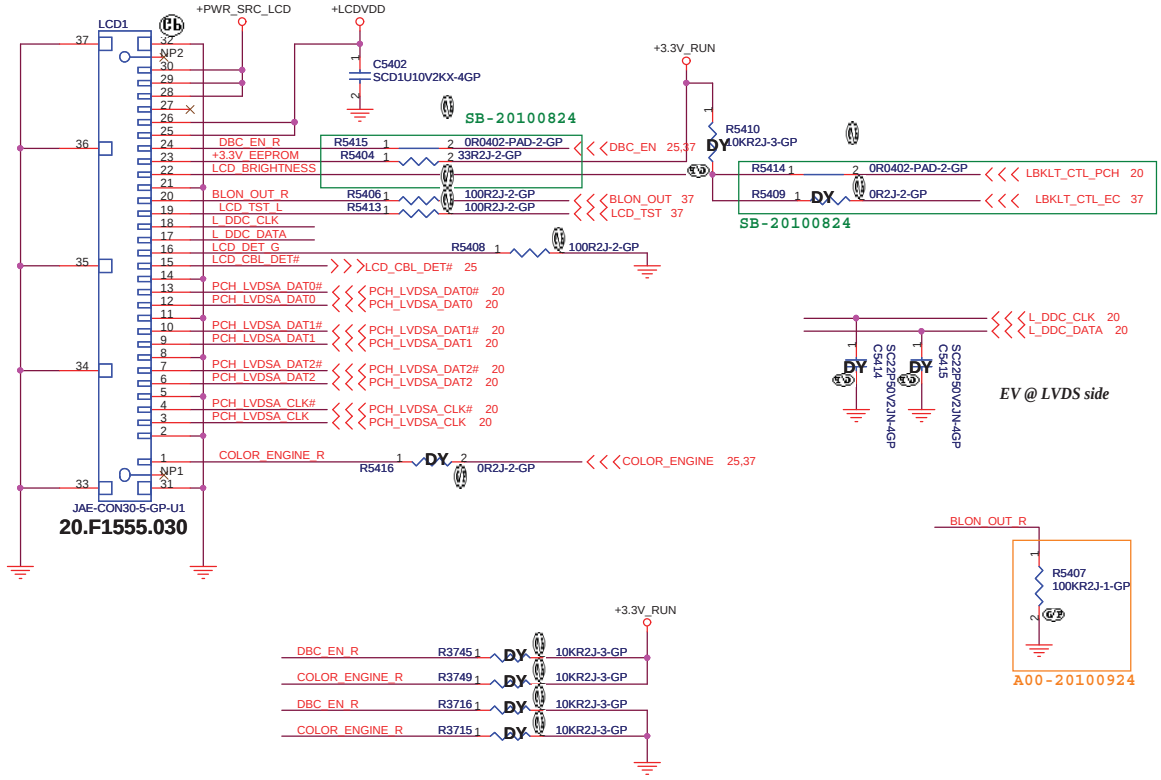
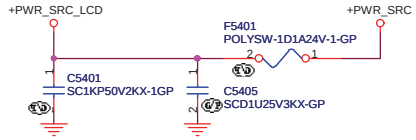
SSID = VIDEO

LVDS CONNECTOR



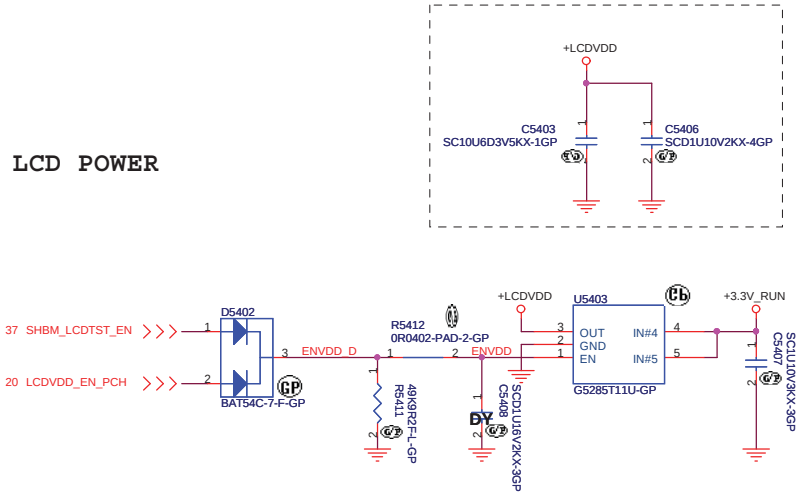
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD/Inverter Connector	
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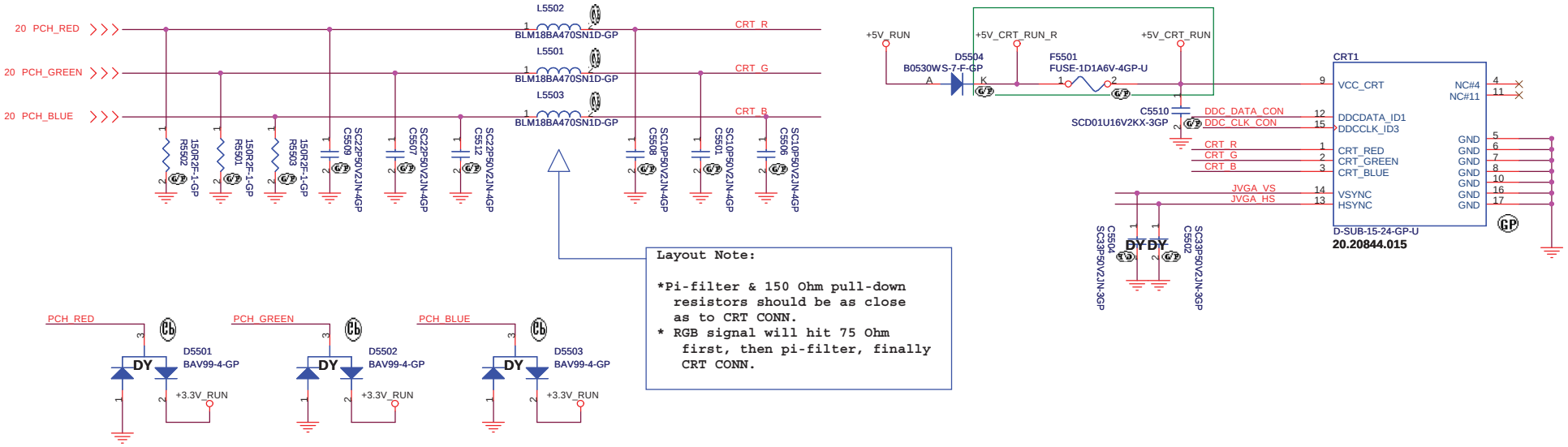
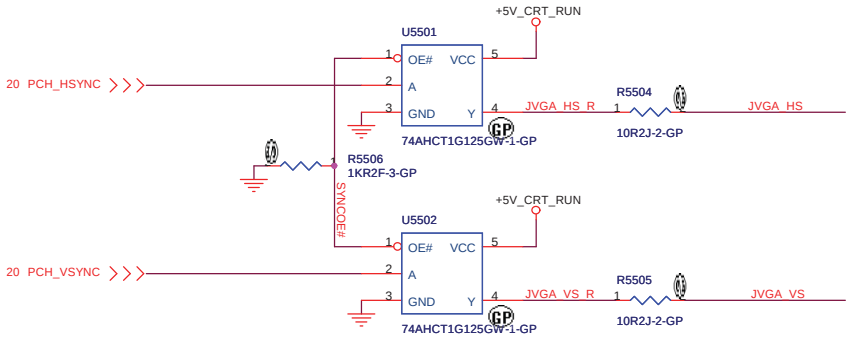
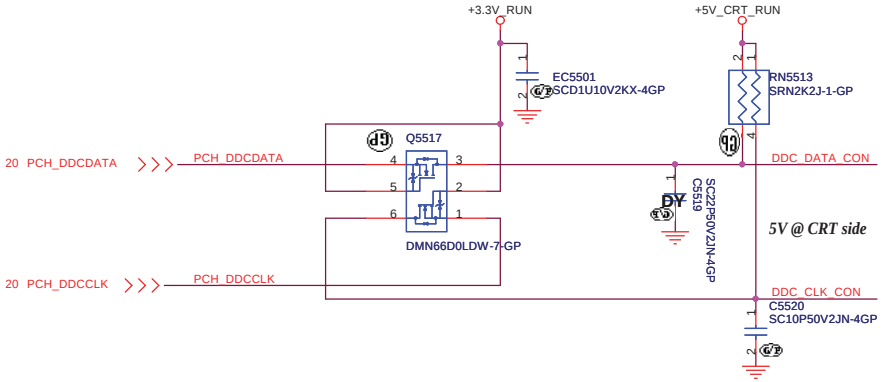
SSID = VIDEO



Hsync & Vsync





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **CRT Connector**

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<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
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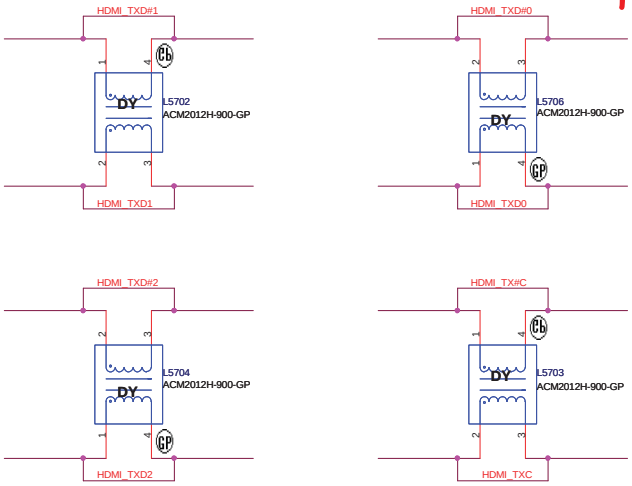
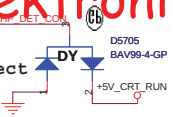
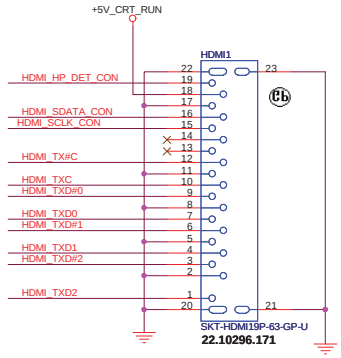
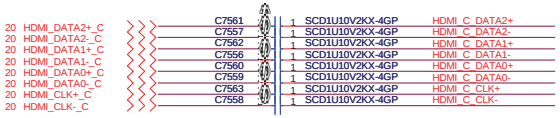


Close HDMI Connect

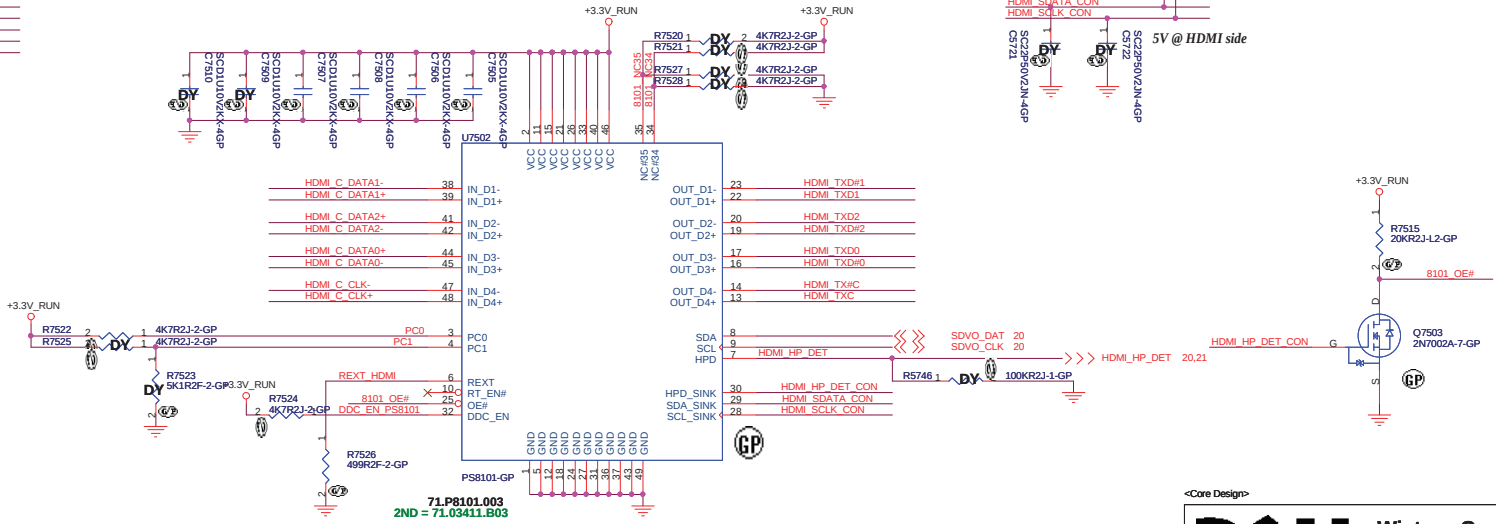


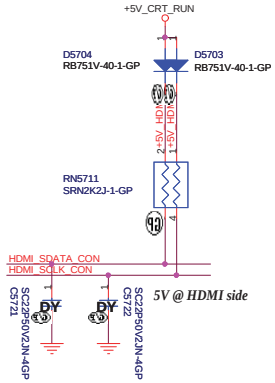




Close to PCH

UMA HDMI level shift circuit





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<Core Design>

Title: HDMI Connector

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SSID = Thermal

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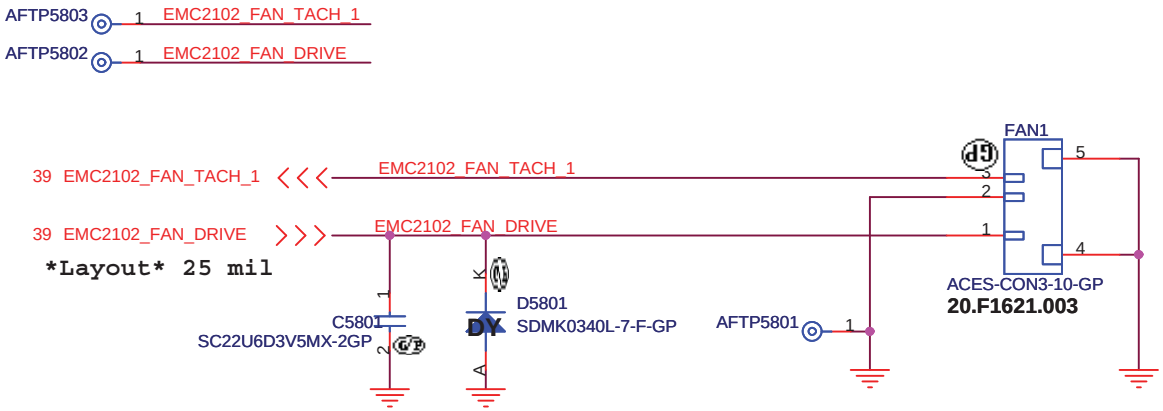
Fan Connector



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: FAN		
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<Core Design>

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Title

(Reserved)

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<Core Design>

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Title

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SSID = LOM

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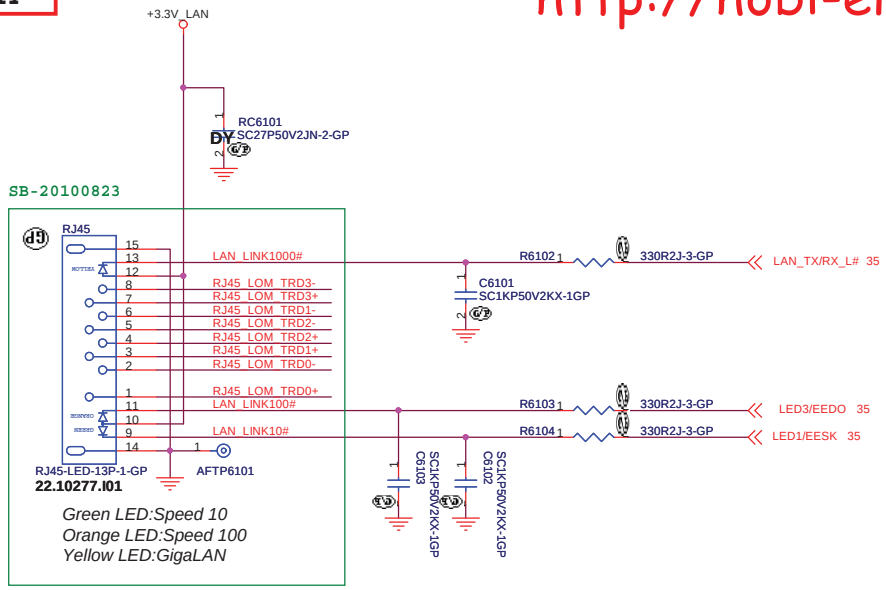
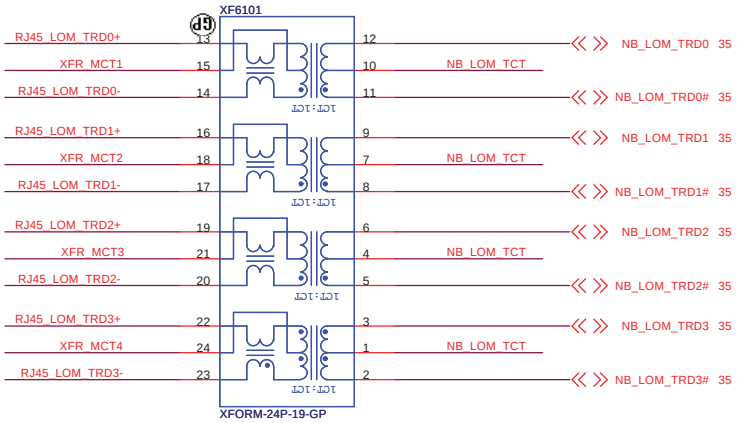
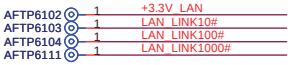
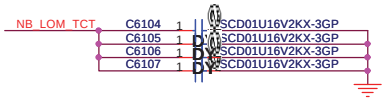


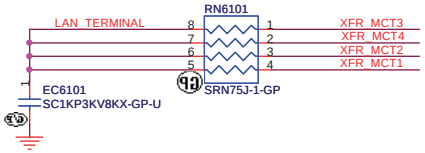
10/100/1000M Lan Transformer



68.IH601.301







1.Route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.Pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

Off /No link – no light
10Mbps – Green
100Mbps – Orange
1000Mbps – Yellow (Orange/Green Combination)
Activity LED - Separate blinking yellow LED to indicate traffic

<Core Design>

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Title: RJ45/Transformer
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SSID = Flash.ROM

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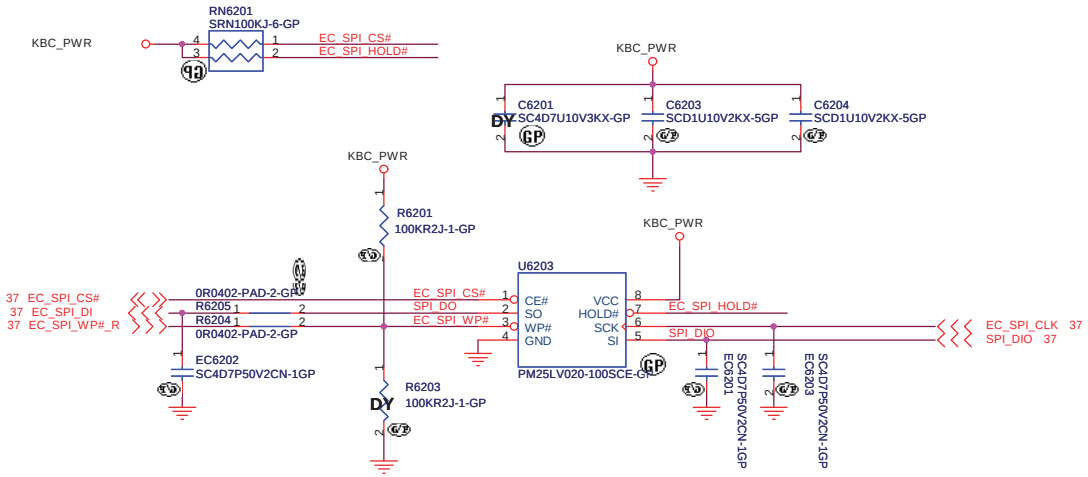
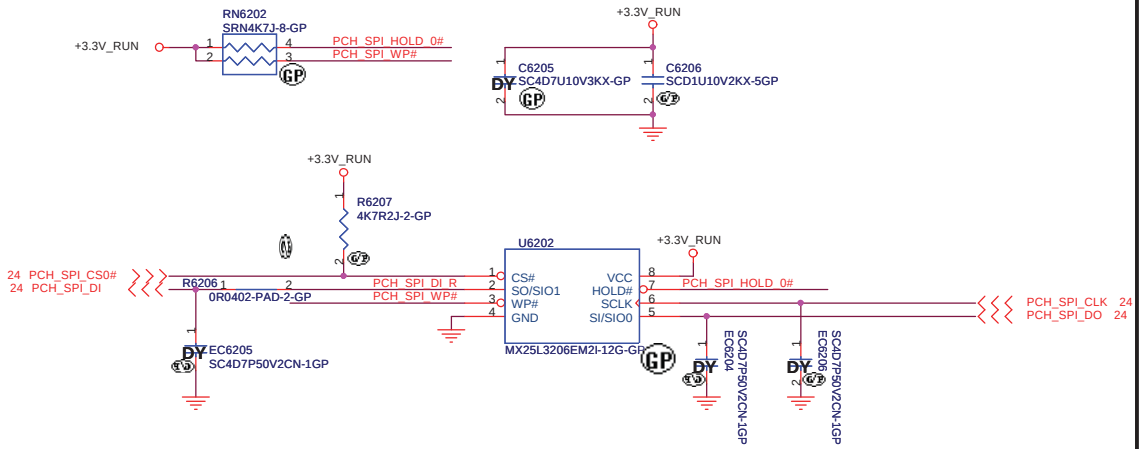
SSID = PBATT

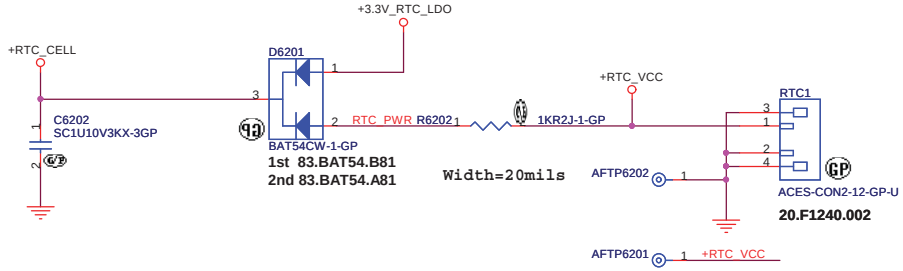
SPI FLASH ROM (2M bits) for KBC



SPI FLASH ROM (32M bits) for PCH



RTC Connector



<Core Design>

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Title	EEPROM/RTC Connector	
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SSID = USB

USB Port Power SW

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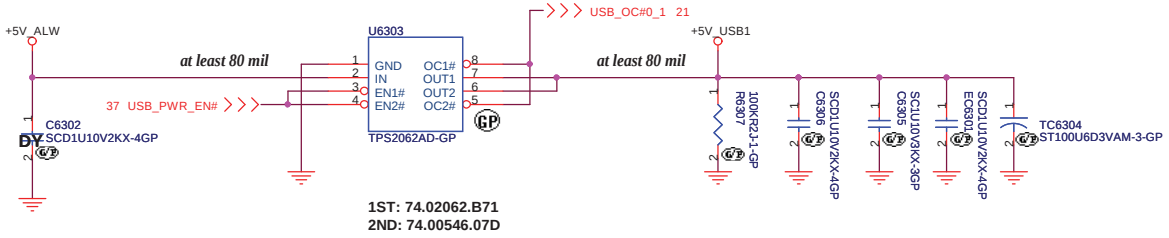
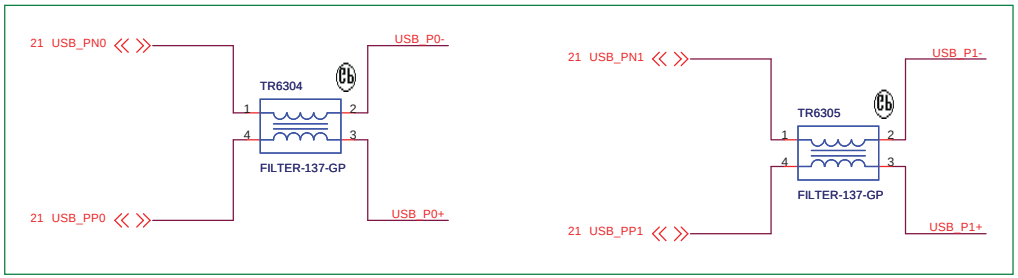
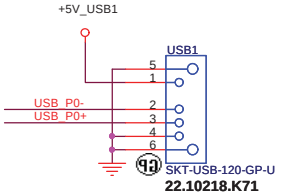
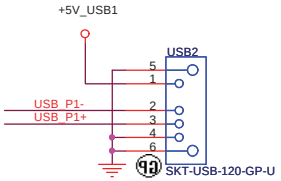


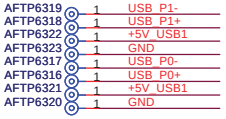
1ST: 74.02062.B71
2ND: 74.00546.07D

SB-20100824



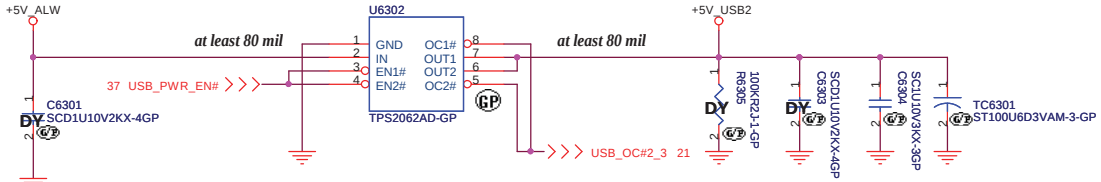






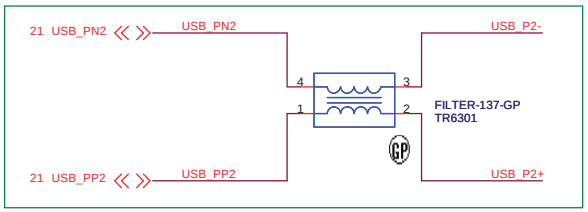
SSID = ESATA

ESATA Power



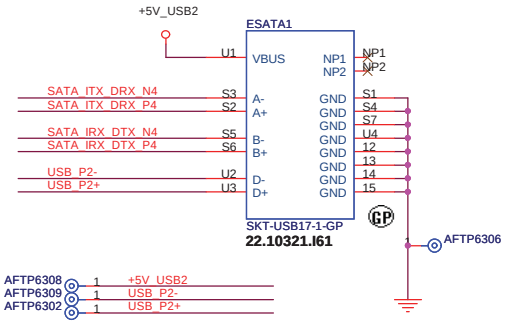
SB-20100824

SB-20100824



SB-20100824

SB-20100824



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Title: USB/ESATA Port

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SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

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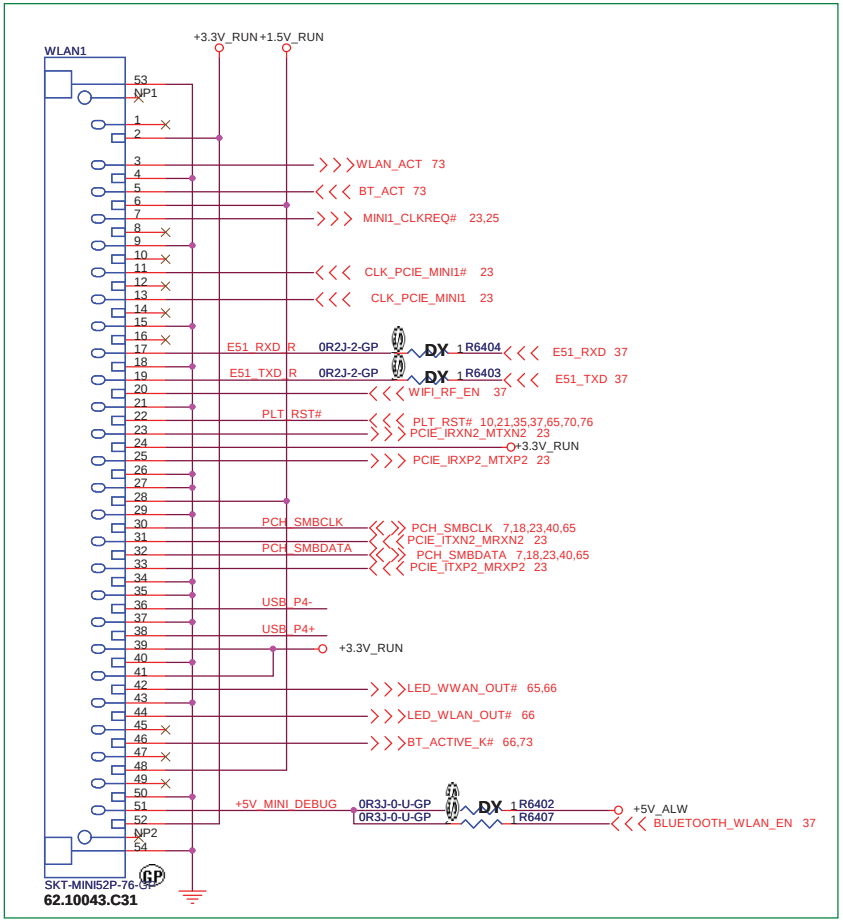
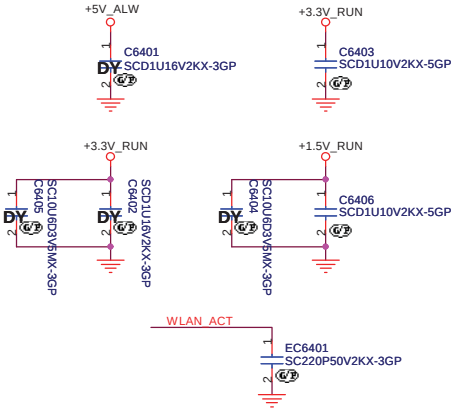
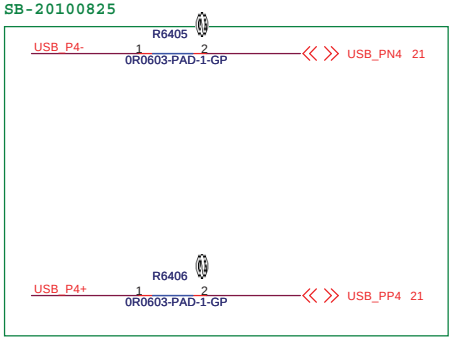




SB-20100825



<Core Design>

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Title: MINICARD(WLAN)/ITP CONN

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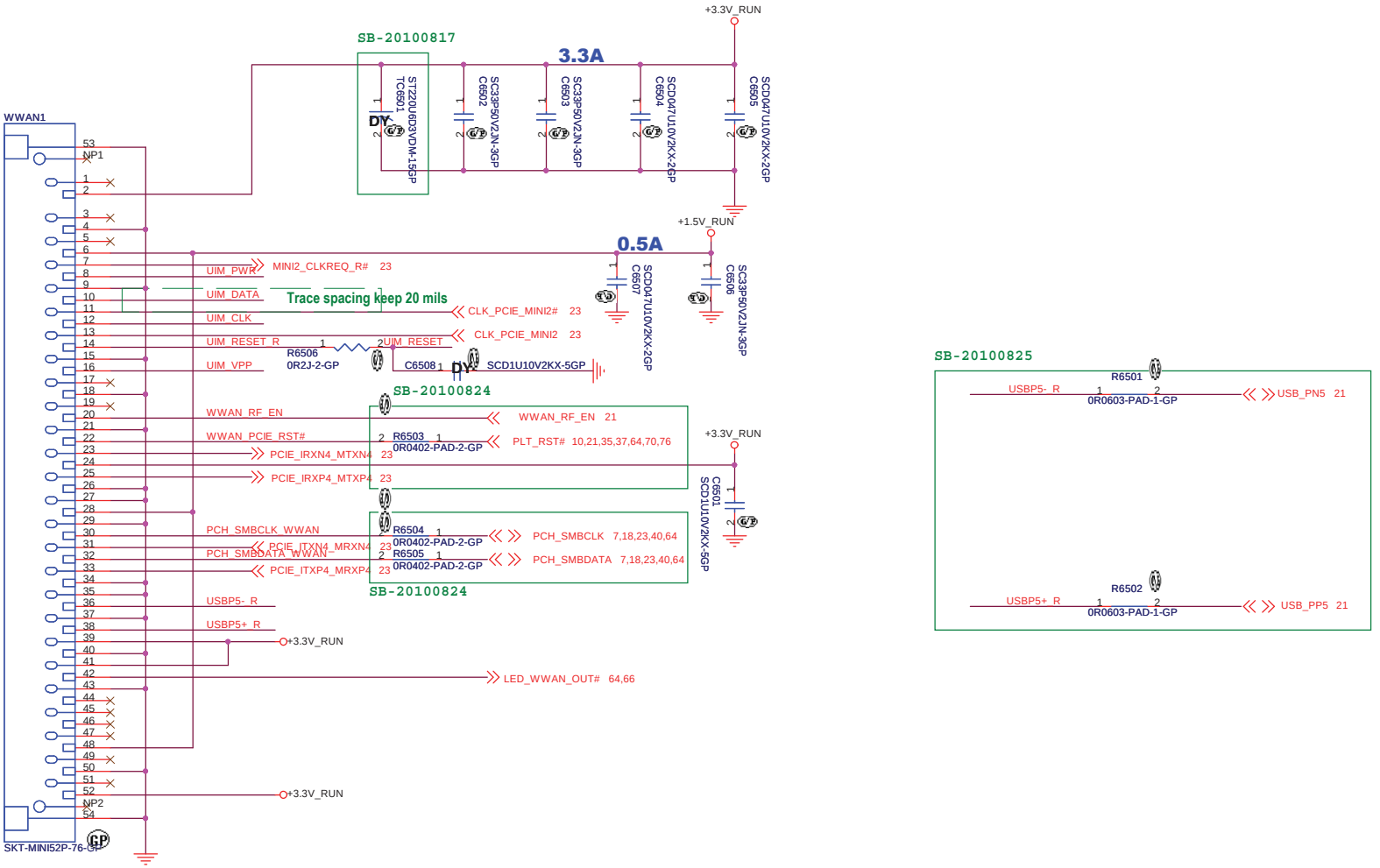
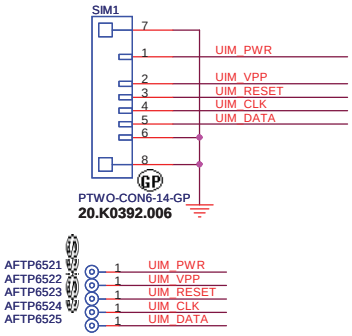
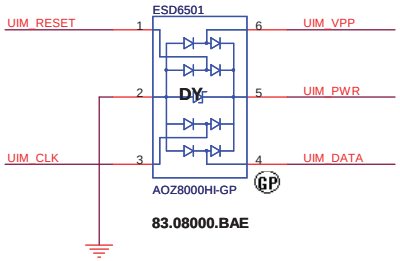
SSID = WWAN

Layout note: Place caps C6501~C6507, TC6501 close WWAN1 connector.

MiniCard WWAN connector







<Core Design>

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Title: **WWAN Connector**

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SSID = LED

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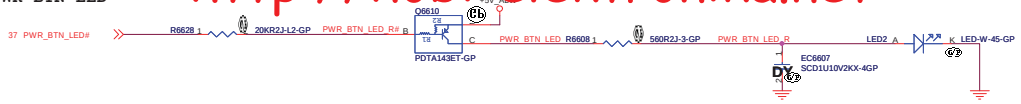
For LED & Capacity board:

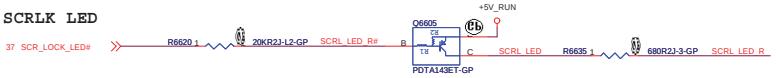
LED Type	Color	Power rail
BATTERY LED1	Amber(Multi-color)	ALW
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN

PWR BTN LED

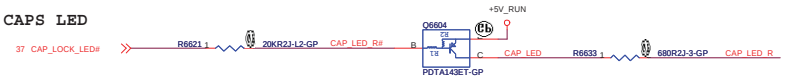


LED Board to Board

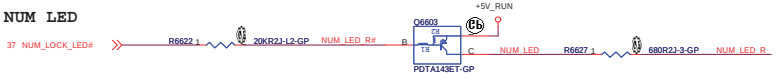
SCRLK LED



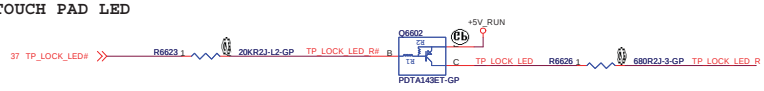
CAPS LED



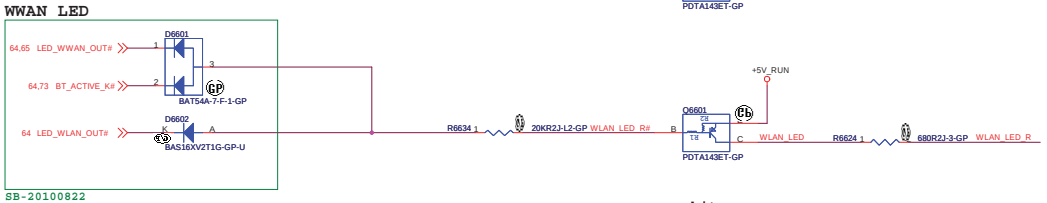
NUM LED



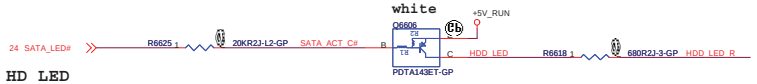
TOUCH PAD LED



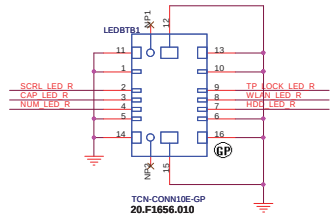
WLAN WIMAX_LED
Bluetooth LED
WWAN LED



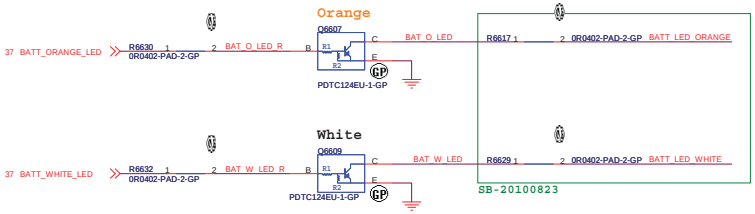
white

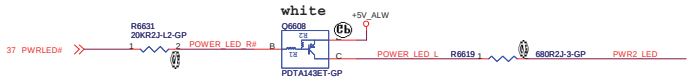


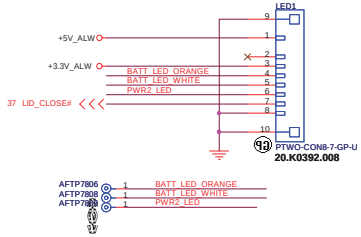
HD LED



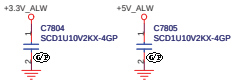
External LED







Close to LED1



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Title: LED

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SSID = KBC

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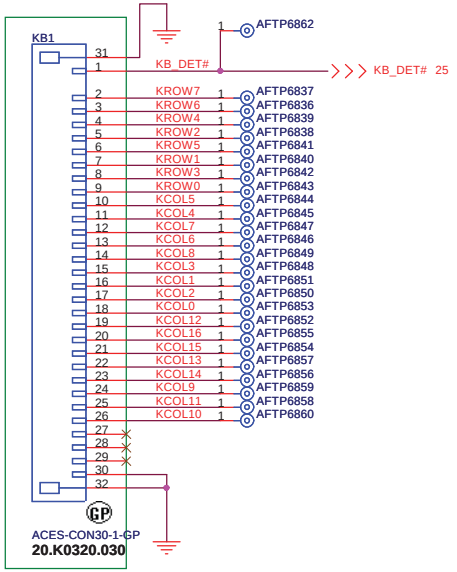
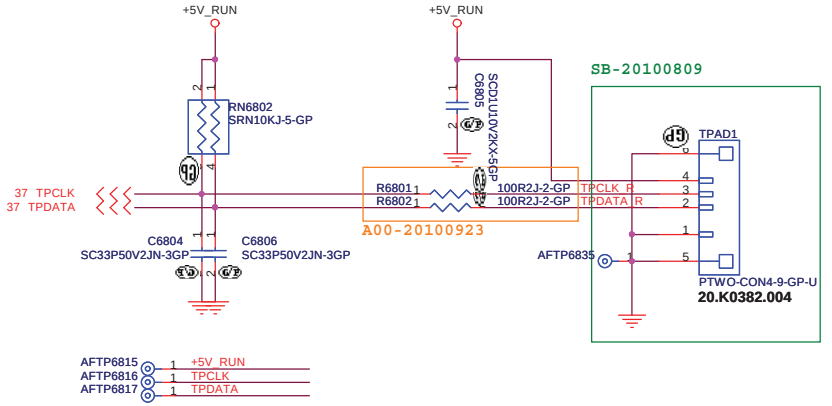
SSID = Touch Pad

Internal KeyBoard Connector



SB-20100813

TouchPad Connector



<Core Design>

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Title: Keyboard/Touch Pad

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Title

Hall sensor

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SSID = DEBUG PORT

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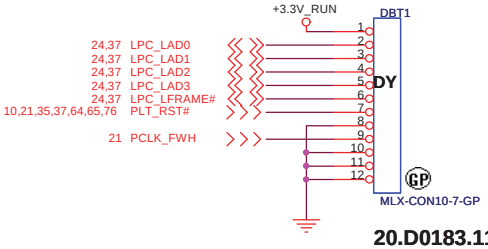
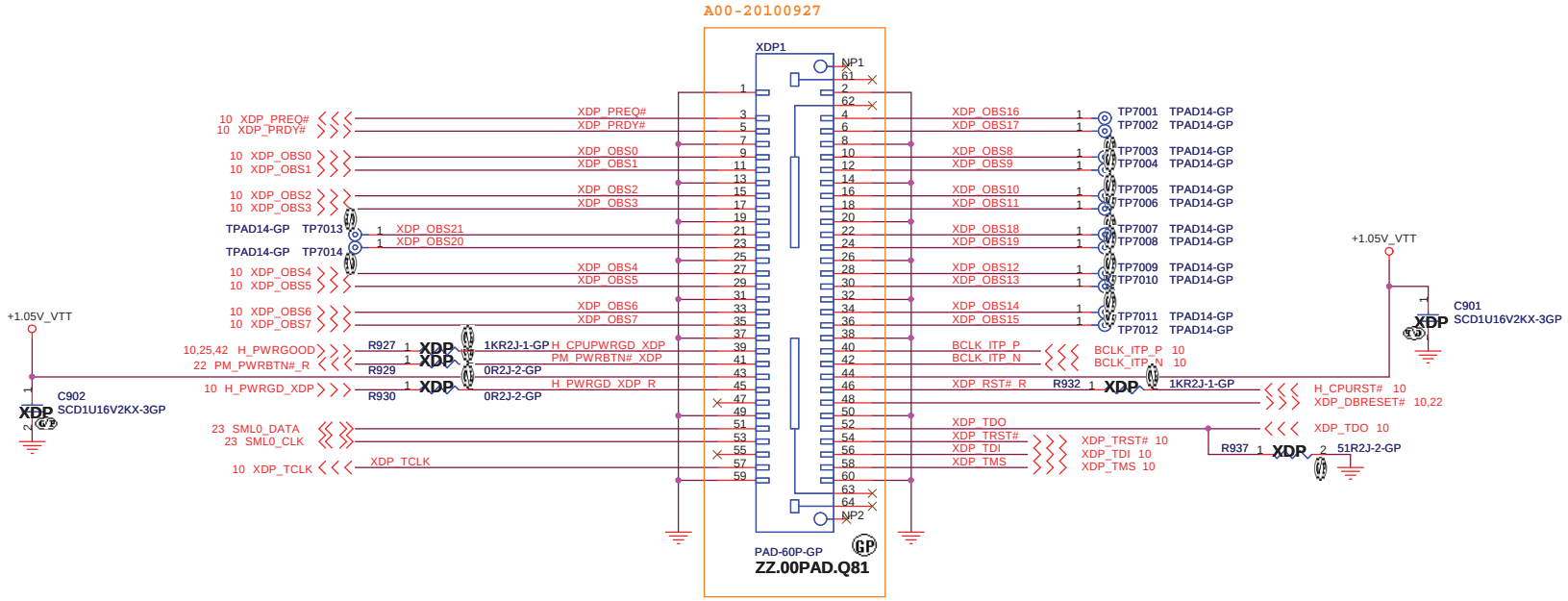
GOLDEN FINGER FOR DEBUG BOARD



20.D0183.110

SSID = CPU



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SSID = User.Interface

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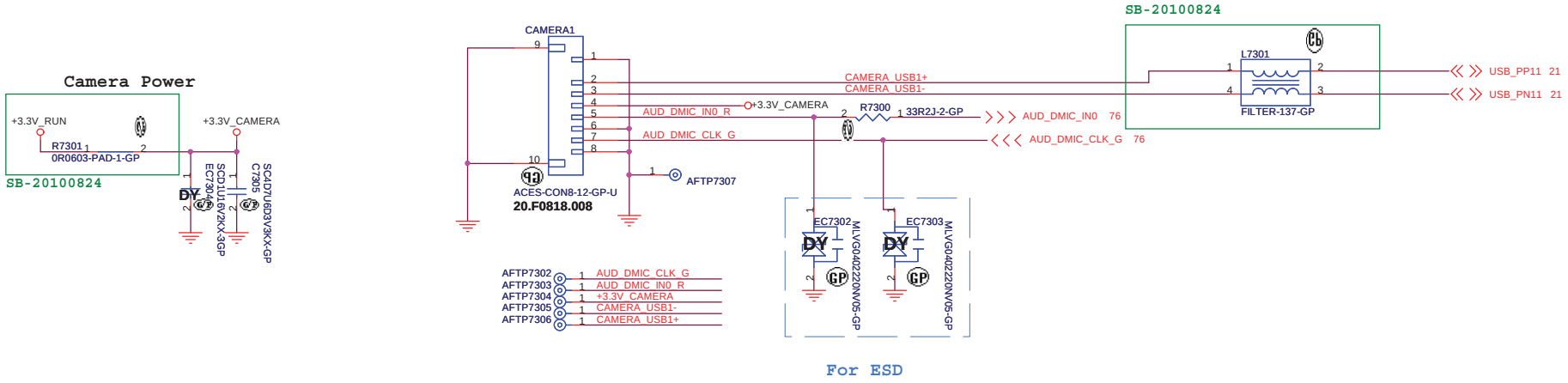
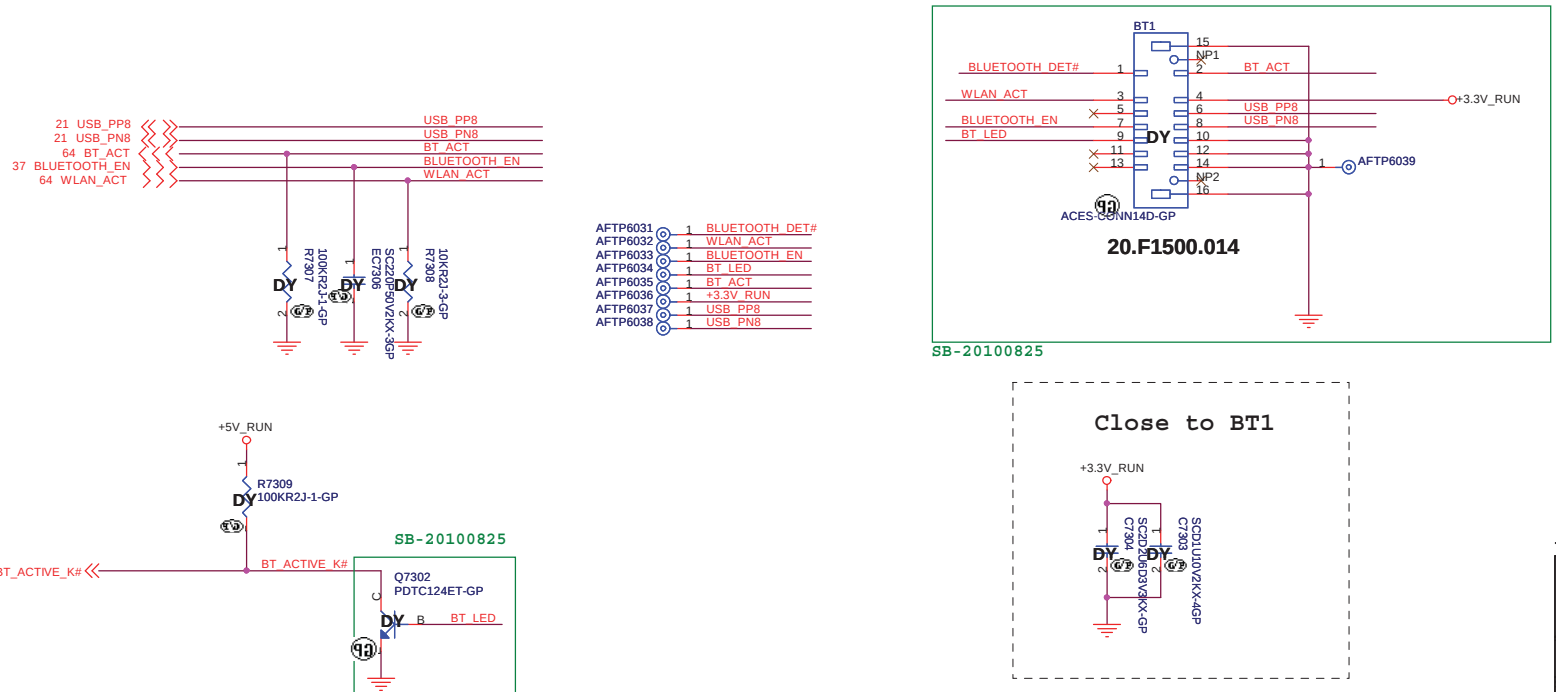
Camera Connector



SSID = User.Interface

Bluetooth cable conn.



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Title: Camera CONN

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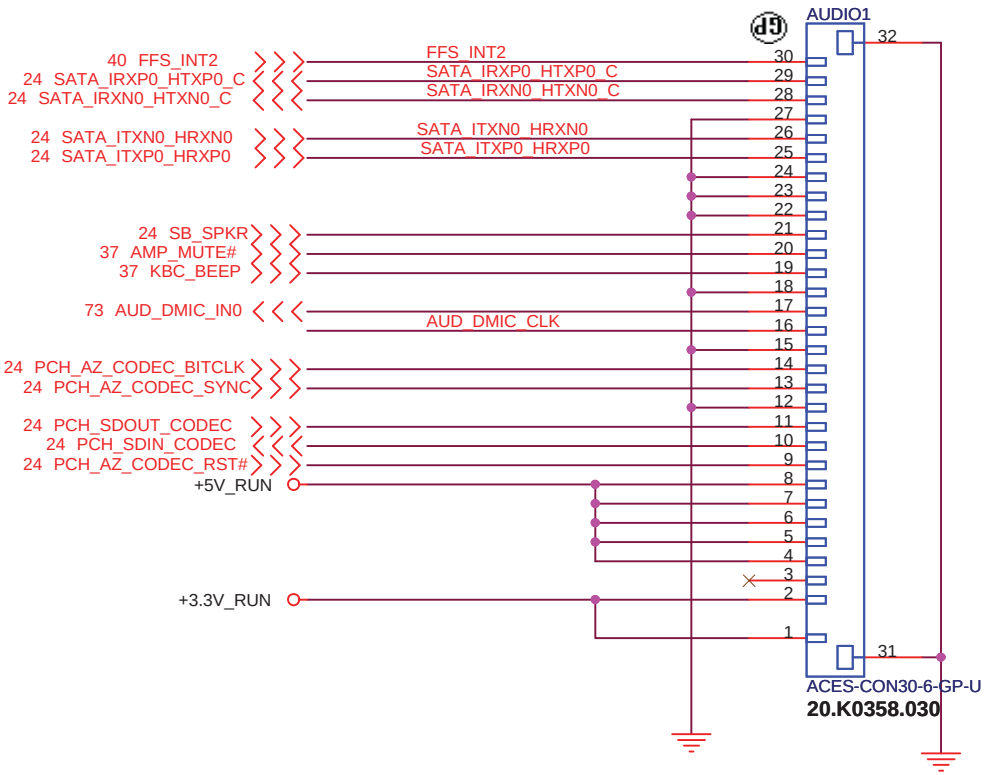
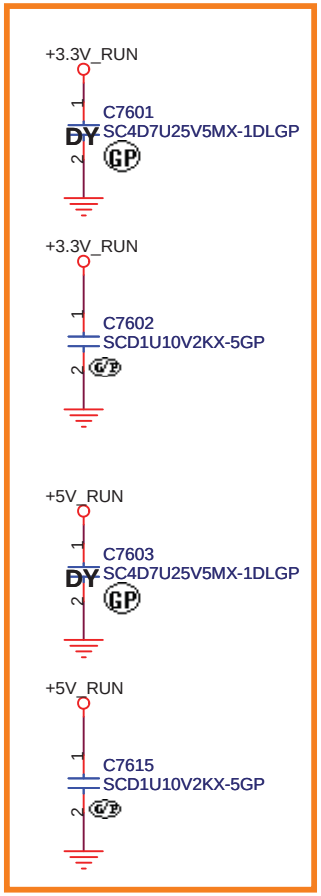
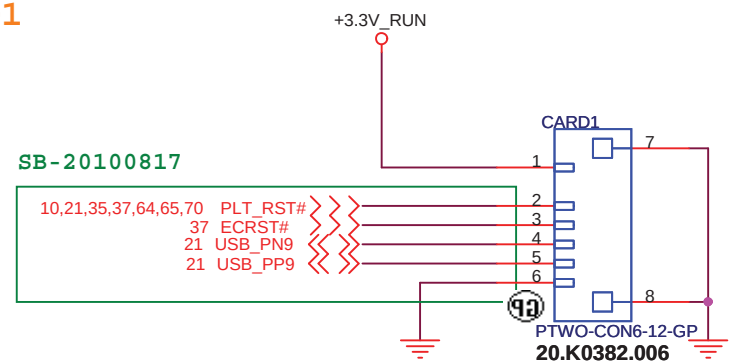
Audio baord CONN



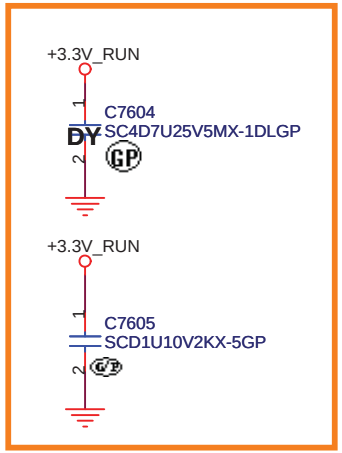
Place near AUDIO1

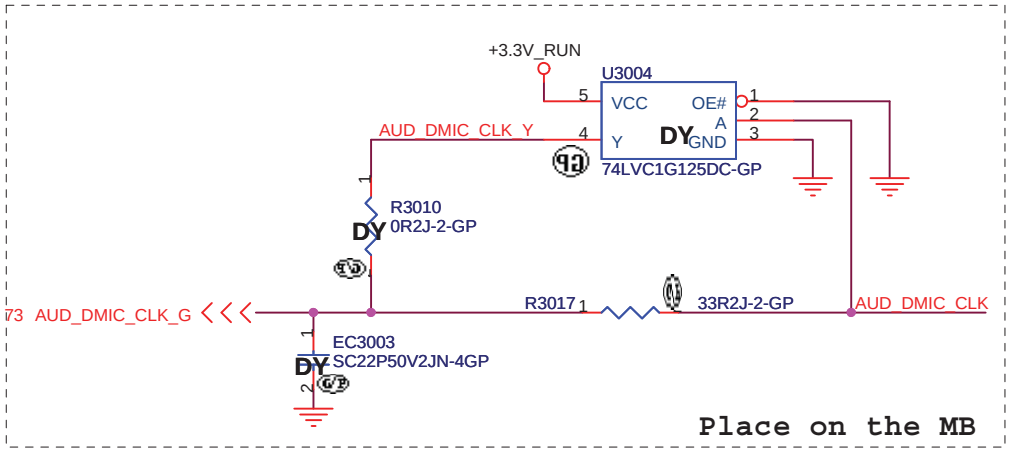


SB-20100817



Place near CARD1





<Core Design>

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Title: DC_IN Board BTB Connector

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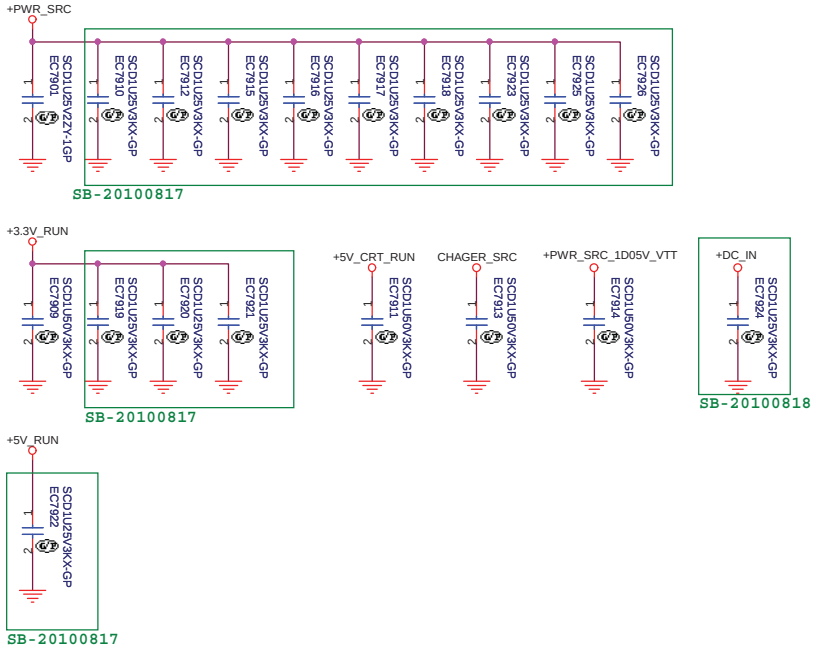
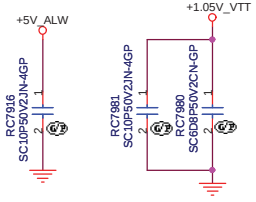
SSID = EMI



SSID = RF



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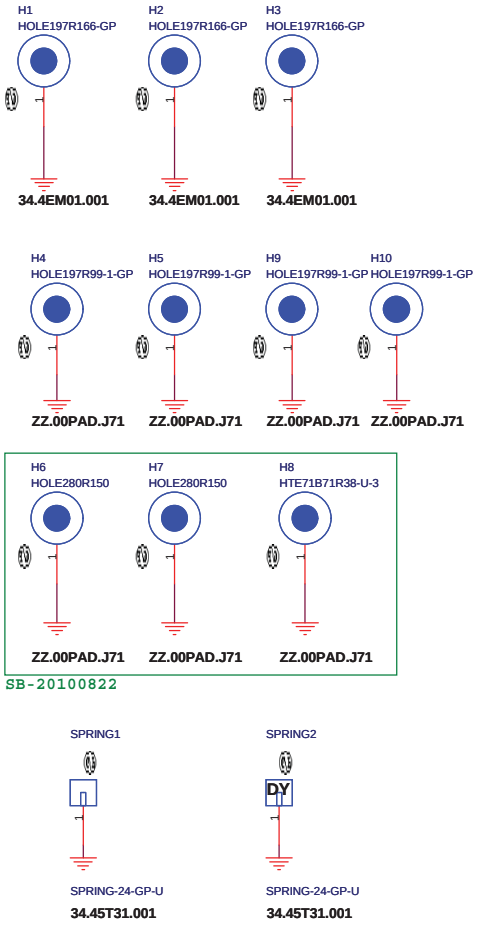

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	43	2010/07/30	EE	+DC_IN short to GND	Modify DCIN1 connector pin4, pin5 connect to GND.	SB
2	37	2010/07/30	EE	SW1 always short to GND.	Change pin 6 connect to GND.	SB
3	68	2010/08/09	EE		Change TPAD1 pin defined.	SB
4	68	2010/08/13	EE		Change KB1 connector to 20.K0320.030.	SB
5	76	2010/08/17	EE		Add ECRST# connect to CARD1 pin 3.	SB
6	79	2010/08/17	EMI		Between +PWR_SRC and GND add 0.1uf/50v cap X 9. Between +3.3V_RUN and GND add 0.1uf/50v cap X 3. Between +5V_RUN and GND add 0.1uf/50v cap X 1. Between +DC_IN and GND add 0.1uf/50v cap X 1. Between +DC_IN and GND add 0.1uf/50v cap.	SB
7	47	2010/08/18	Power		Change +VCC_CORE VID3~5 from 001 to 010.	SB
8	37	2010/08/19	EE		Add LID_CLOSE# pull high resistor to +3.3V_ALW.	SB
9	51	2010/08/19	EE		Co-lay +1.8V_RUN LDO power solution.	SB
10	55	2010/08/19	EE		Between +5V_RUN and +5V_CRT_RUN add Fuse.	SB
11	45	2010/08/22	ME		Change PC4532, PC4530, PC4533 from 1206 size to 0805 size for ME request.	SB
12	45	2010/08/22	Power		Change PU4505 from SIS7716 to SIS412DN (84.00412.037). For cost down.	SB
13	47	2010/08/22	Power		PR4714 change to 2.2K for OTP & OCP setting. PR4715 change to 4.7K for OTP & OCP setting. PR4716 change to 7.15K for OTP & OCP setting. PR4721 change to 78.7K for Load Line & COMP setting. PC4705 change to 27pF for Load Line & COMP setting. PR4728 change to 63.4K for Current Monitor setting. PC4709 change to 22nF for Current Monitor setting.	SB
14	66	2010/08/22	EE		Add D6601, D6602 for wireless function.	SB
15	7	2010/08/23	RF		Add RC701, RC702 for RF request.	SB
16	42	2010/08/23	EE		Change +1.5V_CPU power rail from +1.5V_RUN to +1.5V_SUS.	SB
17	53	2010/08/23	Power		PR5314 :7.5k change to 8.45K(64.84515.6DL) for GFX core imon.	
18	61	2010/08/23	EE		Change RJ45 connector to 22.10277.I01 for hi-port fail.	SB
19	64,65	2010/08/23	EE		Change WLAN1, WWAN1 connector to 62.10043.C31.	SB

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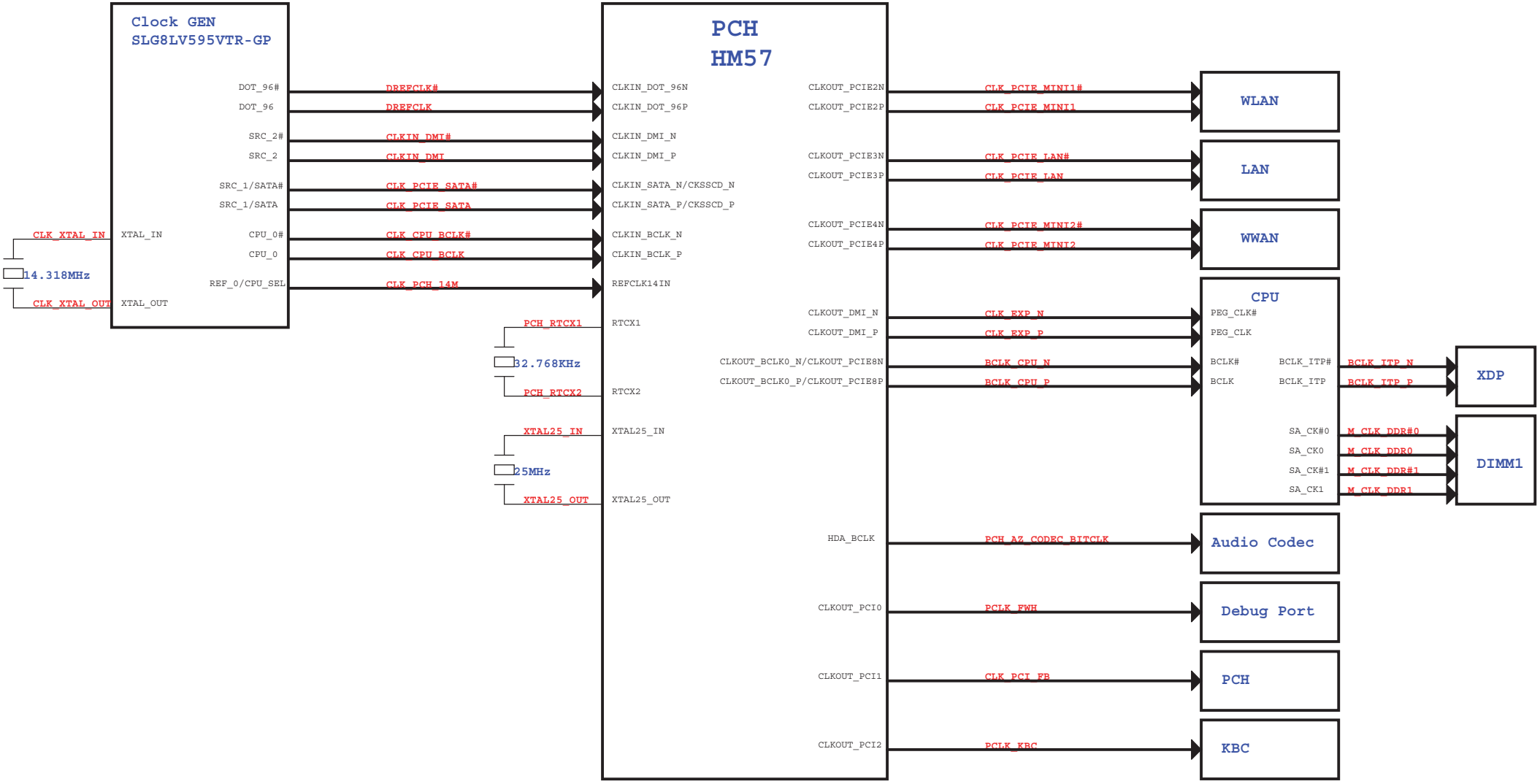

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Title: Clock Block Diagram

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20	66	2010/08/23	EE		Change R6617, R6629 to 0ohm.	SB
21	63,73	2010/08/24	EMI		Change USB port0, port1, port2 and camera from 0 ohm to common chock.	SB
22	73	2010/08/25	EE		Dummy BT 365 function.	SB
23	24	2010/08/25	EE		Change C2402 from 12PF to 5PF.For Vendor recommend. Change C2403 from 12PF to 6PF.For Vendor recommend.	SB
24	7	2010/08/25	EE		Change C714, C715 from 12PF to 15PF for vendor recommend.	SB
25	47,49	2010/08/25	Power	SI7686DP-T1-GE3-GP will EOL.	PU4702, PU4703, PU4902: (SI7686DP-T1-GE3-GP) change to SIR172DP-T1-GE3-GP 84.00172.037	SB

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1	7	2010/08/24	EE	Cost down	Change R708, R709, RN701, RN702, RN703, RN704 from 0 ohm to short pad.	SB
2	10	2010/08/23	EE	Cost down	Dummy U927, R989, R977, Q901, C915, R934, R989. Add R935, R919. Change R920 to 3 K ohm.	SB
3	10	2010/08/24	EE	Cost down	Change R906, R909, R921, R924, R926 from 0 ohm to short pad.	SB
4	20	2010/08/24	EE	Cost down	Change R2011 from 0 ohm to short pad.	SB
5	21	2010/08/24	EE	Cost down	Change R2104, R2121 from 0 ohm to short pad.	SB
6	21	2010/08/24	EE	Cost down	Change R2519, R2102, R2105 from single resistor to array resistor.	SB
7	22	2010/08/24	EE	Cost down	Change R2207, R2210, R2218, R2213, R2216, R2219, R2220, R2211, R2212 from 0 ohm to short pad.	SB
8	23	2010/08/24	EE	Cost down	Change RN2311, RN2312, RN2314 from 0 ohm to short pad.	SB
9	23	2010/08/24	EE	Cost down	Change R2302, R2201, R2301, R2209 from single resistor to array resistor.	SB
10	24	2010/08/24	EE	Cost down	Change R2417 from 0 ohm to short pad.	SB
11	25	2010/08/24	EE	Cost down	Change R2521, R2334, R2522, R2512, R2411, R2513, R2217, R2538, R2304, R2533, R2416, R2503, R2535, R2214 from single resistor to array resistor.	SB
12	26	2010/08/24	EE	Cost down	Change R2606, R2605, R2601, R2609, R2602 from 0 ohm to short pad.	SB
13	27	2010/08/24	EE	Cost down	Change R2707 from 0 ohm to short pad.	SB
14	35	2010/08/24	EE	Cost down	Change R3509, R3512, R3508, R3514 from 0 ohm to short pad.	SB
15	35	2010/08/24	EE	Cost down	Change R3517, R3518 from single resistor to array resistor.	SB
16	37	2010/08/24	EE	Cost down	Change R3706, R3730, RR3720, R3707, R3753, R3702, R3723, R3727 from 0 ohm to short pad.	SB
17	37	2010/08/24	EE	Cost down	Change R3742, R3743 from single resistor to array resistor.	SB
18	39	2010/08/24	EE	Cost down	Change R3910, R3906 from single resistor to array resistor.	SB
19	44	2010/08/24	EE	Cost down	Change R4401 from 0 ohm to short pad.	SB

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20	45	2010/08/24	EE	Cost down	Change PR4522, PR4515, PR4530, PR4531, PR4533, PR4524 from 0 ohm to short pad.	SB
21	46	2010/08/26	EE	Cost down	Dummy PU4606, PD4605, PR4623, PR4624, PR4625.	SB
22	47	2010/08/24	EE	Cost down	Change PR4719, R4710, PR4701, PR4702, PR4703, PR4704, PR4705, PR4707, PR4708 from 0 ohm to short pad.	SB
23	49	2010/08/24	EE	Cost down	Change PR4924 from 0 ohm to short pad.	SB
24	50	2010/08/24	EE	Cost down	Change PR5014, PR5002 from 0 ohm to short pad.	SB
25	53	2010/08/24	EE	Cost down	Change PR5302, PR5303, PR5304, PR5305, PR5307, PR5308, PR5309, PR5310, PR5331, PR5332, PR5333 from 0 ohm to short pad.	SB
26	54	2010/08/24	EE	Cost down	Change R5415, R5414 from 0 ohm to short pad.	SB
27	63	2010/08/24	EE	Cost down	Change R6304, R6310, R6311, R6312 from 0 ohm to short pad.	SB
28	64	2010/08/25	EE	Cost down	Change R6405, R6406 from 0 ohm to short pad.	SB
29	65	2010/08/24	EE	Cost down	Change R6503, R6504, R6505, R6501, R6502 from 0 ohm to short pad.	SB

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